`--print-instruction-encoding`	`-hex`	When specified, print the encoding bytes after each operation.
`--print-life-ranges`	`-plr`	Print register life range information in a trailing col produced disassembly.
`--print-line-info`	`-g`	Annotate disassembly with source line information .debug_line section, if present.
`--print-raw`	`-raw`	Print the disassembly without any attempt to beaut
`--separate-functions`	`-sf`	Separate the code corresponding with function sym lines to let them stand out in the printed disassemb
`--version`	`-V`	Print version information on this tool.

4. Instruction Set Reference

This is an instruction set reference for NVIDIA® GPU architectures Fermi, Kepler, Maxwell, Pascal, Volta and Turing.

4.1. Fermi Instruction Set

The Fermi architecture (Compute Capability 2.x) has the following instruction set format:

```
(instruction) (destination) (source1), (source2) ...
```

Valid destination and source locations include:

- RX for registers
- SRX for special system-controlled register
- PX for condition register
- c[X][Y] for constant memory

Table 4 lists valid instructions for the Fermi GPUs.

Table 4. Fermi Instruction Set

Opcode	Description
Floating Point Instructions	
FFMA	FP32 Fused Multiply Add
FADD	FP32 Add
FCMP	FP32 Compare
FMUL	FP32 Multiply
FMNMX	FP32 Minimum/Maximum
FSWZ	FP32 Swizzle
FSET	FP32 Set
FSETP	FP32 Set Predicate
RRO	FP Range Reduction Operator
MUFU	FP Multi-Function Operator
DFMA	FP64 Fused Multiply Add
DADD	FP64 Add
DMUL	FP64 Multiply
DMNMX	FP64 Minimum/Maximum