
 **DEVELOPER ZONE**

**CUDA TOOLKIT DOCUMENTATION**



CUDA Toolkit v10.2.89

CUDA Binary Utilities

▼ 1. Overview

1.1. What is a CUDA Binary?

1.2. Differences between cuobjdump and nvdisasm

▼ 2. cuobjdump

2.1. Usage

2.2. Command-line Options

▼ 3. nvdisasm

3.1. Usage

3.2. Command-line Options

▼ 4. Instruction Set Reference

4.1. Fermi Instruction Set

4.2. Kepler Instruction Set

4.3. Maxwell and Pascal Instruction Set

4.4. Volta Instruction Set

4.5. Turing Instruction Set

▼ 5. nvprune

5.1. Usage

5.2. Command-line Options

--print-instruction-encoding

-hex

when specified, print the encoding bytes after each operation.

--print-life-ranges

-plr

Print register life range information in a trailing column produced disassembly.

--print-line-info

-g

Annotate disassembly with source line information from .debug\_line section, if present.

--print-raw

-raw

Print the disassembly without any attempt to beautify.

--separate-functions

-sf

Separate the code corresponding with function symbols to let them stand out in the printed disassembly.

--version

-V

Print version information on this tool.

## 4. Instruction Set Reference

This is an instruction set reference for NVIDIA® GPU architectures Fermi, Kepler, Maxwell, Pascal, Volta and Turing.

### 4.1. Fermi Instruction Set

The Fermi architecture (Compute Capability 2.x) has the following instruction set format:

(instruction) (destination) (source1), (source2) ...

Valid destination and source locations include:

- RX for registers
- SRX for special system-controlled register
- PX for condition register
- c[X][Y] for constant memory

[Table 4](#) lists valid instructions for the Fermi GPUs.

Opcode	Description
Floating Point Instructions	
FFMA	FP32 Fused Multiply Add
FADD	FP32 Add
FCMP	FP32 Compare
FMUL	FP32 Multiply
FMNMX	FP32 Minimum/Maximum
FSWZ	FP32 Swizzle
FSET	FP32 Set
FSETP	FP32 Set Predicate
RRO	FP Range Reduction Operator
MUFU	FP Multi-Function Operator
DFMA	FP64 Fused Multiply Add
DADD	FP64 Add
DMUL	FP64 Multiply
DMNMX	FP64 Minimum/Maximum

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