Shuai Zhang

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EDUCATION

Columbia University in the City of New York — New York, NY
M.S. Computer Engineering — Dec 2022
GPA: 3.5 / 4.0

University of Wisconsin-Madison — Madison, WI
B.S. Electrical Engineering & B.S. Computer Science — May 2021
GPA: 3.6 / 4.0

PROFESSIONAL EXPERIENCE

Arm, Inc. — Chandler, AZ
Verification Engineer — Apr 2024 - Present

- Owned verification of the Request Node (RNID) module in the Arm Coherent Mesh Network (CMN).
- Mentored and onboarded new team members in the RNID Val group, guiding them in verification methodology.
- Collaborated with the RTL team to develop detailed test plans for new CMN features.
- Coordinated with the top-level team to ensure regression stability and health.
- Developed unit-level UVM testbenches for RNID functional verification.
- Investigated and debugged regression failures in various components and environments.
- Defined and implemented functional and statistical coverage metrics, driving coverage closure.

Arm, Inc. — Chandler, AZ
Graduate Verification Engineer — Feb 2023 - Mar 2024

- Developing comprehensive verification strategies for Arm M-Class CPU memory system
- Constructing UVM testbenches for CPU memsys functional verification
- Developing and improving stimulus, test cases, testbench checkers and System Verilog assertions
- Debugging regression failures in simulation and formal and report bugs in the design under test
- Defining and implementing functional and statistical coverage and improving the testbench for coverage closure

Arm, Inc. — Chandler, AZ
CPU Verification Engineer Intern — May 2022 - Aug 2022

- Migrated event/trace-based verification workflow from A class CPU to M class CPU
- Captured memory system RTL signal and compiled the signal into linked events
- Traced memory transaction events, and visualized them in an intuitive manner for easier debugging

Arm, Inc. — Chandler, AZ
CPU Verification Engineer Intern — May 2021 - Aug 2021

- Optimized run-time performance of interrupt controller testbench
- Identified performance bottleneck and enhanced UVM testbench resource utilization
- Collaborated and Improved workflow efficiency by reducing testbench runtime overhead by 25%

RESEARCH EXPERIENCE

University of Wisconsin - Madison: Photonics lab — Apr 2019 - May 2021

- Contributed to a research group developing an ML-based magnetic levitation system.
- Collaborated on embedded system data acquisition and digital signal processing.
- Enhanced control system and circuitry, achieving a 10x reduction in response time overhead.

TECHNICAL SKILLS

Programming Skills	Verilog / SystemVerilog, Python, C / C++, Java, MATLAB
EDA Tools	QuestaSim / Visualizer, QuestaFormal, Quartus, Vivado, DVT, Verdi
Computer Skills	Linux, Git, VS Code, Jira, Jenkins