



1. Description

1.1. Project

Project Name	RAK3172
Board Name	custom
Generated with:	STM32CubeMX 6.4.0
Date	01/12/2022

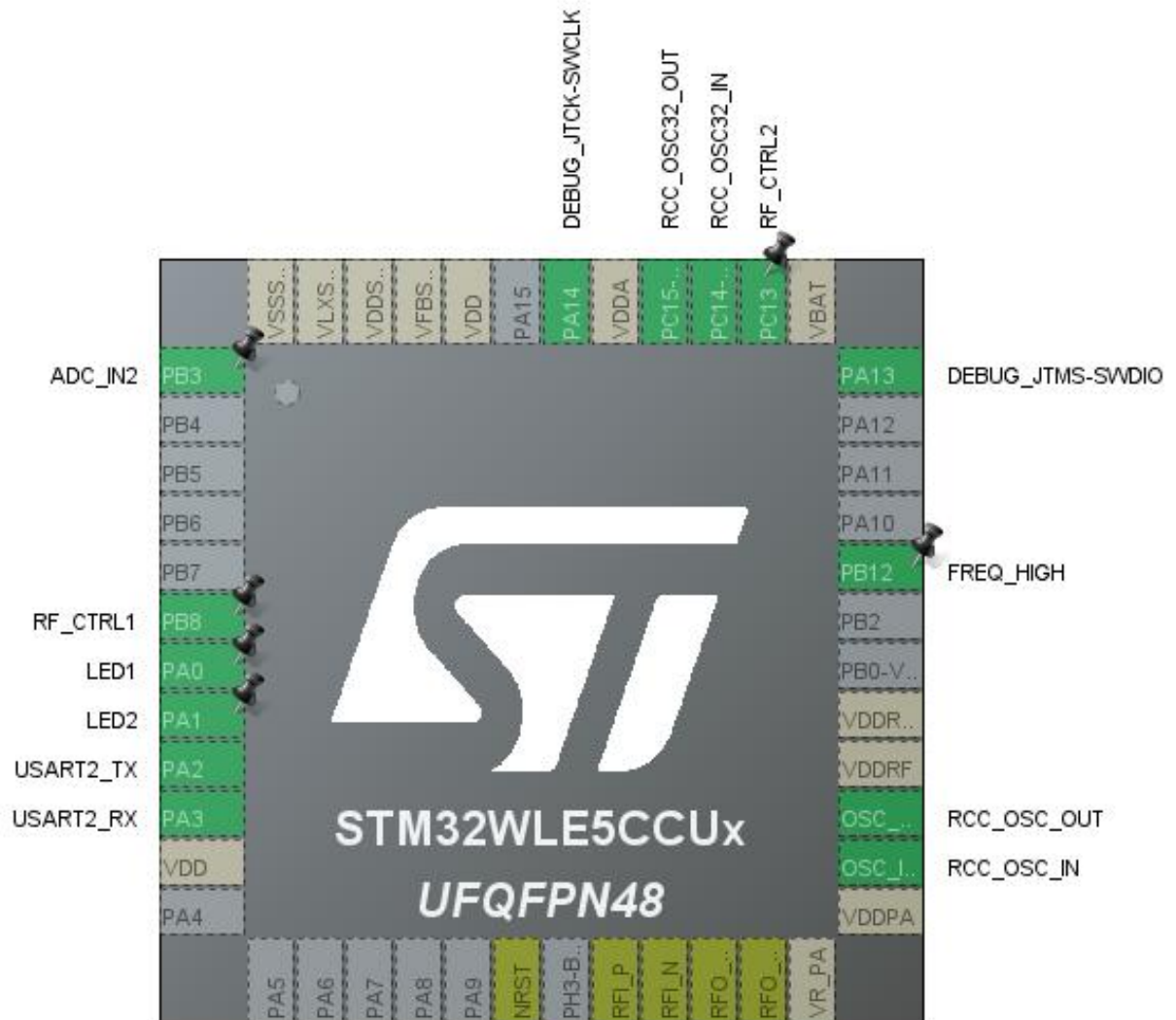
1.2. MCU

MCU Series	STM32WL
MCU Line	STM32WLEx
MCU name	STM32WLE5CCUx
MCU Package	UFQFPN48
MCU Pin number	48

1.3. Core(s) information

Core(s)	ARM Cortex-M4
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2. Pinout Configuration

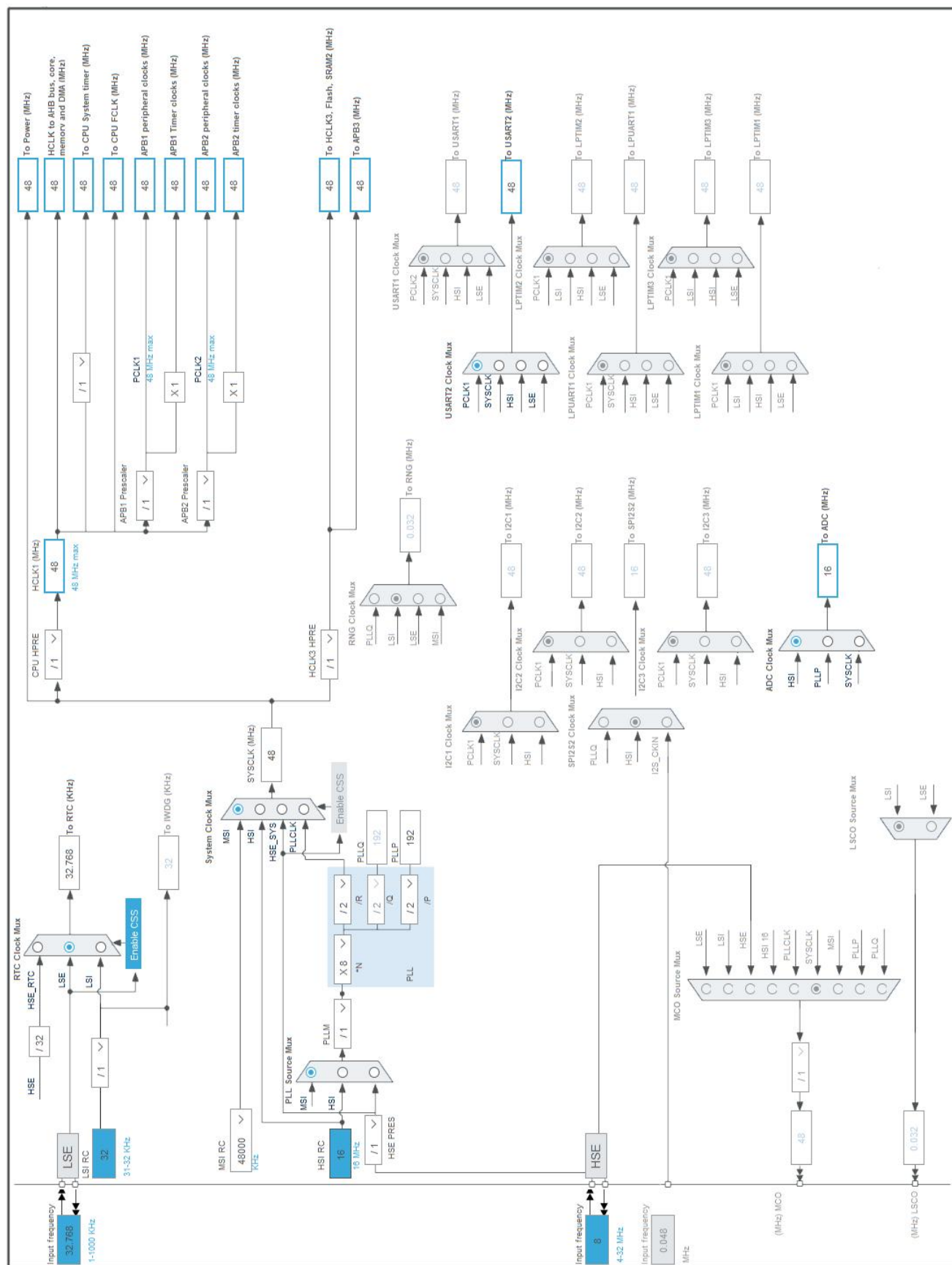


3. Pins Configuration

Pin Number UFQFPN48	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	PB3	I/O	ADC_IN2	
6	PB8 *	I/O	GPIO_Output	RF_CTRL1
7	PA0 *	I/O	GPIO_Output	LED1
8	PA1 *	I/O	GPIO_Output	LED2
9	PA2	I/O	USART2_TX	
10	PA3	I/O	USART2_RX	
11	VDD	Power		
18	NRST	Reset		
20	RFI_P	MonoIO		
21	RFI_N	MonoIO		
22	RFO_LP	MonoIO		
23	RFO_HP	MonoIO		
24	VR_PA	Power		
25	VDDPA	Power		
26	OSC_IN	MonoIO	RCC_OSC_IN	
27	OSC_OUT	MonoIO	RCC_OSC_OUT	
28	VDDRF	Power		
29	VDDRF1V55	Power		
32	PB12 *	I/O	GPIO_Input	FREQ_HIGH
36	PA13	I/O	DEBUG_JTMS-SWDIO	
37	VBAT	Power		
38	PC13 *	I/O	GPIO_Output	RF_CTRL2
39	PC14-OSC32_IN	I/O	RCC_OSC32_IN	
40	PC15-OSC32_OUT	I/O	RCC_OSC32_OUT	
41	VDDA	Power		
42	PA14	I/O	DEBUG_JTCK-SWCLK	
44	VDD	Power		
45	VFBSMPS	Power		
46	VDDSMPS	Power		
47	VLXSMPS	Power		
48	VSSMPS	Power		

* The pin is affected with an I/O function

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value
Project Name	RAK3172
Project Folder	C:\Users\danam\STM32CubeIDE\workspace_1.7.0\RAK3172
Toolchain / IDE	STM32CubeIDE
Firmware Package Name and Version	STM32Cube FW_WL V1.1.0
Application Structure	Advanced
Generate Under Root	Yes
Do not generate the main()	No
Minimum Heap Size	0x200
Minimum Stack Size	0x400

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	Yes
Backup previously generated files when re-generating	Yes
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No
Enable Full Assert	No

5.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	SystemClock_Config	RCC
2	MX_GPIO_Init	GPIO
3	MX_ADC_Init	ADC
4	MX_RTC_Init	RTC
5	MX_SUBGHZ_Init	SUBGHZ
6	MX_USART2_UART_Init	USART2
7	MX_DMA_Init	DMA
8	MX_LoRaWAN_Init	LORAWAN

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32WL
Line	STM32WLEx
MCU	STM32WLE5CCUx
Datasheet	DS13105_Rev7

6.2. Parameter Selection

Temperature	25
Vdd	3.0

6.3. Battery Selection

Battery	Li-SOCL2(AAA700)
Capacity	700.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.6 V
Max Cont Current	10.0 mA
Max Pulse Current	30.0 mA
Cells in series	1
Cells in parallel	1

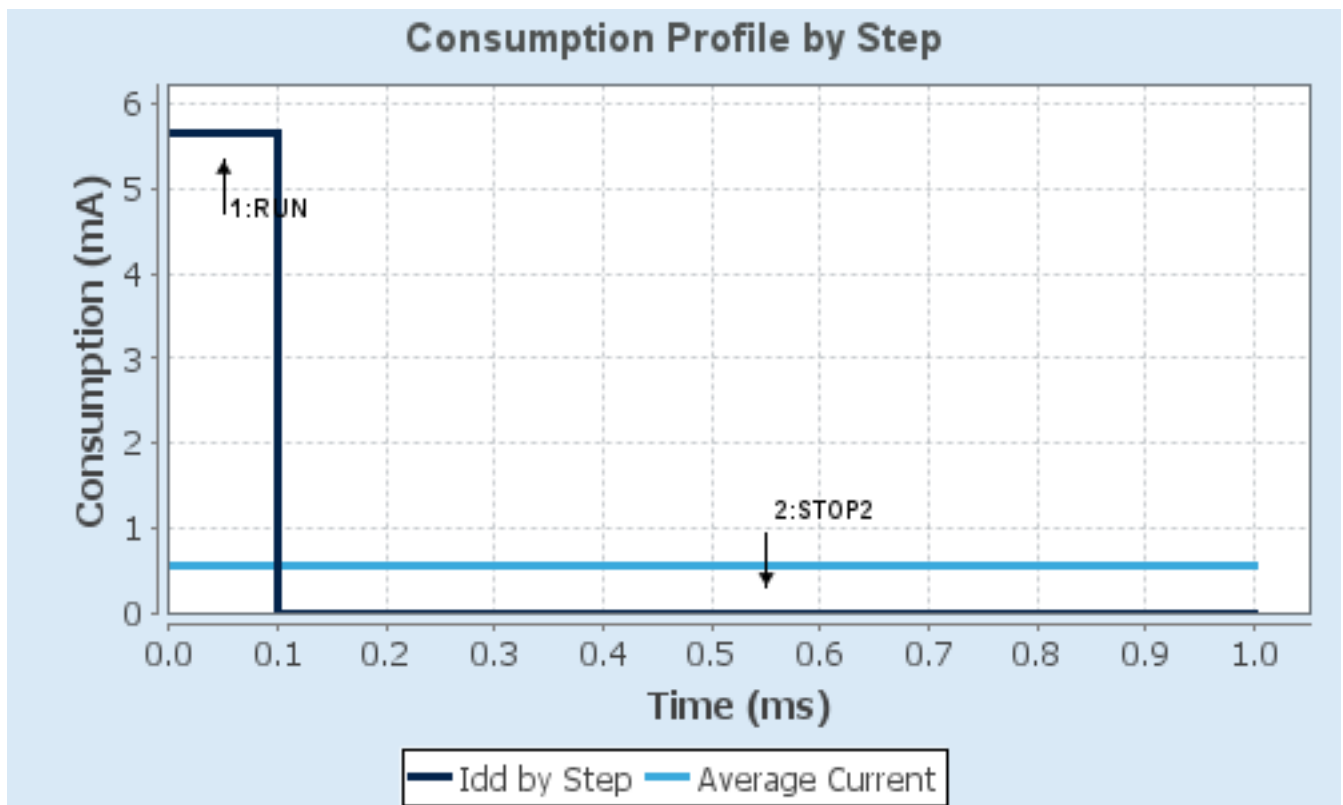
6.4. Sequence

Step	Step1	Step2
Mode	RUN	STOP2
Vdd	3.0	3.0
Voltage Source	Battery	Battery
Range	Range1-Medium/SMPS-OFF	NoRange
Fetch Type	SRAM1	NA
CPU Frequency	48 MHz	0 Hz
Clock Configuration	MSI	ALL CLOCKS OFF
Clock Source Frequency	48 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	5.65 mA	885 nA
Duration	0.1 ms	0.9 ms
DMIPS	60.0	0.0
Ta Max	124.53	125
Category	In DS Table	In DS Table

6.5. Results

Sequence Time	1 ms	Average Current	565.8 μ A
Battery Life	1 month, 21 days, 1 hour	Average DMIPS	60.0 DMIPS

6.6. Chart



7. Peripherals and Middlewares Configuration

7.1. ADC

mode: IN2

mode: Vrefint Channel

7.1.1. Parameter Settings:

ADC_Settings:

Clock Prescaler

Resolution

Calibration

Data Alignment

Scan Conversion Mode

End Of Conversion Selection

Low Power Auto Wait

Auto Off

Continuous Conversion Mode

Discontinuous Conversion Mode

External Trigger Conversion Source

External Trigger Conversion Edge

DMA Continuous Requests

Overrun behaviour

Sequencer

SamplingTime Common 1

SamplingTime Common 2

Oversampling Mode

Trigger Frequency

ADC_Regular_ConversionMode:

Enable Regular Conversions

Asynchronous clock mode divided by 64 *

ADC 12-bit resolution

Disable

Right alignment

Disabled

End of single conversion

Disabled

Disabled

Disabled

Disabled

Regular Conversion launched by software

None

Disabled

Overrun data preserved

Sequencer set to fully configurable

160.5 Cycles *

160.5 Cycles *

Disabled

High frequency

Disable

7.2. ADV_TRACE

mode: Enabled

7.3. DEBUG

JTAG and Trace: Serial Wire

7.4. MISC

mode: misc

7.5. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

Low Speed Clock (LSE) : Crystal/Ceramic Resonator

7.5.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Instruction Cache	Enabled
Prefetch Buffer	Disabled
Data Cache	Enabled
Flash Latency(WS)	2 WS (3 CPU cycle)

RCC Parameters:

HSI Calibration Value	64
MSI Calibration Value	0
MSI Auto Calibration	Enabled
HSE Startup Timeout Value (ms)	100
LSE Startup Timeout Value (ms)	5000
LSE Drive Capability	LSE oscillator low drive capability

Power Parameters:

Power Regulator Voltage Scale	Power Regulator Voltage Scale 1
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7.6. RTC

mode: Activate Clock Source

mode: Activate Calendar

Alarm A: Internal Alarm A

7.6.1. Parameter Settings:

General:

Asynchronous Predivider value

Bin Mode

SSRU Underflow Interrupt

Alarm A:

Free running 32 bit value

Binary AutoControl

Free running 32 bit mask

RTC_PREDIV_A *

Free running Binary mode *

Enabled

0

RTC_ALARMSUBSECONDBIN_AUTOCLR_NO *

SS[31:0] are compared and must match to activate alarm.

7.7. SEQUENCER

mode: Enabled

7.8. SUBGHZ

mode: Activated

7.8.1. Parameter Settings:

Baudrate Prescaler Value **4 ***

7.9. SYS

Timebase Source: None

7.10. TIMER

mode: Enabled

7.11. TINY_LPM

mode: Enabled

7.12. USART2

Mode: Asynchronous

7.12.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable
ClockPrescaler	1
Fifo Mode	Enable *
Txfifo Threshold	1 eighth full configuration

Rxfifo Threshold 1 eighth full configuration

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

7.13. LORAWAN

mode: Enabled

7.13.1. LoRaWAN application:

Application selection:

Application

Application configuration recommendations

End Node skeleton *

!! Please read carefully Information panel below!!

board settings:

Board Resources

None

Send Tx on Timer or Button Evt

TX_ON_TIMER

lora_app:

Active region

LORAMAC_REGION_US915 *

Transmission duty cycle

10000

Application user port

2

Switch class port

3

Default class

CLASS_A

Default handler message state

Unconfirmed message

Handler Adaptive Data Rate

On

Default activation type

OTAA

Default Unicast ping slots periodicity

4

sys_conf:

Trace verbose level

VLEVEL_M

Enable Application Logging

true

Activate Debugger

false

Disable Low Power Mode

false

7.13.2. LoRaWAN commissioning:

Commissioning:

Public network true

Current network ID 0

se-identity:

Static Device EUI true *

LoRaWAN device EUI AC, 1F, 09, FF, FE, 05, 36, A8 *

App/Join EUI 01, 01, 01, 01, 01, 01, 01, 01

Application key 88,BC,B4,59,7C,EA,42,E7,C0,4
D,8D,EB,4E,E7,2B,9C *

Network key 78,BC,B4,59,7C,EA,42,E7,C0,4
D,8D,EB,4E,E7,2B,9C *

Static Device Address false

Network session key 2B,7E,15,16,28,AE,D2,A6,AB,F7,15,88,0
9,CF,4F,3C

Application session key 2B,7E,15,16,28,AE,D2,A6,AB,F7,15,88,0
9,CF,4F,3C

lorawan_conf:

Enable Key read access true

7.13.3. LoRaWAN middleware:

lorawan_conf:

Region(s) selection please select the desired region(s) in the list below

Region Asia freq: 923 false

Region Australia freq: 915 false

Region China freq: 470 false

Region China freq: 779 false

Region Europe freq: 433 false

Region Europe freq: 868 true

Region Korea freq: 920 false

Region India freq: 865 false

Region USA freq: 915 true

Region Russia freq: 864 false

Enable Hybrid mode false

Enable LoRaMAC ClassB false

radio_conf:

Radio maximum wakeup time (in ms) 1

Probes Lines in Platform Settings false

radio_board_if:

Select radio Driver

Bsp via extSettings *

mw_log_conf:

Enable Middleware log

true

7.13.4. Platform Settings:

RTC

RTC

ADC

ADC

USART

USART2

*** User modified value**

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC	PB3	ADC_IN2	Analog mode	No pull-up and no pull-down	n/a	
DEBUG	PA13	DEBUG_JTMS-SWDIO	n/a	n/a	n/a	
	PA14	DEBUG_JTCK-SWCLK	n/a	n/a	n/a	
RCC	OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	
	OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
	PC14-OSC32_IN	RCC_OSC32_IN	n/a	n/a	n/a	
	PC15-OSC32_OUT	RCC_OSC32_OUT	n/a	n/a	n/a	
USART2	PA2	USART2_TX	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
	PA3	USART2_RX	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
GPIO	PB8	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	RF_CTRL1
	PA0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	High *	LED1
	PA1	GPIO_Output	Output Push Pull	No pull-up and no pull-down	High *	LED2
	PB12	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	FREQ_HIGH
	PC13	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	RF_CTRL2

8.2. DMA configuration

DMA request	Stream	Direction	Priority
USART2_TX	DMA1_Channel1	Memory To Peripheral	Low

USART2_TX: DMA1_Channel1 DMA request Settings:

Mode: Normal
Peripheral Increment: Disable
Memory Increment: **Enable ***
Peripheral Data Width: Byte
Memory Data Width: Byte

8.3. NVIC configuration

8.3.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Prefetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
RTC Tamper, RTC TimeStamp, LSECSS and RTC SSRU Interrupts	true	0	0
DMA1 Channel 1 Interrupt	true	2	0
USART2 Interrupt	true	2	0
RTC Alarms (A and B) Interrupt	true	0	0
SUBGHZ Radio Interrupt	true	0	0
PVD and PVM detector	unused		
FLASH (CFI) global Interrupt	unused		
RCC Interrupt	unused		
ADC Interrupt	unused		

8.3.2. NVIC Code generation

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Prefetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	true	false
Debug monitor	false	true	false
Pendable request for system service	false	true	false
System tick timer	false	true	false
RTC Tamper, RTC TimeStamp, LSECSS and RTC SSRU Interrupts	false	true	true
DMA1 Channel 1 Interrupt	false	true	true
USART2 Interrupt	false	true	true
RTC Alarms (A and B) Interrupt	false	true	true

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
SUBGHZ Radio Interrupt	false	true	true

* User modified value

9. System Views

9.1. Category view

9.1.1. Current

Middleware									
LORAWAN									
System Core	Analog	Timers	Connectivity	Multimedia	Security	Computing	Trace and Debug	Power and Thermal	Utilities
DMA	ADC	RTC	SUBGHZ				DEBUG		ADV_TRACE
GPIO			USART2						MISC
IIVIC									SEQUENCER
RCC									TIMER
SYS									TINY_LPM

10. Docs & Resources

Type	Link
Datasheet	http://www.st.com/resource/en/datasheet/DM00648230.pdf
Reference manual	http://www.st.com/resource/en/reference_manual/DM00530369.pdf
Programming manual	http://www.st.com/resource/en/programming_manual/DM00046982.pdf
Programming manual	http://www.st.com/resource/en/programming_manual/DM00104451.pdf
Errata sheet	http://www.st.com/resource/en/errata_sheet/DM00660735.pdf
Application note	http://www.st.com/resource/en/application_note/CD00167594.pdf
Application note	http://www.st.com/resource/en/application_note/CD00211314.pdf
Application note	http://www.st.com/resource/en/application_note/CD00259245.pdf
Application note	http://www.st.com/resource/en/application_note/CD00264342.pdf
Application note	http://www.st.com/resource/en/application_note/DM00073742.pdf
Application note	http://www.st.com/resource/en/application_note/DM00081379.pdf
Application note	http://www.st.com/resource/en/application_note/DM00160482.pdf
Application note	http://www.st.com/resource/en/application_note/DM00220769.pdf
Application note	http://www.st.com/resource/en/application_note/DM00226326.pdf
Application note	http://www.st.com/resource/en/application_note/DM00236305.pdf
Application note	http://www.st.com/resource/en/application_note/DM00257177.pdf
Application note	http://www.st.com/resource/en/application_note/DM00311483.pdf
Application note	http://www.st.com/resource/en/application_note/DM00315319.pdf
Application note	http://www.st.com/resource/en/application_note/DM00380469.pdf
Application note	http://www.st.com/resource/en/application_note/DM00395696.pdf
Application note	http://www.st.com/resource/en/application_note/DM00403796.pdf
Application note	http://www.st.com/resource/en/application_note/DM00493651.pdf
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Application note http://www.st.com/resource/en/application_note/DM00690797.pdf
Application note http://www.st.com/resource/en/application_note/DM00725181.pdf
Application note http://www.st.com/resource/en/application_note/DM00739353.pdf