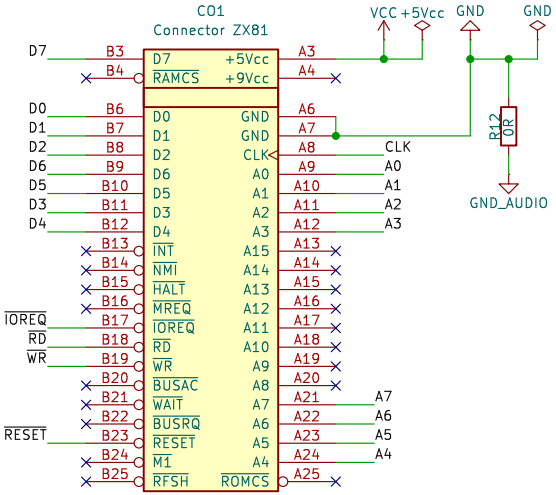
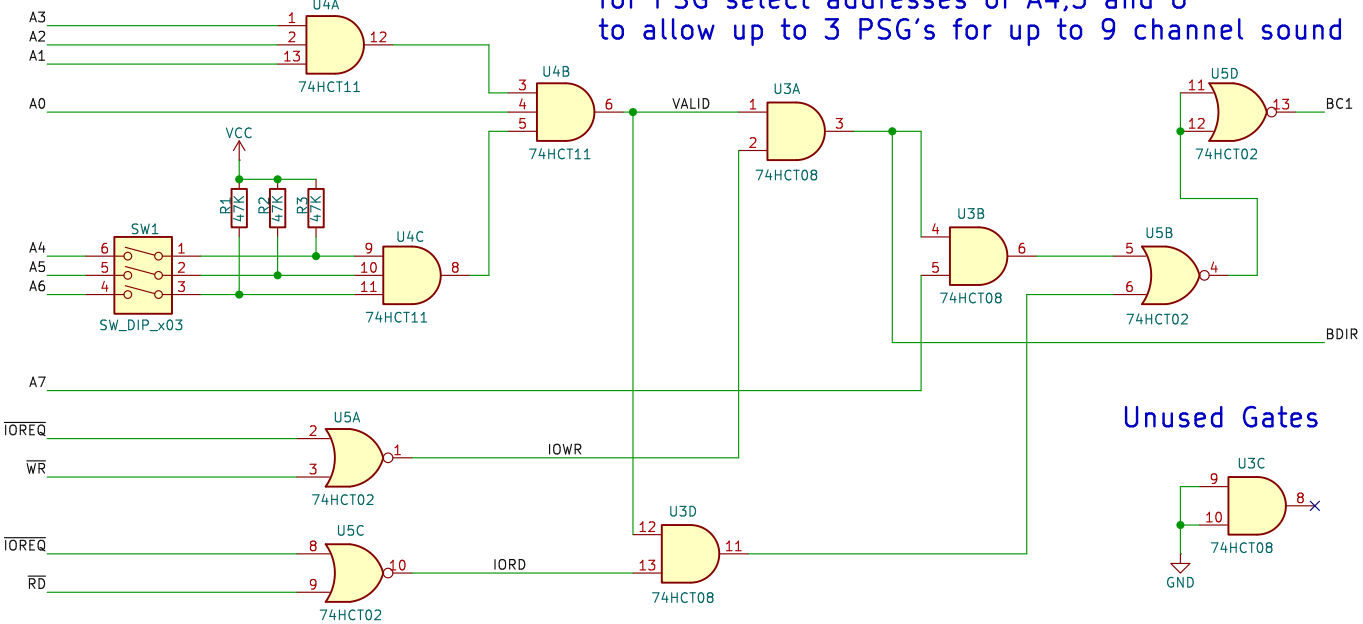
ZX81 Edge Connector

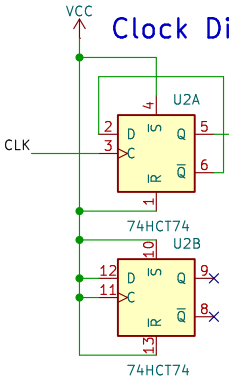


Address Decoding with DIP Switch Options for PSG select addresses of A4,5 and 6 to allow up to 3 PSG's for up to 9 channel sound



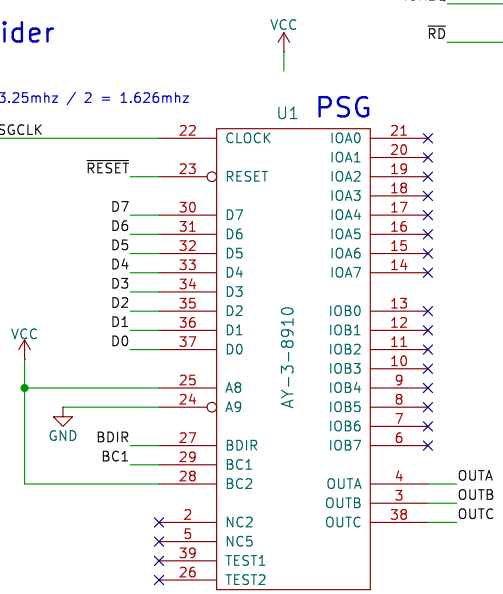
Unused Gates

Clock Divider

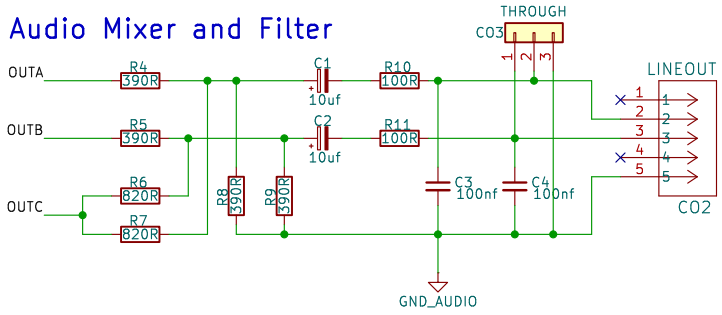


3.25mhz / 2 = 1.626mhz

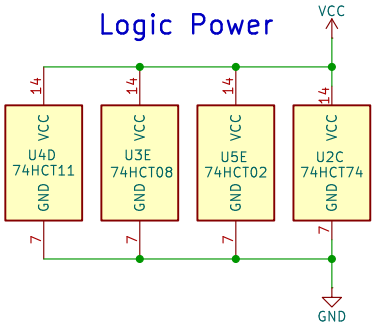
PSG



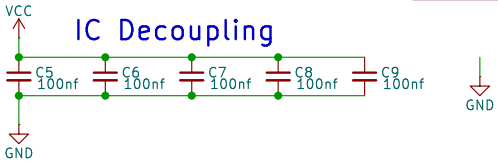
Audio Mixer and Filter



Logic Power



IC Decoupling



BDIR	BC1			
0	0			INACTIVE
0	1	/IORD	XX0FH	READ PSG
1	0	/IOWR	XX0FH	WRITE PSG
1	1	/IOWR	XXDFH	LATCH ADDRESS

XX0FH = 0FH = 00001111
XXDFH = DFH = 10001111

Channel A is Left
Channel B is right
Channel C (normaly noise) is mixed

Sheet: /
File: JONZON-X-81.kicad_sch

Title: JONZON-X-81

Size: A4	Date: 2025-08-01	**Rev: 1.0**
KiCad E.D.A. 9.0.3		Id: 1/1