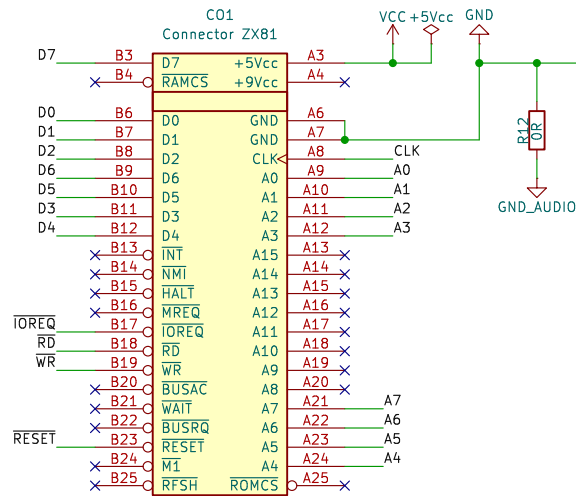
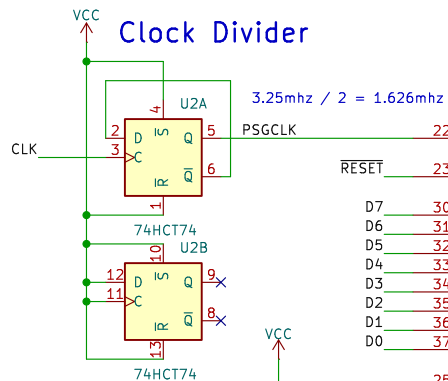


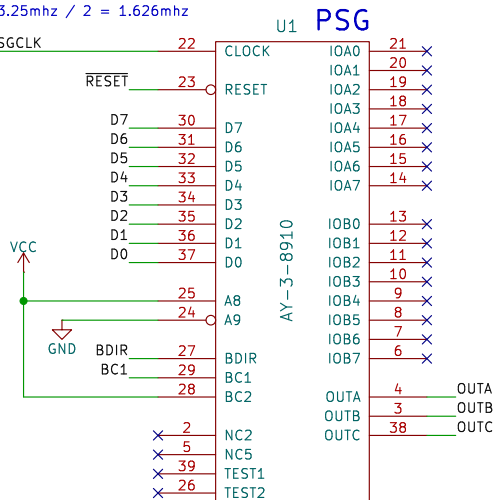
ZX81 Edge Connector



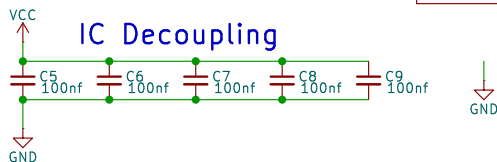
Clock Divider



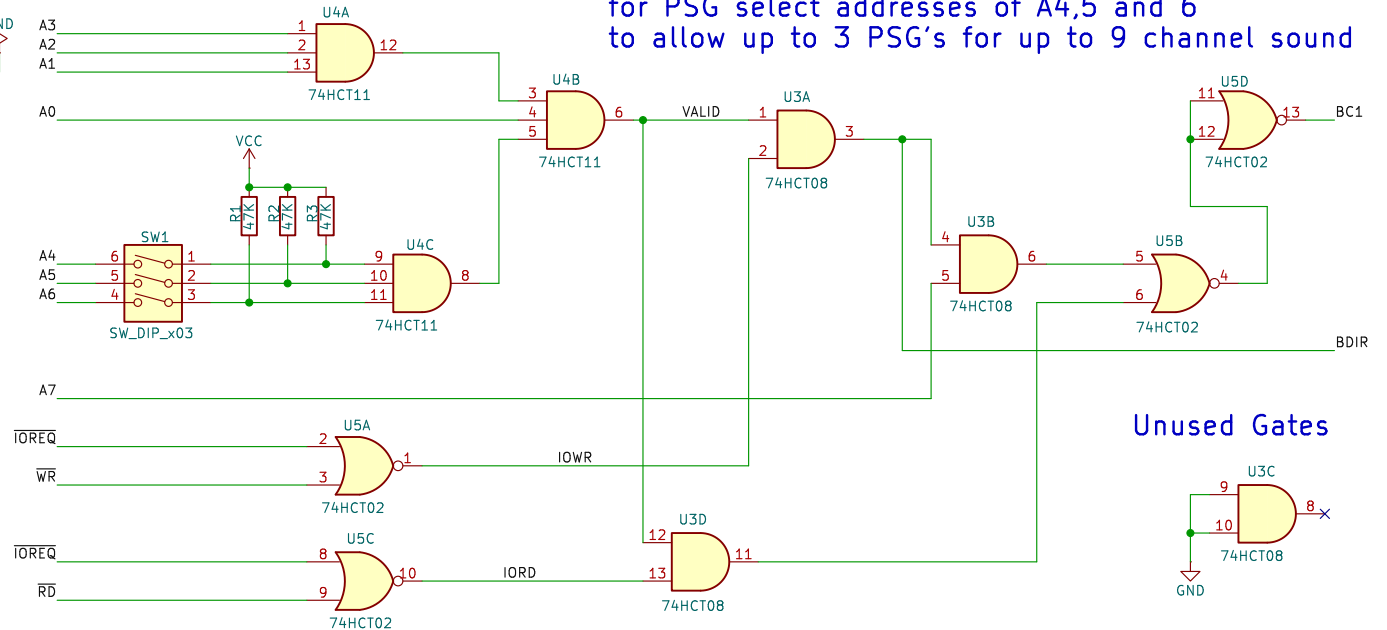
PSG



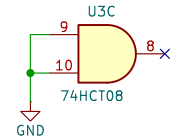
IC Decoupling



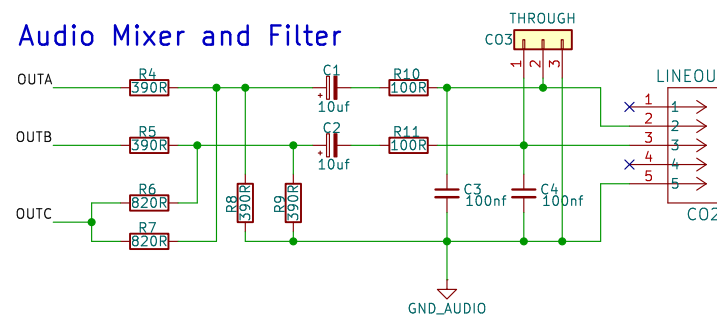
Address Decoding with DIP Switch Options
for PSG select addresses of A4,5 and 6
to allow up to 3 PSG's for up to 9 channel sound



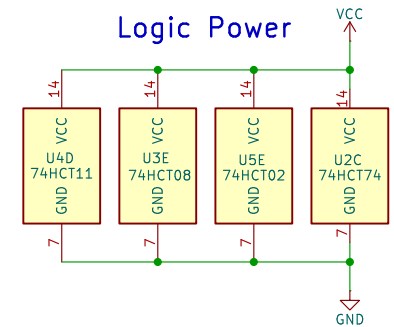
Unused Gates



Audio Mixer and Filter



Logic Power



Channel A is Left	BDR	BC1		
Channel B is right	0	0		INACTIVE
Channel C (normally noise) is mixed	0	1	/IORB	READ PSB
	1	0	/IORW	WRITE PSB
	1	1	/IOWR	LATCH ADDRESS
				XX0FH = 0FH = 00001111
				XXDFH = DFH = 10001111

Sheet: /
File: JONZON-X-81.kicad_sch

Title: JONZON-X-81

Size: A4	Date: 2025-08-01
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Rev: 1.0

Id: 1/1