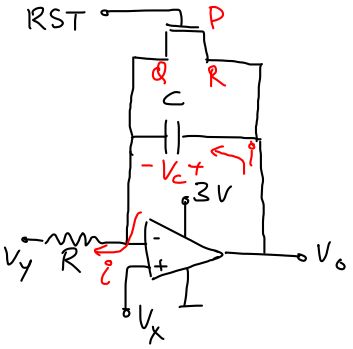
* ramp only occurs when RST is 0. While f_{RST} = 1 kHz, the ramp exists for ~0.9ms (from counter output screen shot)



* input goes 0.25 to 2.75 V
  ⇒ ramp must cover this range.
  lets go a bit wider to account for component tolerances etc : 0.2 V to 2.8 V
* slope of ramp : (2.8-0.2)/0.9ms = 2.9 V/ms

* with V_x fixed, for V_o to increase over time (slope>0), current must flow in indicated direction

* $i = \frac{C dV_c}{dt} = C\frac{d}{dt}(V_o - V_x) = C\frac{dV_o}{dt}$ → ramp slope

* $i = \frac{V_x - V_y}{R}$

* @ RST, $V_c = 0 \Rightarrow V_o = V_x$ (start of the ramp, chosen to be 0.2 V)

* $C\frac{dV_o}{dt} = \frac{V_x - V_y}{R} \Rightarrow 2900 = \frac{V_x - V_y}{RC}$

$$2900 = \frac{0.2 - V_y}{RC}$$

→ $V_y = 0$ is easy to make, we already have it @ opamp supply.

$$RC = 0.2/2900 = 68.97\ \mu s$$

* R dissipates $\frac{(V_x - V_y)^2}{R}$ ⇒ use large R
* breadboards have several pF parasitics, so chose C > 100pF
* ceramic capacitors more accurate than electrolytic which are typically used for high capacitances (μF & higher)
* large C will take longer to discharge through FET resistance.
* several RC combinations with these constraints will work!
* my choice: V_x = 0.2V, V_y = 0, R = 6.8 kΩ, C = 10 nF
* for nFET, ① clearly gate.
  @ Reset, V3 (the ramp = 2.8 V) > V2 (= V_x = 0.2 V)
  ∴ 3 is drain & 2 is source