Rev A to Rev A2 (skipped A1)

Page 9 – corrected Path to include FPGA, corrected file name LedBlinkingDSpeed.v(hd)

Future\FPGA\Microsemi\CreativeBoard\IGLOO2\Source then into either the **VHDL** or **verilog** folder.

Double click the top file: **LedBlickingDSpeed.v(hd)**

Page 12 – appended file extension to LedBlinkingDSpeed.io.pdc

Select the **LedBlinkingDSpeed.io.pdc** file.

Page 13 - appended file extension to LedBlinkingDSpeed.io.sdc

Select the **LedBlinkingDSpeed_sdc.sdc** file.

Page 15 – added clarity to the sentence.

At the bottom of the top-left window you will find several tabs with the following titles:

Page 16 - corrected file name LedBlinkingDSpeed.v(hd)

Verify that the file titled **LedBlinkingDSpeed.v(hd)** is the Bold File, …

Page 20 – corrected typo to file extension and added clarity to following sentence.

<DesignTop>.srr was .ssr -> is .srr

In the clock summary section of this report, … changed *the* to *this*

Page 22 – corrected location of the *Close* Button.

Click the **Close** button in the lower right.

Page 24 – corrected description of the Transcript Window. From *Tab* to *Window.*

The Transcript Window shows a list of all the tasks that were run via the .do file.

Page 27 – added the and button to the sentence.

Click the **Edit with I/O Editor** button and the window will grey …

Page 28 - added button & and to the sentences.

Click on the **Edit with Constraints Editor** button, and then click **Edit Place and Route Constraints.**

Like before, the window will grey out, the logo will briefly appear, and then the …