

Glen Muthoka Mutinda

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Bananz0

Professional Summary

Final-year Electrical & Electronics Engineering student at the University of Southampton with specialization in PCB design, FPGA development, and embedded systems. Proven expertise in hardware design across multiple domains including signal processing, IC physical implementation, and real-time system integration. Proficient in VHDL and SystemVerilog for FPGA development and embedded C/C++ for firmware. Experience with industrial EDA tools (Cadence, Mentor Calibre, Altera Quartus) and open-source PCB design platforms (KiCad, Eagle). Demonstrated ability to deliver complete hardware solutions from schematic capture through PCB fabrication and system integration. Seeking graduate opportunities in hardware design, FPGA development, and PCB design within defence and aerospace sectors.

Education

University of Southampton

Southampton, UK

BEng Electrical & Electronics Engineering (Expected First Class Honours)

2023–2026

Key Modules: Digital Systems Design, Integrated Circuit Design, Control Systems, Embedded Systems, Network Security, Signal Processing

Second Year Project: TSMC 65nm Ring Oscillator for Real-Time Clock IC (Team Lead)

Final Year Project: AI-Driven Optical Authentication Framework using Optical PUFs

ONCAMPUS Global

Southampton, UK

Undergraduate Foundation Programme, Engineering Pathway (Distinction)

2022–2023

Professional Experience

ARTEMIS Small Sat-1 Lunar CubeSat Project

University of Southampton

Junior Software Engineer

Sep 2023–Jun 2025

- Developed and optimized flight software in C/C++ for lunar mission CubeSat, reducing system latency by 6% through algorithm optimization and code refactoring
- Enhanced system reliability by 20% through implementation of comprehensive unit testing frameworks and automated debugging procedures
- Collaborated with multidisciplinary team of 8 engineers following NASA coding standards and MISRA C guidelines
- Implemented real-time telemetry processing system with strict timing constraints

Technical Projects

Hardware Design & PCB Development

TSMC 65nm Real-Time Clock Design: Ring Oscillator IC Fabrication: Sep 2023–Jun 2024

Role: Team Lead (6-member team) | **Tools:** S-Edit (Schematic), L-Edit (Layout), T-Spice (Simulation), Calibre DRC/LVS


Led complete integrated circuit design workflow from RTL to GDSII tape-out for TSMC 65nm process. Performed schematic capture and full custom layout design for Ring Oscillator real-time clock chip. Conducted comprehensive physical verification including Design Rule Checking and Layout vs. Schematic validation. Successfully submitted GDSII files for fabrication with zero DRC violations. Achieved 15% area reduction through custom cell optimization and strategic floorplanning. Extensive SPICE simulations for frequency stability and timing verification.

16-Stage FIR Notch Filter for Real-Time Audio on FPGA: Nov 2024–Dec 2024

Platform: Altera Cyclone V (DE1-SoC) FPGA | **Language:** SystemVerilog (VHDL-equivalent) | **Tools:** Quartus Prime, ModelSim


Designed parametrized Finite Impulse Response digital filter with notch filtering capabilities for real-time stereo

audio processing on FPGA. Implemented 4-state FSM controller achieving 19-cycle latency (950ns at 50MHz) from ADC input to DAC output. Successfully processed dual-channel 48kHz audio with -40dB notch depth. Synthesized design utilized 2,847 logic elements (5% FPGA utilization). Demonstrates practical signal processing algorithm implementation on FPGA hardware.

 github.com/Bananz0/16-Stage-FIR-Notch-Filter

WattsApp: Embedded Smart System Management Platform: Jan 2025–Mar 2025

MCU: AVR ATmega644p Microcontroller | **Stack:** Embedded C, InfluxDB, Grafana | **Protocols:** UART, I2C
Designed embedded system management platform for real-time monitoring and control on AVR microcontroller. Developed bare-metal C firmware implementing sensor polling, data acquisition, and serial communication protocols. Integrated time-series database and visualization dashboards for live system monitoring. Achieved sub-millisecond response times with interrupt-driven architecture. Experience with microcontroller selection, peripheral integration, and firmware optimization.

 github.com/Bananz0/WattsApp

AI-Driven Optical Authentication Framework: Sep 2025–Jun 2026

Tools: Python, NumPy, CuPy (CUDA), Scipy, Matplotlib


Developing novel anti-counterfeiting security framework leveraging Optical Physical Unclonable Functions (OPUFs) for hardware authentication. Designed machine learning pipelines for spectral data analysis with statistical feature extraction. Engineered GPU-accelerated data processing for high-dimensional emission spectra. Developed robust quantization algorithm to convert analog spectral features into cryptographic-strength bitstreams for secure hardware identification.

Digital Design & Signal Processing

MIPSquare++: 5-Stage Pipelined MIPS Processor Simulator: Apr 2025–Jun 2025

Language: C++ (C++23) | **Tools:** CMake, CLion

Developed comprehensive MIPS CPU simulator implementing realistic 5-stage pipeline architecture (Fetch, Decode, Execute, Memory, Write-Back) with full hazard detection and mitigation. Implemented custom MIPS assembly parser supporting R-type, I-type, and J-type instructions. Engineered intelligent data forwarding between pipeline stages to minimize stalls. Developed load-use hazard detection with automatic pipeline stalling and branch hazard handling. Achieved near 1 CPI with proper forwarding implementation.


 github.com/Bananz0/MIPSquare

Software Development & Tools

SmartSync Lighting: AI-Driven Smart Home Automation: Dec 2024–Present

Language: Python | **Libraries:** OpenCV, Spotify API, python-kasa


Engineered automated lighting system synchronizing TP-Link smart bulbs with Spotify playback. Implemented computer vision algorithms using OpenCV for real-time album artwork analysis. System processes and updates lighting in <200ms for seamless synchronization.

 github.com/Bananz0/SmartSync-Lighting

ControlCraft: Interactive Control Systems Analysis Toolbox: Nov 2024–Dec 2024

Platform: MATLAB GUI (App Designer)

Built comprehensive educational tool for control systems analysis and design. Implemented interactive PID controller tuning with real-time visualization, automated stability analysis (Routh-Hurwitz, Nyquist), and frequency domain analysis. Successfully deployed in undergraduate labs serving 60+ students.

 github.com/Bananz0/ControlCraft

PiBoard: Real-Time Collaborative Whiteboard: Apr 2024–May 2024

Framework: Qt (C++) | **Platform:** Raspberry Pi


Developed collaborative whiteboard application with custom serial communication protocol. Implemented efficient data serialization for real-time synchronization. Achieved <100ms update latency through optimized protocol design.

 github.com/Bananz0/PiBoard

Galaxy Book Enabler: 2024–Present

Language: PowerShell | **Downloads:** 10,000+ | **Stars:** 350+

Developed professional-grade Windows tool with 21 authentic hardware profiles. Features registry manipulation, automatic elevation, and smart package management. Auto-update checker with System Support Engine integration.

 github.com/Bananz0/GalaxyBookEnabler

eGPU Auto-Enabler: 2024–Present

Language: PowerShell | **Technologies:** PnP Utilities, Power Management APIs

Created background service with automatic PnP device monitoring, custom power plan switching, and crash recovery. Achieved 99.9% reliability with <50ms detection latency.

 github.com/Bananz0/eGPUae

WinStream: Windows to AirPlay Audio Bridge: Jun 2024–Present

Language: C#/.NET | **Technologies:** Virtual Audio Drivers, AirPlay Protocol

Creating Windows application enabling system-wide audio streaming to AirPlay devices with virtual audio device driver and real-time encoding/transmission.

 github.com/Bananz0/WinStream

Somnus: Sleep Optimization Mobile Application: Jan 2025–Present

Platform: Android (Kotlin) | **APIs:** Health Connect, Google Fit, Samsung Health

Developing Android application for optimal wake time calculation using sleep cycle analysis and REM pattern detection.

 github.com/Bananz0/Somnus

Technical Skills

Hardware Design Languages.....

Proficient: SystemVerilog (VHDL-equivalent), Embedded C/C++

Competent: VHDL, Python, MATLAB

PCB Design & Schematic Capture.....

PCB Design Tools: KiCad (PCB layout, schematic capture), Eagle (circuit design), Fritzing (prototyping)

Industrial Platforms: Cadence S-Edit/L-Edit (IC schematic/layout), Mentor Calibre (DRC/LVS verification)

Expertise: Schematic capture, PCB layout, design rule checking, layout verification, footprint management

FPGA & Digital Design.....

Platforms: Altera Quartus Prime, Xilinx Vivado, TSMC 65nm Process Node

Simulation: ModelSim, LTSpice, T-Spice, NI Multisim, MATLAB Simulink/Simscape

Verification: Design Rule Checking (DRC), Layout vs. Schematic (LVS), SPICE Simulation, Synthesis Place & Route

Microcontroller Platforms.....

Development: Arduino (AVR/ARM), ESP32, Raspberry Pi, STM32, AVR ATmega644p

Interfaces: UART, I2C, SPI, GPIO

Firmware: Bare-metal development, interrupt-driven architecture, real-time systems

Software & Development Tools.....

Version Control: Git, GitHub, GitLab CI/CD

Scripting: Python (NumPy/SciPy), MATLAB, Bash, Tcl

IDEs: VS Code, CLion, Android Studio, Quartus, Vivado

Professional Memberships

2024–Present: Member, Institute of Electrical and Electronics Engineers (IEEE)

2024–Present: Member, Information Systems Audit and Control Association (ISACA)

2024–2026: Associate Member, Royal Aeronautical Society (AMRAeS)

Additional Information

Languages: English (Native), Swahili (Native), Spanish (Beginner - A1)

Right to Work: UK Student Visa (valid until 2026), eligible for Graduate Route visa