Glen Muthoka Mutinda

+44 7341 625286 • theglenmuthoka@gmail.com • glenmuthoka
Bananz0

Professional Summary

Final-year Electrical & Electronics Engineering student with practical experience in the complete IC design flow, from RTL to GDSII tape-out on the TSMC 65nm process node. Proficient in physical verification (DRC/LVS), timing analysis, and embedded systems development. Proven ability to lead technical teams and deliver high-reliability hardware/software systems, demonstrated through a successful CPU tape-out and flight software development for a lunar CubeSat. Seeking an internship at TSMC to contribute to advanced semiconductor manufacturing and design enablement.

Education

University of Southampton **Southampton, UK**
BEng Electrical & Electronics Engineering (Expected First Class Honours) *2023–2026*
Key Modules: Integrated Circuit Design, Digital Systems Design, Embedded Systems, Control Systems, Signal Processing
Second Year Project: TSMC 65nm IC Design & Fabrication (Team Lead) – *Achieved zero DRC violations*
Final Year Project: AI-Driven Optical Authentication Framework using Optical PUFs

Relevant Technical Projects

TSMC 65nm CPU Design: Complete IC Design & Fabrication Flow: Sep 2023–Jun 2024
Role: Team Lead | **Tools:** Cadence S-Edit, L-Edit, T-Spice, Mentor Calibre (DRC/LVS)
Led a 6-member team through the full custom IC design flow for a CPU on TSMC's 65nm process.

- Designed CPU datapath and control logic from schematic to layout.
- Performed extensive SPICE simulations to verify setup/hold times and critical path timing.
- Conducted full physical verification including Design Rule Checking (DRC) and Layout vs. Schematic (LVS) validation using Calibre.
- Successfully submitted GDSII files for fabrication with zero DRC violations.
- Optimized layout to achieve 15% area reduction through custom cell design and strategic floorplanning.

16-Stage FIR Notch Filter for Real-Time Audio on FPGA: Nov 2024–Dec 2024
Platform: Altera Cyclone V (DE1-SoC) | **Language:** SystemVerilog | **Tools:** Quartus Prime, ModelSim
Designed a parametrized FIR digital filter for real-time processing.

- Implemented a 4-state FSM controller achieving 19-cycle latency (950ns) from ADC to DAC.
- Synthesized design utilizing 2,847 logic elements (5% utilization) with verified timing closure.

AI-Driven Optical Authentication Framework: Sep 2025–Jun 2026
Role: Lead Researcher | **Tools:** Python, CUDA, NumPy
Developing a security framework using Optical Physical Unclonable Functions (OPUFs).

- Engineering GPU-accelerated data processing pipelines for high-dimensional spectral data.
- Developing quantization algorithms to convert analog spectral features into cryptographic bitstreams.

MIPSquare: MIPS Assembly Simulator: 2024
Language: C++ | **Focus:** Computer Architecture
Built a MIPS processor simulator implementing instruction decoding, register file management, and memory operations, demonstrating deep understanding of processor architecture.

Professional Experience

ARTEMIS Small Sat-1 Lunar CubeSat Project **University of Southampton**
Junior Software Engineer *Sep 2023–Jun 2025*

- Developed flight software in C/C++ for a lunar mission, adhering to strict reliability standards (MISRA C guidelines).
- Reduced system latency by 6% and enhanced reliability by 20% through rigorous unit testing and code refactoring.
- Collaborated in a multidisciplinary team to meet space-grade timing and safety requirements.

Technical Skills

IC Design & Hardware

IC Design: TSMC 65nm Process, Cadence S-Edit/L-Edit/T-Spice, Mentor Calibre (DRC/LVS), GDSII Tape-out, SPICE Simulation

Digital Design: SystemVerilog, VHDL, FPGA (Altera Quartus Prime, Xilinx Vivado), ModelSim, Timing Analysis

PCB Design: KiCad, Autodesk EAGLE

Programming & Embedded

Languages: C/C++, SystemVerilog, Python, MATLAB, Assembly (MIPS/ARM)

Embedded: ESP32, Raspberry Pi, RTOS concepts, I2C/SPI/UART protocols

Tools and Platforms

OS/DevOps: Linux (Ubuntu/Debian), Git, Docker, Bash Scripting

General: VS Code, MATLAB Simulink

Professional Memberships

2024–Present: Member, Institute of Electrical and Electronics Engineers (IEEE)