

# Glen Muthoka Mutinda

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Bananz0

## Professional Summary

Final-year Electrical & Electronics Engineering student at the University of Southampton with specialization in embedded systems, IC design, and digital implementation. Proven track record in physical implementation from RTL to GDSII tape-out on TSMC 65nm process. Experience spans hardware description languages (SystemVerilog), EDA tools (Cadence, Quartus, ModelSim), and scripting for design automation (Python, C/C++, MATLAB). Demonstrated ability to optimize for power and area while collaborating in multidisciplinary teams. Seeking graduate opportunities in physical implementation and digital design.

## Education

<b>University of Southampton</b> <i>BEng Electrical &amp; Electronics Engineering (Expected First Class Honours)</i>	<b>Southampton, UK</b> 2023–2026
<b>Key Modules:</b> Digital Systems Design, Integrated Circuit Design, Control Systems, Embedded Systems, Network Security, Signal Processing	
<b>Second Year Project:</b> TSMC 65nm Ring Oscillator for Real-Time Clock IC (Team Lead)	
<b>Final Year Project:</b> AI-Driven Optical Authentication Framework using Optical PUFs	
<b>ONCAMPUS Global</b> <i>Undergraduate Foundation Programme, Engineering Pathway (Distinction)</i>	<b>Southampton, UK</b> 2022–2023

## Professional Experience

<b>ARTEMIS Small Sat-1 Lunar CubeSat Project</b> <i>Junior Software Engineer</i>	<b>University of Southampton</b> Sep 2023–Jun 2025
○ Developed and optimized flight software in C/C++ for lunar mission CubeSat, reducing system latency by 6% through algorithm optimization and code refactoring ○ Enhanced system reliability by 20% through implementation of comprehensive unit testing frameworks and automated debugging procedures ○ Collaborated with multidisciplinary team of 8 engineers following NASA coding standards and MISRA C guidelines ○ Implemented real-time telemetry processing system with strict timing constraints	

## Technical Projects

### Hardware & Digital Design

**TSMC 65nm Real-Time Clock Design: Ring Oscillator IC Fabrication Flow:** Sep 2023–Jun 2024

**Role:** Team Lead (6-member team) | **Tools:** S-Edit, T-Spice, L-Edit, Calibre DRC/LVS

Led complete integrated circuit design from RTL to GDSII tape-out for TSMC 65nm process node. Designed and implemented Ring Oscillator circuit for real-time clock chip with extensive SPICE simulations for frequency stability and timing verification. Conducted full physical verification including Design Rule Checking and Layout vs. Schematic validation. Successfully submitted GDSII files for fabrication with zero DRC violations. Achieved 15% area reduction through custom cell optimization and strategic floorplanning.

**MIPSquare++: 5-Stage Pipelined MIPS Processor Simulator:** Apr 2025–Jun 2025

**Language:** C++ (C++23) | **Tools:** CMake, CLion

Developed comprehensive MIPS CPU simulator implementing realistic 5-stage pipeline architecture (Fetch, Decode, Execute, Memory, Write-Back) with full hazard detection and mitigation. Implemented custom MIPS assembly parser supporting R-type, I-type, and J-type instructions. Engineered intelligent data forwarding between EX/MEM and MEM/WB stages to minimize pipeline stalls. Developed load-use hazard detection with automatic pipeline stalling and branch hazard handling with pipeline flushing. Achieved near 1 CPI with proper forwarding

implementation.

[🔗](https://github.com/Bananz0/MIPSquare) [github.com/Bananz0/MIPSquare](https://github.com/Bananz0/MIPSquare)

### 16-Stage FIR Notch Filter for Real-Time Audio on FPGA: Nov 2024–Dec 2024

**Platform:** Altera Cyclone V (DE1-SoC) | **Language:** SystemVerilog | **Tools:** Quartus Prime, ModelSim

Designed parametrized Finite Impulse Response digital filter with notch filtering capabilities for real-time stereo audio processing. Implemented 4-state FSM controller achieving 19-cycle latency (950ns at 50MHz) from ADC input to DAC output. Successfully processed dual-channel 48kHz audio with -40dB notch depth. Synthesized design utilized 2,847 logic elements (5% FPGA utilization).

[🔗](https://github.com/Bananz0/16-Stage-FIR-Notch-Filter) [github.com/Bananz0/16-Stage-FIR-Notch-Filter](https://github.com/Bananz0/16-Stage-FIR-Notch-Filter)

### AI-Driven Optical Authentication Framework: Sep 2025–Jun 2026

**Tools:** Python, NumPy, CuPy (CUDA), Scipy, Matplotlib

Developing novel anti-counterfeiting security framework leveraging Optical Physical Unclonable Functions (OPUFs).

Designed machine learning pipelines for spectral data analysis with statistical feature extraction. Engineered GPU-accelerated data processing using CUDA/CuPy for high-dimensional emission spectra. Developed robust quantization algorithm to convert analog spectral features into cryptographic-strength bitstreams.

### WattsApp: Embedded Smart System Management Platform: Jan 2025–Mar 2025

**MCU:** AVR ATMega644p | **Stack:** Embedded C, InfluxDB, Grafana | **Protocols:** UART, I2C

Designed embedded system management platform for real-time monitoring and control on AVR ATMega644p microcontroller. Developed bare-metal C firmware implementing sensor polling, data acquisition, and serial communication. Integrated InfluxDB time-series database and Grafana dashboards for live system visualization. Achieved sub-millisecond response times with interrupt-driven architecture.

[🔗](https://github.com/Bananz0/WattsApp) [github.com/Bananz0/WattsApp](https://github.com/Bananz0/WattsApp)

## Software Development

### SmartSync Lighting: AI-Driven Smart Home Automation: Dec 2024–Present

**Language:** Python | **Libraries:** OpenCV, Spotify API, python-kasa

Engineered automated lighting system synchronizing TP-Link smart bulbs with Spotify playback. Implemented computer vision algorithms using OpenCV for real-time album artwork analysis and dominant color extraction. System processes and updates lighting in <200ms for seamless synchronization.

[🔗](https://github.com/Bananz0/SmartSync-Lighting) [github.com/Bananz0/SmartSync-Lighting](https://github.com/Bananz0/SmartSync-Lighting)

### ControlCraft: Interactive Control Systems Analysis Toolbox: Nov 2024–Dec 2024

**Platform:** MATLAB GUI (App Designer)

Built comprehensive educational tool for control systems analysis and design. Implemented interactive PID controller tuning with real-time step response visualization, automated stability analysis (Routh-Hurwitz, Nyquist), and frequency domain analysis. Successfully deployed in undergraduate control systems labs serving 60+ students.

[🔗](https://github.com/Bananz0/ControlCraft) [github.com/Bananz0/ControlCraft](https://github.com/Bananz0/ControlCraft)

### PiBoard: Real-Time Collaborative Whiteboard: Apr 2024–May 2024

**Framework:** Qt (C++) | **Platform:** Raspberry Pi

Developed collaborative whiteboard application with custom serial communication protocol over GPIO. Implemented efficient data serialization for real-time drawing synchronization between multiple Raspberry Pi devices. Achieved <100ms update latency through optimized protocol design and threading architecture.

[🔗](https://github.com/Bananz0/PiBoard) [github.com/Bananz0/PiBoard](https://github.com/Bananz0/PiBoard)

## Open Source & Personal Tools

### Galaxy Book Enabler: 2024–Present

**Language:** PowerShell | **Downloads:** 10,000+ | **Stars:** 350+

Developed professional-grade Windows tool that spoofs PCs as Samsung Galaxy Books, unlocking the Samsung ecosystem including Quick Share, Multi Control, Samsung Notes, and 20+ exclusive applications. Implemented 21 authentic Galaxy Book hardware profiles with registry manipulation, automatic elevation via gsudo, and smart package management through WinGet. Features auto-update checker, System Support Engine integration, and seamless migration between versions.

[🔗](https://github.com/Bananz0/GalaxyBookEnabler) [github.com/Bananz0/GalaxyBookEnabler](https://github.com/Bananz0/GalaxyBookEnabler)

**eGPU Auto-Enabler:** 2024–Present

**Language:** PowerShell | **Technologies:** PnP Utilities, Power Management APIs

Created background service that automatically re-enables external GPUs after hot-plugging on Windows. Implemented automatic PnP device monitoring with 2-second polling, custom power plan switching for optimal eGPU performance, and crash recovery with runtime state preservation. Features Windows toast notifications, 500KB rotating logs, and daily auto-update verification. Achieved 99.9% reliability with <50ms detection latency.

[🔗](https://github.com/Bananz0/eGPUae) [github.com/Bananz0/eGPUae](https://github.com/Bananz0/eGPUae)

**WinStream: Windows to AirPlay Audio Bridge:** Jun 2024–Present

**Language:** C#/.NET | **Technologies:** Virtual Audio Drivers, AirPlay Protocol

Creating Windows application enabling system-wide audio streaming to AirPlay devices. Implemented virtual audio device driver for transparent audio capture and developed real-time audio encoding/transmission using AirPlay 2 protocol specifications. Achieved <50ms latency for lip-sync compatibility.

[🔗](https://github.com/Bananz0/WinStream) [github.com/Bananz0/WinStream](https://github.com/Bananz0/WinStream)

**Somnus: Sleep Optimization Mobile Application:** Jan 2025–Present

**Platform:** Android (Kotlin) | **APIs:** Health Connect, Google Fit, Samsung Health

Developing Android application that calculates optimal wake times using sleep cycle analysis and REM pattern detection algorithms. Integrated with Android Health Connect module for unified access to multiple health platforms.

[🔗](https://github.com/Bananz0/Somnus) [github.com/Bananz0/Somnus](https://github.com/Bananz0/Somnus)

## Technical Skills

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### Programming & Hardware Description Languages.....

**Proficient:** SystemVerilog, C/C++, Python, MATLAB

**Competent:** C#, Kotlin, PowerShell, JavaScript

### Hardware Design & EDA Tools.....

**IC Design:** TSMC 65nm Process, Cadence S-Edit/L-Edit/T-Spice, Mentor Calibre (DRC/LVS), GDSII Tape-out

**FPGA/Digital:** Altera Quartus Prime, Xilinx Vivado, ModelSim, SystemVerilog

**Simulation:** LTSpice, NI Multisim, MATLAB Simulink/Simscape

**Platforms:** Arduino (AVR/ARM), ESP32, Raspberry Pi, STM32

### Software & Development Tools.....

**Version Control:** Git, GitHub, GitLab CI/CD

**Scripting:** Python (NumPy/SciPy), MATLAB, Bash, Tcl (basic)

**IDEs:** VS Code, CLion, Android Studio, Quartus, Vivado

## Professional Memberships

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**2024–Present:** Member, Institute of Electrical and Electronics Engineers (IEEE)

**2024–Present:** Member, Information Systems Audit and Control Association (ISACA)

**2024–2026:** Associate Member, Royal Aeronautical Society (AMRAeS)

## Additional Information

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**Languages:** English (Native), Swahili (Native), Spanish (Beginner - A1)

**Right to Work:** UK Student Visa (valid until 2026), eligible for Graduate Route visa