“Scalable Systolic Array Multiplier Optimized by Sparse Matrix”

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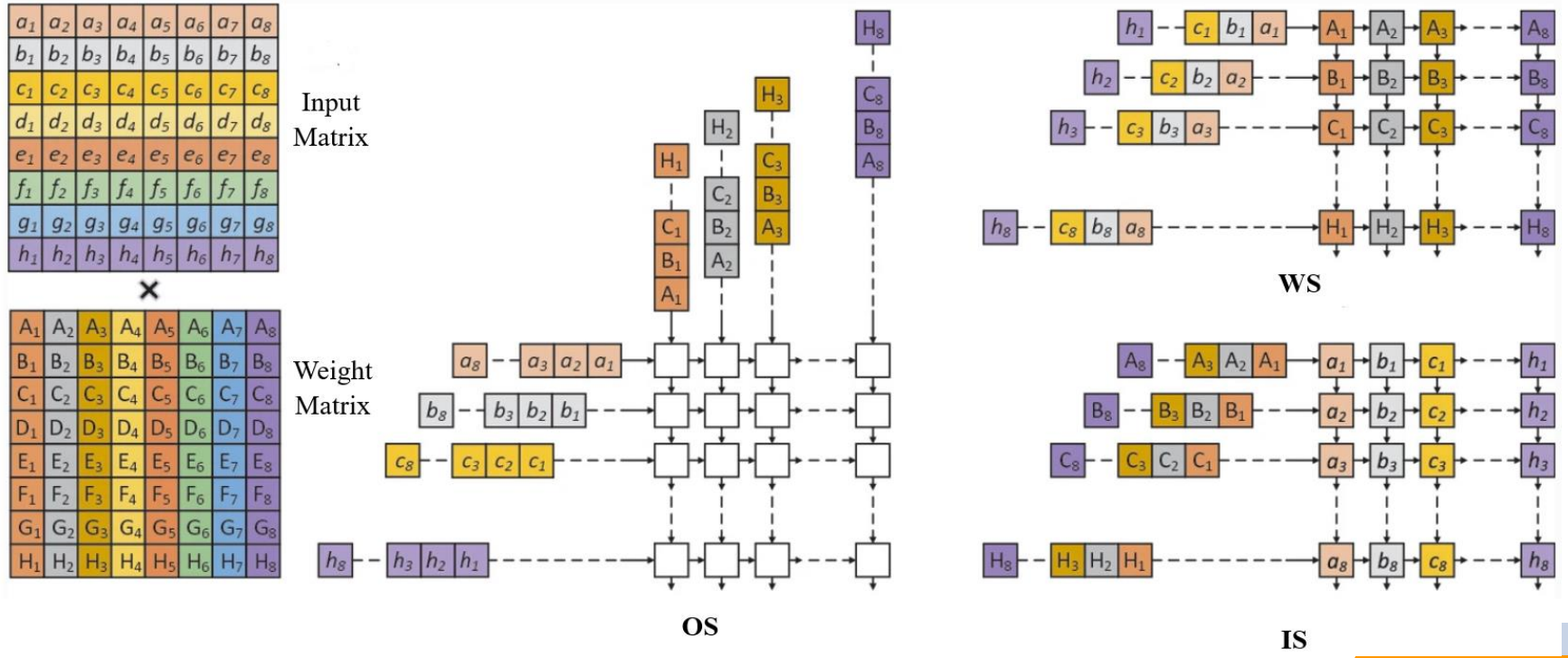
AGENDA

- Objective
- Introduction
- Application
- Paper Implementation & Simulation Results
- Proposed Method
- Implementation Results
- Future Work & Conclusion
- References

Objective

Sparse matrix multiplication optimized by scalable systolic array has been considered, which was compared with traditional systolic array for application in neural networks .

INTRODUCTION – SYSTOLIC ARRAY



Cont.

SPARSE MATRIX MULTIPLICATION

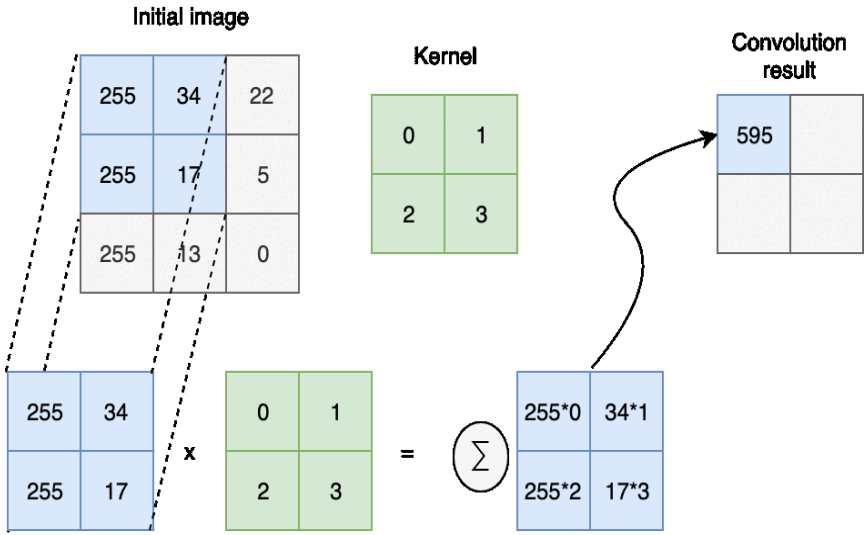
$$\begin{bmatrix} 0 & 0 & 3 & 0 & 4 \\ 0 & 0 & 5 & 7 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 2 & 6 & 0 & 0 \end{bmatrix}$$

Row	0	0	1	1	3	3
Column	2	4	2	3	1	2
Value	3	4	5	7	2	6

APPLICATION - CONVOLTUTION NEURAL NETWORK

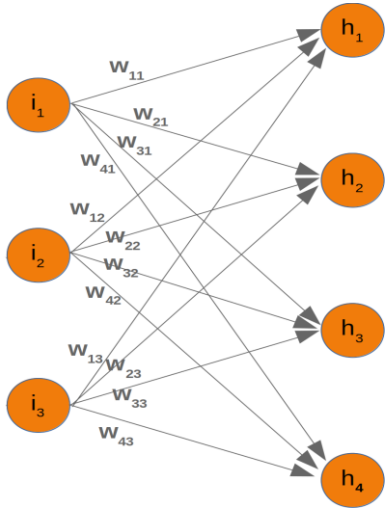
Convolution Layer

Process : Convolution

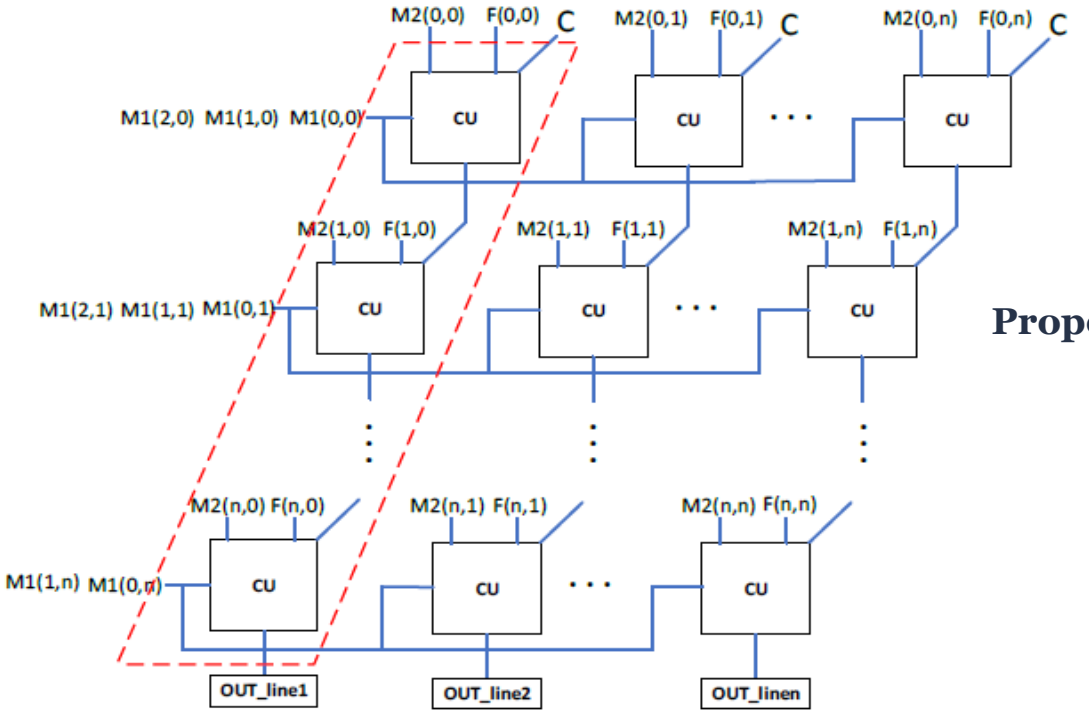


Fully-Connected Layer

Process : Matrix Multiplication

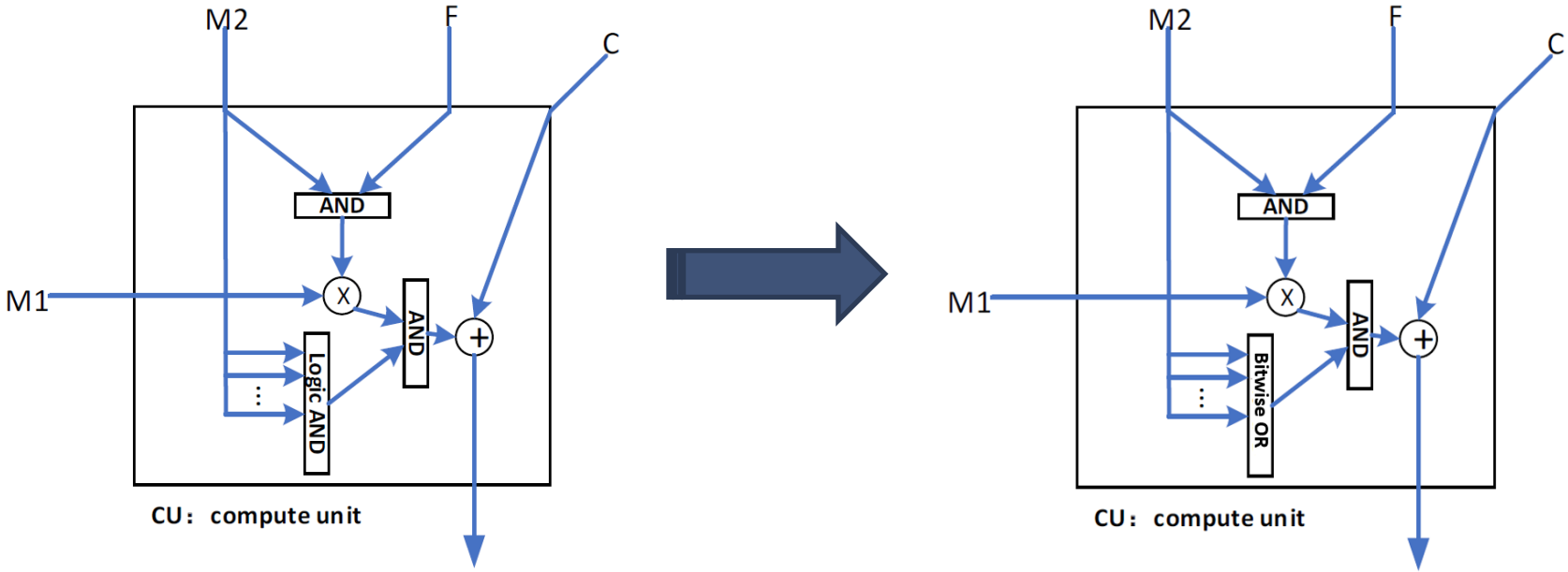


PAPER IMLEMENTATION

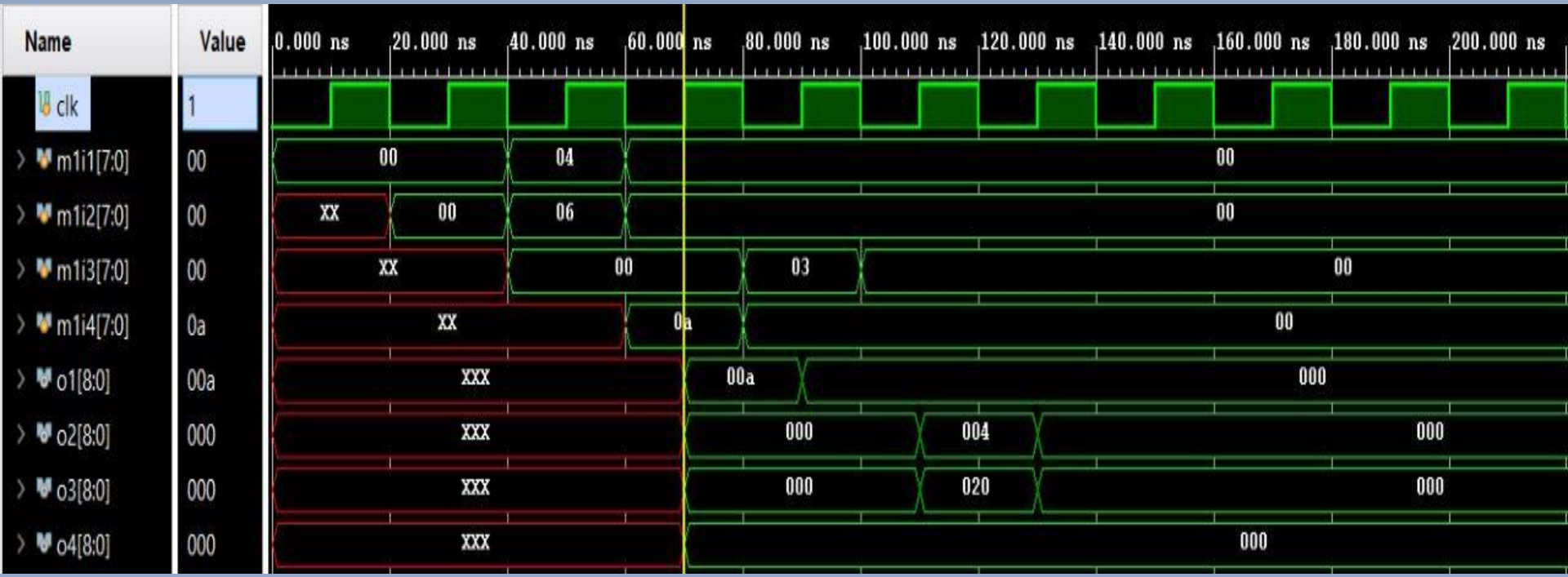


Proposed Systolic Array Circuit

Structure of Computation Unit



SIMULATION RESULTS



FPGA Results

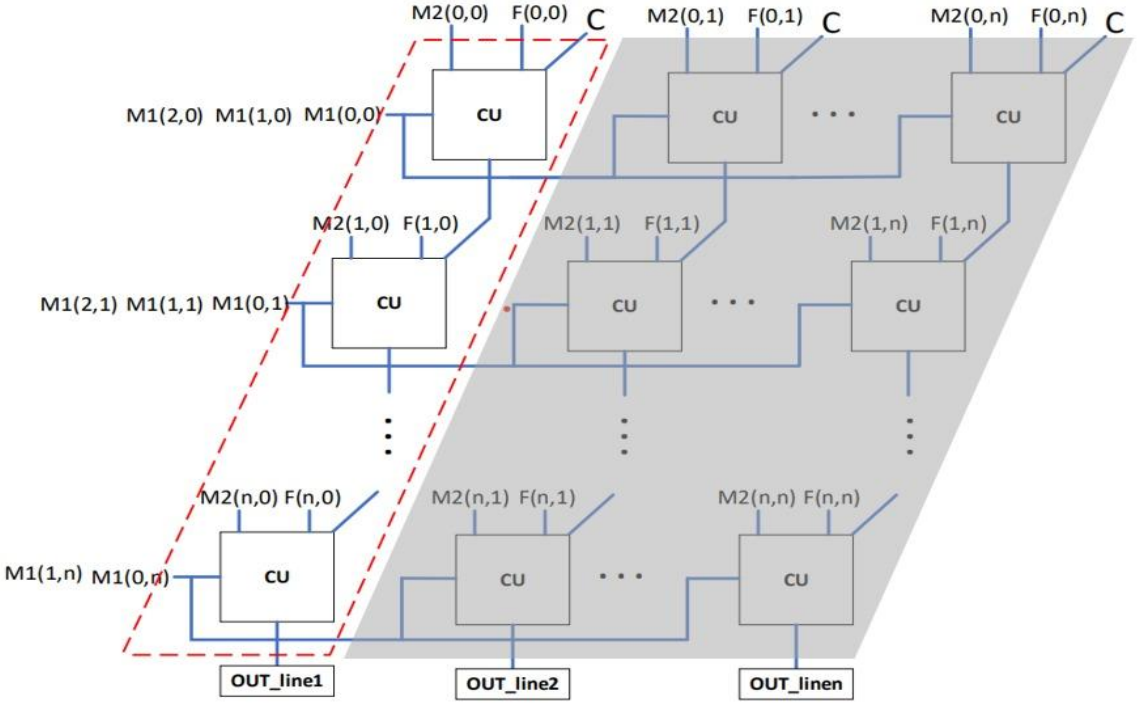
Multiplier Structure	Delay (ns)	LUT
Traditional systolic array	7.874	732
Optimized sparse matrix	6.827	658

ASIC Results

Multiplier Structure	Delay (ps)	AREA (um^2)
Traditional systolic array	4817	5187.146
Optimized sparse matrix	2767	4368.024

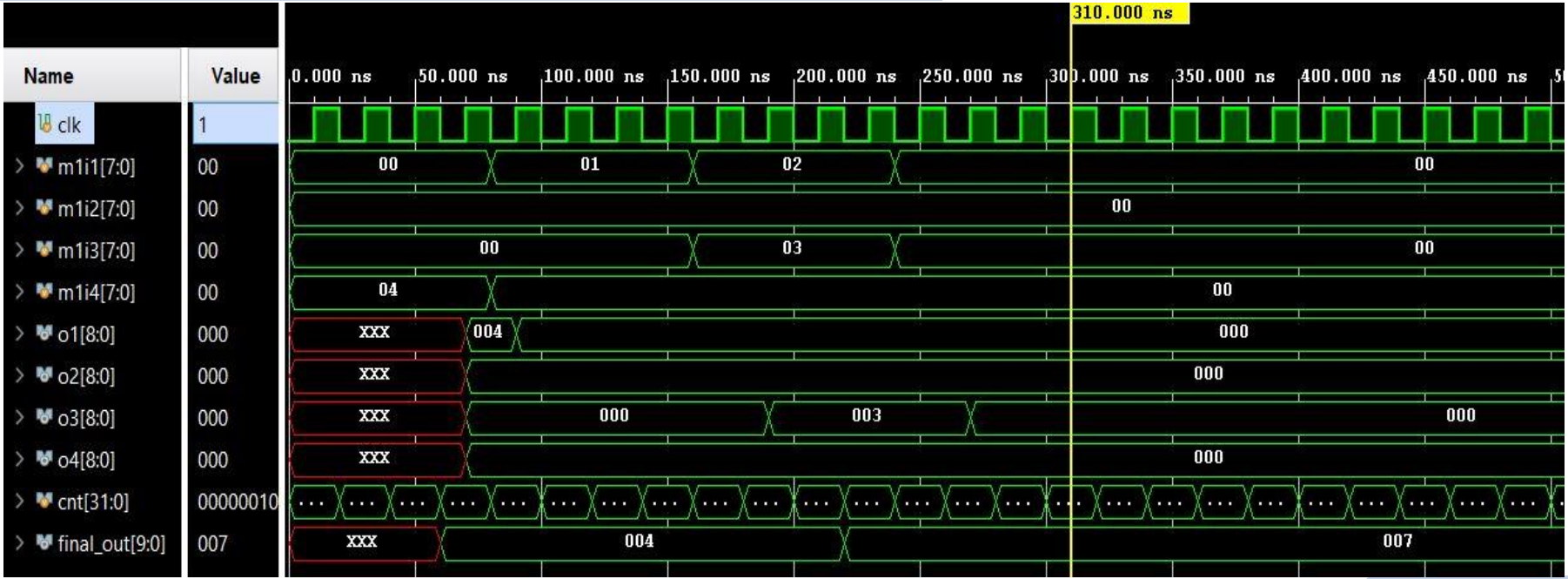
Convolution using Paper Implementation

Systolic Array Structure for Convolution

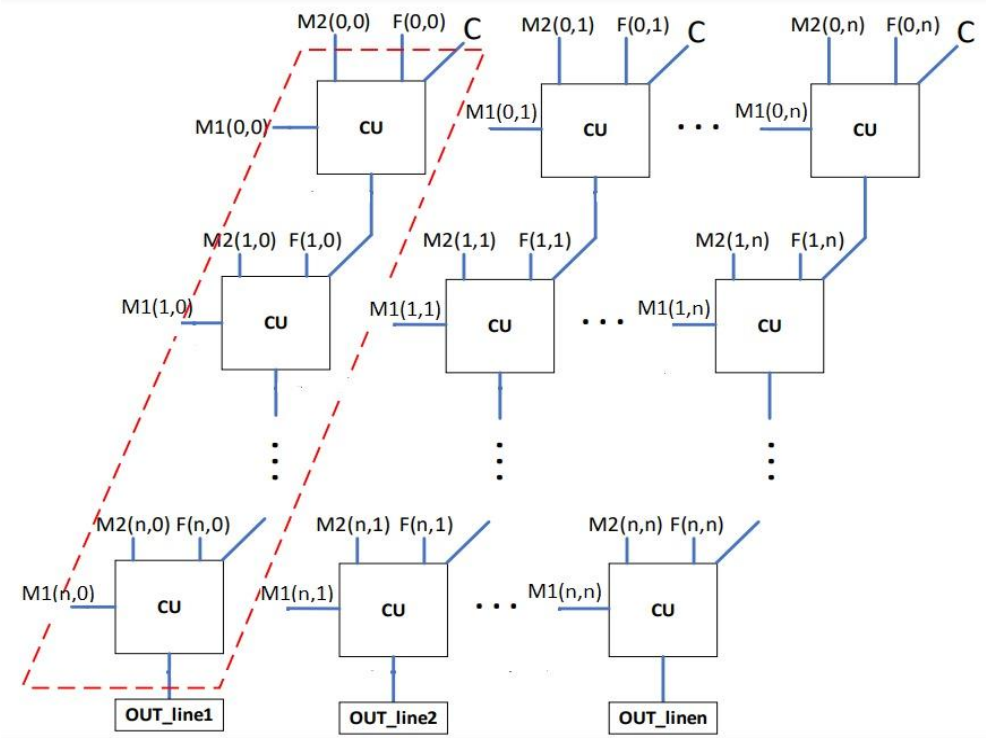


Simulation Results

N x N cycles

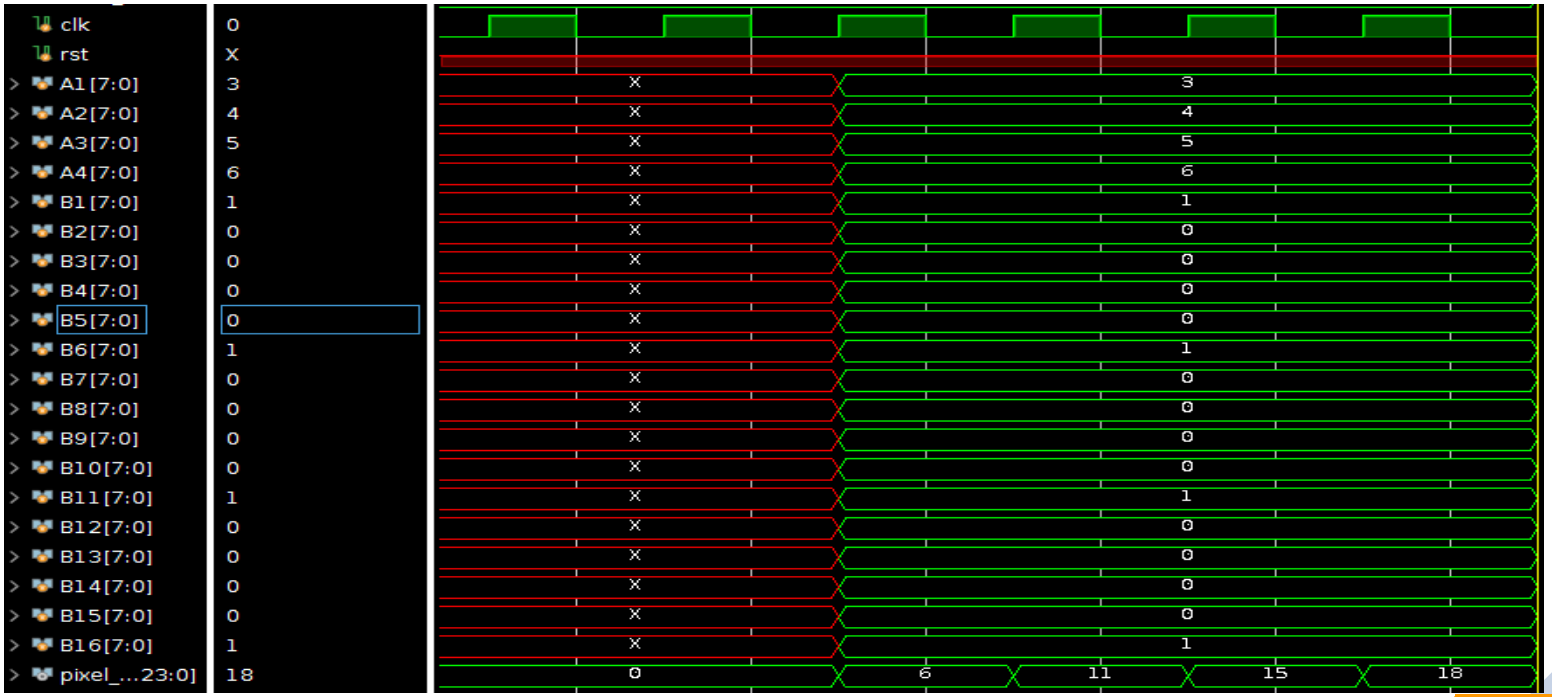


Proposed Method



Simulation Results

N cycles



Implementation Results

Original Image

Gaussian Image

FUTURE WORK

- Replace adders and multipliers with their efficient counterparts.
- Include Compressed Sparse Row.

CONCLUSION

- AND gate in paper is replaced by Bitwise OR to get required results.
- Convolution is also implemented with same architecture and a new one.
- Significant improvement in delay and number of clock cycles has been found with respect to traditional structure.

REFERENCES

[1] R. Jia, T. Xu and Y. Chang, "Scalable Systolic Array Multiplier Optimized by Sparse Matrix," *2021 IEEE 14th International Conference on ASIC (ASICON)*, Kunming, China, 2021, pp. 1-4, doi: 10.1109/ASICON52560.2021.9620326.

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thank you