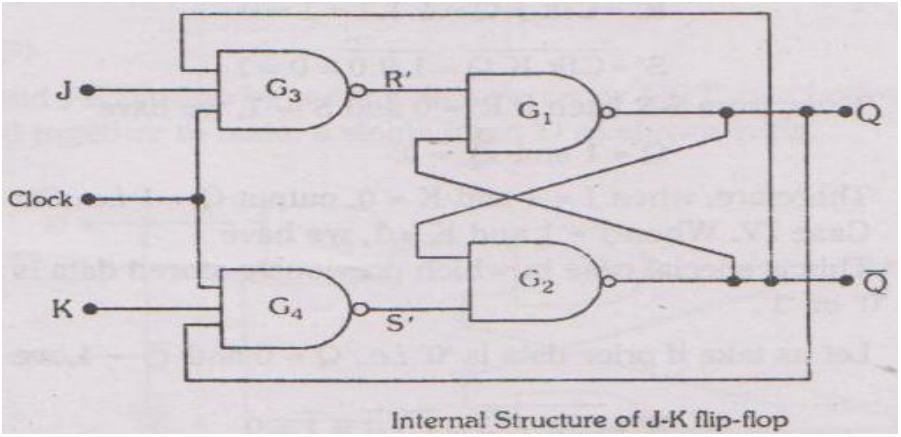
J.K Flip Flop

- The JK flip flop is the most versatile flip-flop, and the most commonly used flip flop
- when discrete devices are used to implement arbitrary state machines.
- It has no undefined states or race condition, however. It is always edge triggered;

$$R' = \overline{Clk.J.\bar{Q}}$$

$$S' = \overline{Clk.K.Q}$$



Internal Structure of J-K flip-flop

Case I : when J = 0 , K = 0

Output of gates **G3 and g4** are always ‘1’ irrespective of clock signal and the output feedbacks

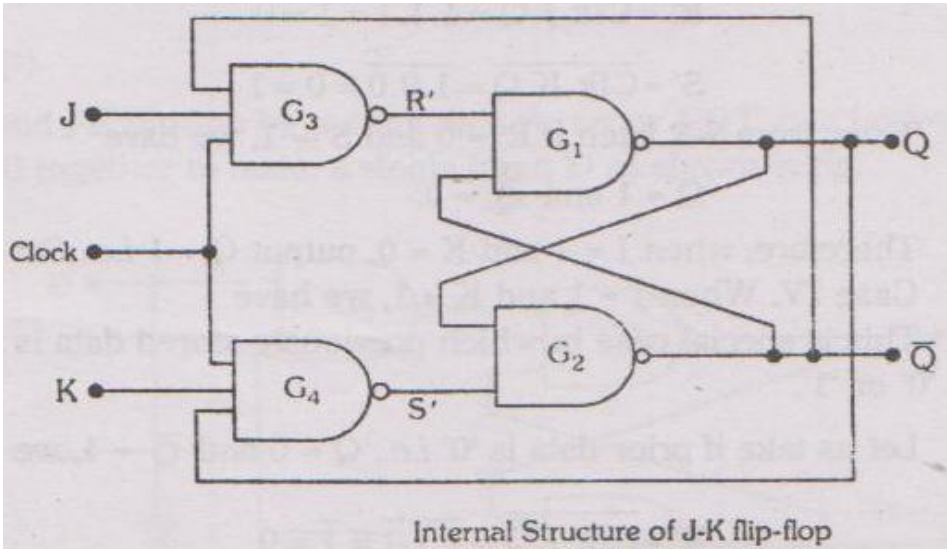
Thus ‘1’ is input to gates **G1 and g2** which provides the output for no change

- Output Q is no change

Inputs			Outputs		State	
Clk	J	K	Q	$\bar{Q}$		
↑	0	0	Q	$\bar{Q}$	No Change	
↑	0	1	0	1	Reset	Positive Edg
↑	1	0	1	0	Set	Triggered Cl
↑	1	1	$\bar{Q}$	Q	Toggle	
0	X	X	Q	$\bar{Q}$	No Change	
1	X	X	Q	$\bar{Q}$	No Change	Flip-flop is disabled
↓	X	X	Q	$\bar{Q}$	No Change	

$$R' = \overline{Clk.J.\bar{Q}} =$$

$$S' = \overline{Clk.K.Q} =$$



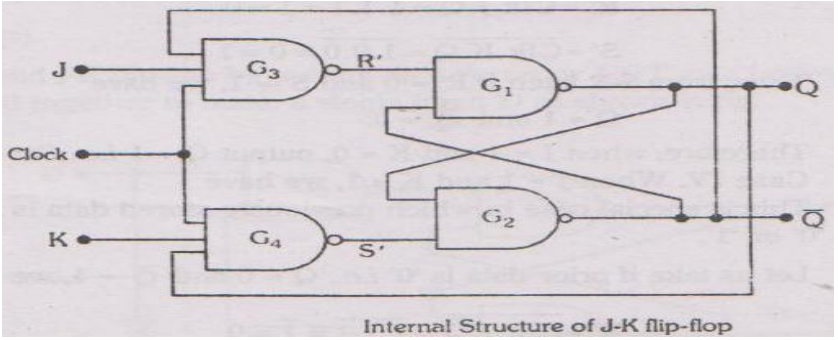
Internal Structure of J-K flip-flop

Case II : when J = 0 , K = 1

Output of gates **G3 is** always ‘1’ **and g4** is always ‘0’ it is clear from the expiration for R’ and S’

$$R' = \overline{Clk.J.\overline{Q}} =$$

$$S' = \overline{Clk.K.Q} =$$



Internal Structure of J-K flip-flop

If the previous state of Q and Q’ is given by Q =1 and Q’ = 0

$$R' = \overline{Clk.J.\overline{Q}} = \overline{1.0..0} = \overline{0} = 1$$

$$S' = \overline{Clk.K.Q} = \overline{1.1.1} = \overline{1} = 0$$

Thus the is input to gates **G1 and g2** are ‘1’ and ‘0’ respectively

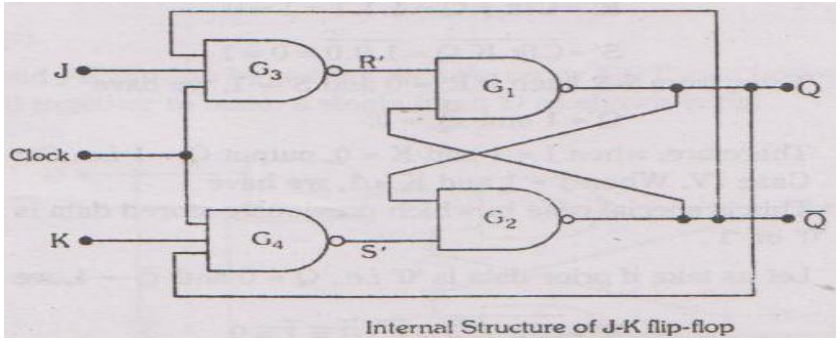
Therefore when J = 0 and K = 1, output Q = 0 Reset

Case III : when J = 1 , K = 0

Output of gates **G3 is** always ‘0’ **and g4** is always ‘1’ it is clear from the expiration for R’ and S’

$$R' = \overline{Clk.J.\bar{Q}} =$$

$$S' = \overline{Clk.K.Q} =$$



Internal Structure of J-K flip-flop

If the previous state of Q and Q’ is given by Q =0 and Q’ = 1

$$R' = \overline{Clk.J.\bar{Q}} = \overline{1.1.0} = \bar{0} = 0$$

$$S' = \overline{Clk.K.Q} = \overline{1.1.1} = \bar{1} = 1$$

Thus the is input to gates **G1 and g2** are ‘0’ and ‘1’ respectively

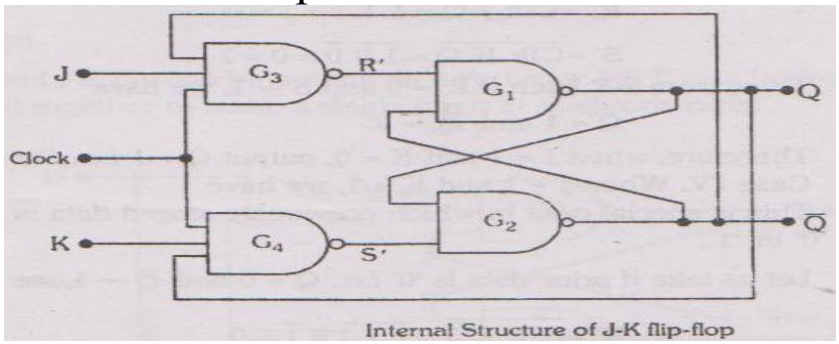
Therefore when J = 1 and K = 0, output Q = 1 Set

Case IV : when J = 1 , K = 1

Output of gates **G3 and g4** are always '1' it is clear from the expiration for R' and S'

$$R' = \overline{Clk.J.\bar{Q}} =$$

$$S' = \overline{Clk.K.Q} =$$



Internal Structure of J-K flip-flop

If the previous state of Q and Q' is given by Q =0 and Q' = 1

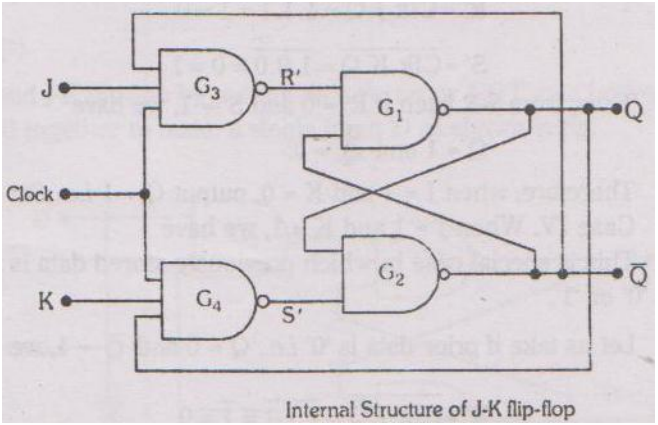
$$R' = \overline{Clk.J.\bar{Q}} = \overline{1.1.\bar{1}} = \bar{1} = 0$$

$$S' = \overline{Clk.K.Q} = \overline{1.1.0} = \bar{0} = 1$$

Thus the is input to gates **G1 (R')** = 0 and G2(S') = 1 respectively

Therefore when J = 1 and K = 0, output Q = 1 Set stat

Inputs			Outputs		State	
Clk	J	K	Q	$\bar{Q}$		
↑	0	0	Q	$\bar{Q}$	No Change	Positive Edge Triggered Cl
↑	0	1	0	1	Reset	
↑	1	0	1	0	Set	
↑	1	1	$\bar{Q}$	Q	Toggle	
0	X	X	Q	$\bar{Q}$	No Change	Flip-flop is disabled
1	X	X	Q	$\bar{Q}$	No Change	
↓	X	X	Q	$\bar{Q}$	No Change	



Internal Structure of J-K flip-flop

If the previous state of Q and Q' is given by Q =1 and Q' = 0

$$R' = \overline{Clk.J.\bar{Q}} = \overline{1.1.0} = \bar{0} = 1$$

$$S' = \overline{Clk.K.Q} = \overline{1.1.1} = \bar{1} = 0$$

Thus the is input to gates **G1 (R')** = 1 and G2(S') = 0 respectively

Therefore when J = 1 and K = 0, output Q = 0 Reset state