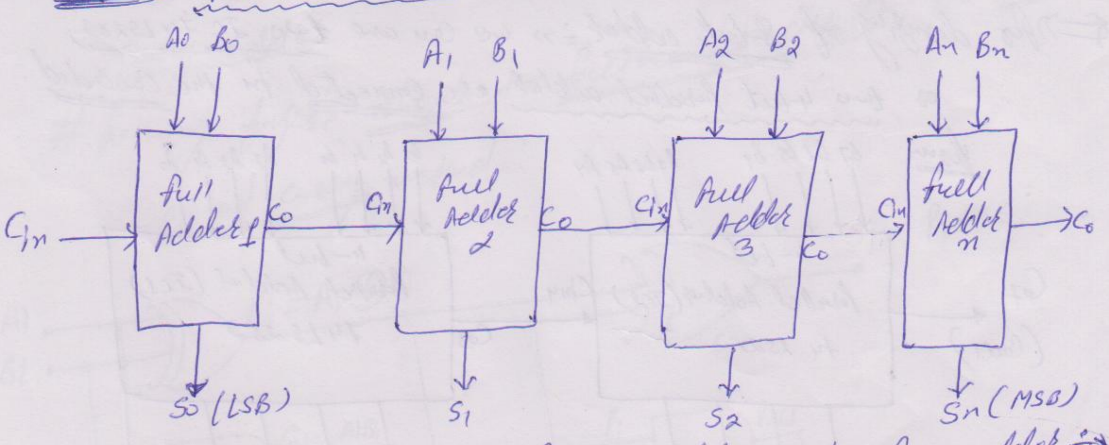
(D-16)

Binary - Parallal Adder or Ripple carry Adder

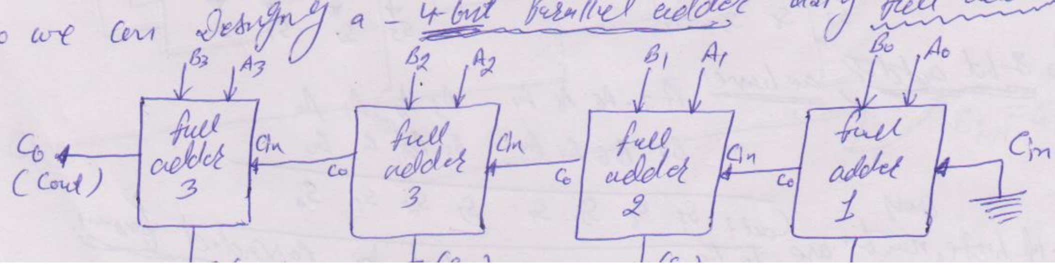
⇒ In case of full-adder - three ~~bits~~ bits added (Two one bit numbers and an input carry). If more than three bits are it be added then number of full adder are Reqired. Binary Parallel adders make the use of full adder for this construction.

⇒ full adder circuits are connected in cascade form, such that the carry output of each circuit is connected to the carry input of next higher order of full adder circuit.

⇔ n-bit parallel adder is shown in below :⇒

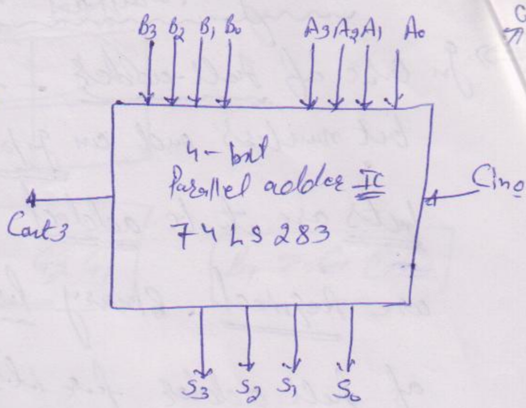


So we can Designing a - 4 bit parallel adder using full adder :⇒



→ Here, the Least significant bit position is made "0" through ground.

→ The logic Diagram of 4-bit parallel adder is shown as:⇒



V.Imp

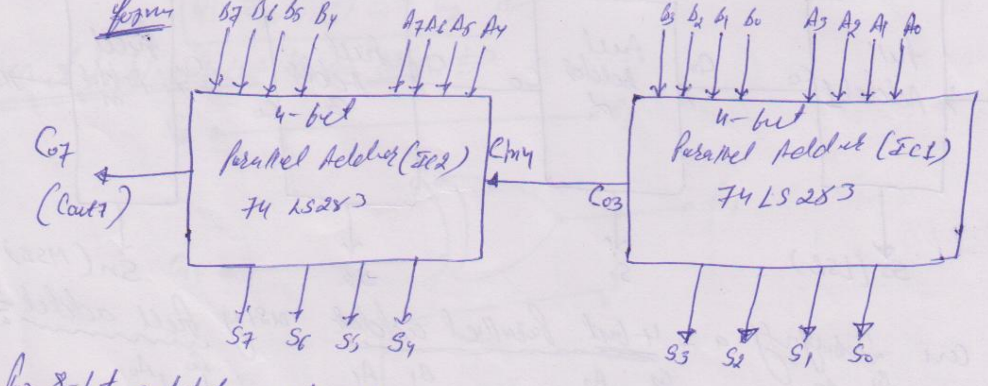
⇐⇒ 4-bit parallel adder means group of 4-bit added with another group of 4-bit, such as:

$$\begin{array}{ccccc} & A_3 & A_2 & A_1 & A_0 \\ & B_3 & B_2 & B_1 & B_0 \\ \hline C_{out3} & S_3 & S_2 & S_1 & S_0 \\ \hline \end{array}$$

→ If carry is comes in any of addition bits, it is added to the next higher order bits.

⇒ 4-bit parallel adder is typical example of MSI (Medium Scale Integration) TTL circuits. These adder are faster but costlier.

⇐⇒ for designing of 8-bit adder ⇒ we can use two IC 74LS283, or two 4-bit parallel adder are connected in the cascaded form



for 8-bit adder, we have:

$$\begin{array}{ccccccccc} & A_7 & A_6 & A_5 & A_4 & A_3 & A_2 & A_1 & A_0 \\ & B_7 & B_6 & B_5 & B_4 & B_3 & B_2 & B_1 & B_0 \\ \hline C_{out7} & S_7 & S_6 & S_5 & S_4 & S_3 & S_2 & S_1 & S_0 \end{array}$$

→ If large binary number are to be added then these adder are connected in cascaded form

Look Ahead Carry Adder

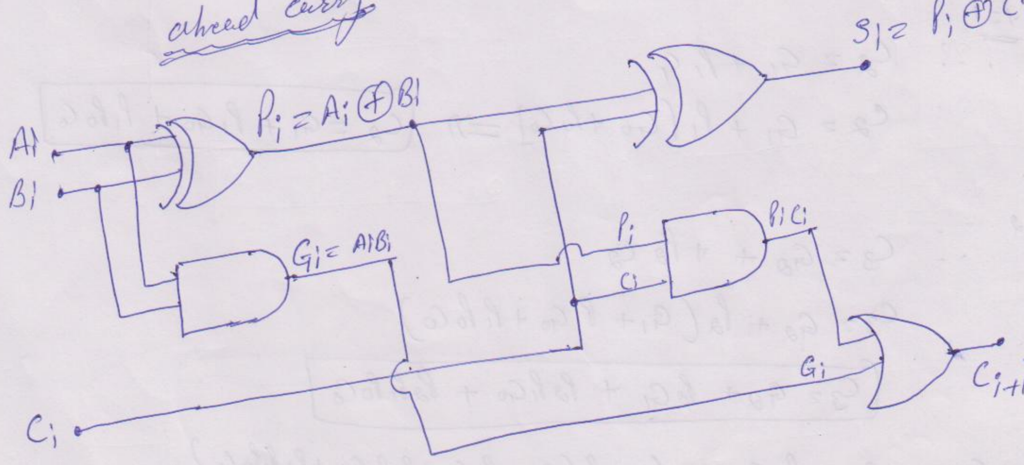
⇒ In case of n-bit parallel adders there comes a disadvantage of delay. for 4-bit parallel adder the delay is 120ns if each full adder has a propagation delay of 30ns. To overcome this problem look ahead -carry adder is designed.

⇒ In this logic gates are used to look at the lower bits and see if higher-order carry is generated.

⇒ It make the use of two fn, carry generate and carry propagate

⇔ This method is adopt to speed up the ripple or decreasing the propagation delay of parallel adder is in look ahead carry adder

following figure shows the full-adder circuits for look ahead carry method:



from the figure, Two fn are defined as:

Carry Prepagate ⇒ $\boxed{P_i = A_i \oplus B_i}$ — (1)

⇒ Here the Term "Carry Prepagate bel It is associated with the Prepagation of carry from C_i to C_{i+1}.

Carry Generate ⇒ $\boxed{G_i = A_i B_i}$ — (2)

⇒ Similarly, the Term "Carry Generate" and It Produces carry when both A_i and B_i are "1" Regardless of carry input.

⟺ from the figure, carry and Sums output are given by:

$$\boxed{\begin{aligned} S_i &= P_i \oplus C_i \quad \text{—— (3)} \\ C_{i+1} &= G_i + P_i C_i \quad \text{—— (4)} \end{aligned}}$$

Now, Let us calculate the carry O/P of each stage for Boolean Expressions ⇒

Let $i=0$, put in eq (1), (2), (3), and (4)

we get

$$\boxed{\begin{aligned} P_0 &= A_0 \oplus B_0 \\ G_0 &= A_0 B_0 \\ S_0 &= P_0 \oplus C_0 \\ C_{0+1} &= G_0 + P_0 C_0 \Rightarrow \boxed{C_1 = G_0 + P_0 C_0} \end{aligned}}$$

Similarly

$i=1$

$\therefore \; C_2 = G_1 + P_1 C_1$

$C_2 = G_1 + P_1 [G_0 + P_0 C_0] \Rightarrow \boxed{C_2 = G_1 + P_1 G_0 + P_1 P_0 C_0}$

Also

$i=2$

$\therefore \; C_3 = G_2 + + P_2 C_2$

$C_3 = G_2 + P_2 (G_1 + P_1 G_0 + P_1 P_0 C_0)$

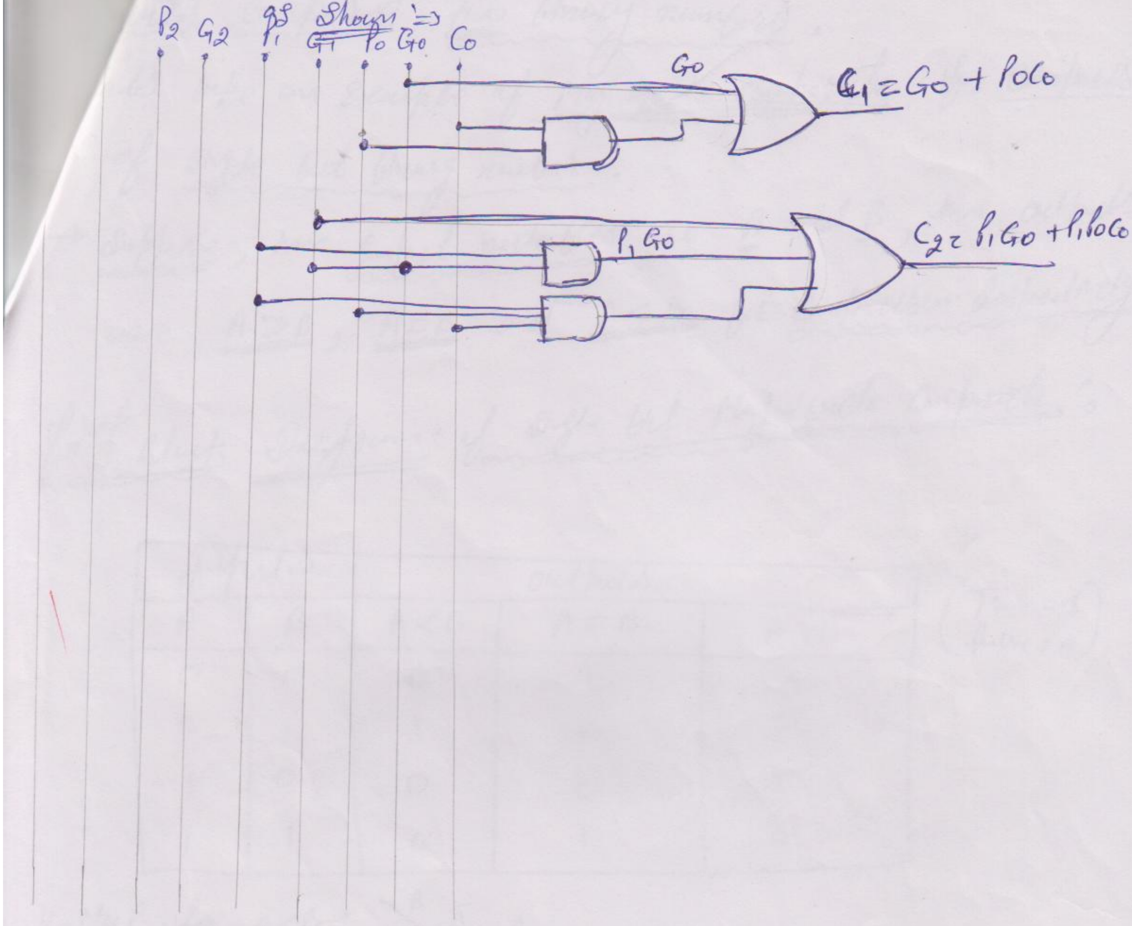
$\boxed{C_3 = G_2 + P_2 G_1 + P_2 P_1 G_0 + P_2 P_1 P_0 C_0}$

Also $i=3$, $C_4 = G_3 + P_3 C_3 \Rightarrow G_3 + P_3 (G_2 + P_2 G_1 + P_2 P_1 G_0 + P_2 P_1 P_0 C_0)$

$C_4 = G_3 + P_3 G_2 + P_3 P_2 G_1 + P_3 P_2 P_1 G_0 + P_3 P_2 P_1 P_0 C_0$

e Logic diagram for Look ahead carry generator is (D-18)

as Shown ⇒


P_2
G_2
P_1
G_1
P_0
G_0
C_0
G_0
$C_1 = G_0 + P_0C_0$
P_1G_0
$C_2 = P_1G_0 + P_1P_0C_0$