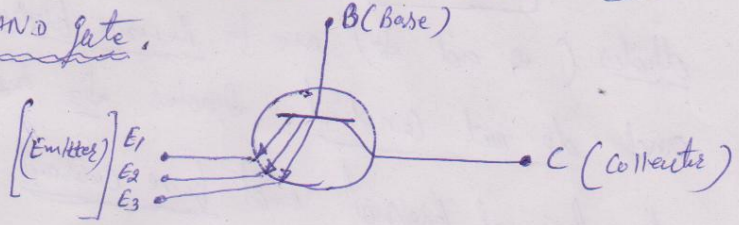
TTL (Transistor Transistor Logic)

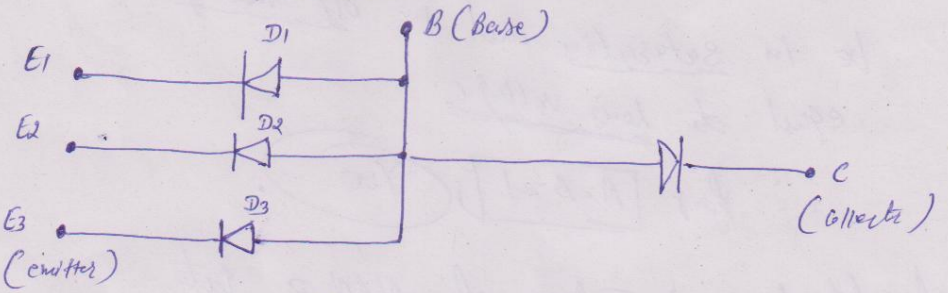
→ It was developed in 1965 as a standard TTL. DTL was used in SSI chips. The next stage of logic circuits was to introduce a new kind of Transistor — and the name of transistor is Multi-emitter transistor, which is used to minimized the number of chips inter-connection.

Multi-emitter Transistor ⇒ This transistor has more than one emitter. It can have upto seven emitters for seven input NAND gate.



multi-emitter transistor

Equivalent ckt of Multi-emitter transistor ⇒



multi-emitter ckt

Working:

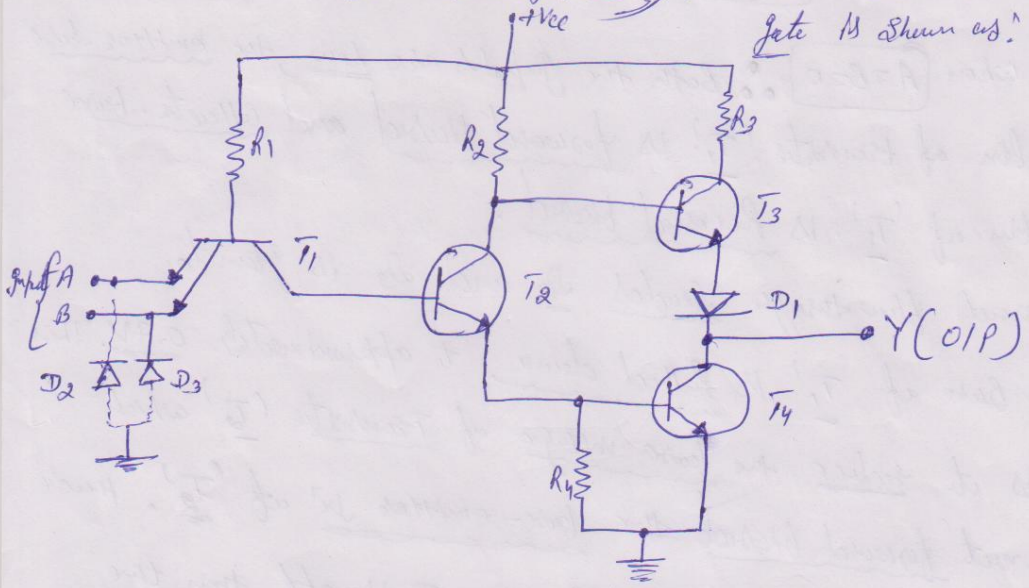
(Case-1): when one input or all the inputs are low then the diodes D1, or D2 or D3, or all are forward biased and Transistor is turned ON

(Case-2): when all inputs are high, then the diodes D1, D2 and D3 are in reverse biased, and transistor will be off.

There are basically 3-types of TTL

1. Two input TTL NAND gate
2. Totem-pole output gate → or Active pull up TTL gate
3. Open-collector TTL gate

TTL NAND Gate (for Two Inputs): The basic ckt of TTL NAND gate is shown as:



TTL NAND Gate

→ The inputs A and B are given to the transistor (T_1) which is a multiple transistor. Diodes D_2 and D_3 are connected at the inputs A and B of transistor (T_1), so as to protect (T_1) from the -ve spikes of voltage from A and B.

→ The Transistors (T_3) and (T_4) are the output transistors to form a "Totem-pole" connection.

→ It is a combination of two NPN transistors are connected in series with a diode in between.

→ Most of the TTL devices make the use of "Totem-pole O/P"

→ The diode D_1 is connected b/w the T_3 and T_4, because only one transistor conducts at a time.

→ when T_3 is ON, O/P goes high and when T_4 is ON, O/P goes low. Here, the transistor T_3 act as emitter follower.

→ The selected value of resistance are:

$R_1 = 4K\Omega$ $R_2 = 1.16K\Omega$ $R_3 = 130\Omega$ $R_4 = 1K\Omega$

Case-1 ⇒ when $A=B=0$ ∴ Both the inputs are low, the emitter-base junction of transistor 'T_1' is forward biased and collector-base junction of 'T_1' is Reversed biased.

→ Current flow through diodes D_2 and D_3 is ground.

→ The Base of 'T_1' is pulled down to approximately 0.7V. This helps to reduce the base voltage of Transistor 'T_2' which can-not forward biased the base-emitter jn of 'T_2'. Hence the Transistor 'T_2' is cuts off. When T_2 is off, then the Transistor T_4 will be off, beca it can-not get the Required voltage to drive the transistor 'T_4'.

→ Transistor 'T_3' will be ON, because No current flow through 'T_2' and whole of current goes to base of Transistor 'T_3'. then O/P Y is pulled up to a high voltage

$Y=1$

Case-2: when A=0 and B=1

or A=1 and B=0 ∴ Any one input is low, the base-emitter Jn of 'T_1' again forward biased and collector-base Jn is Reversed biased

⇒ Again T_2 is goes to off state and 'T_4' goes to off state. Thus 'T_3' will go to ON state and output Y is pulled up to a high voltage, i.e Y=1

Y=1

Case-3: when A=B=1 ∴ both the inputs are high, then emitter-base Jn of Transistor 'T_1' is Reversed biased then 'T_1' stop conducting, but the collector-base Jn of 'T_1' is forward biased. This forces the Transistor 'T_2' to turn on through Resistance R_1. This again forces the 'T_4' to turned ON.

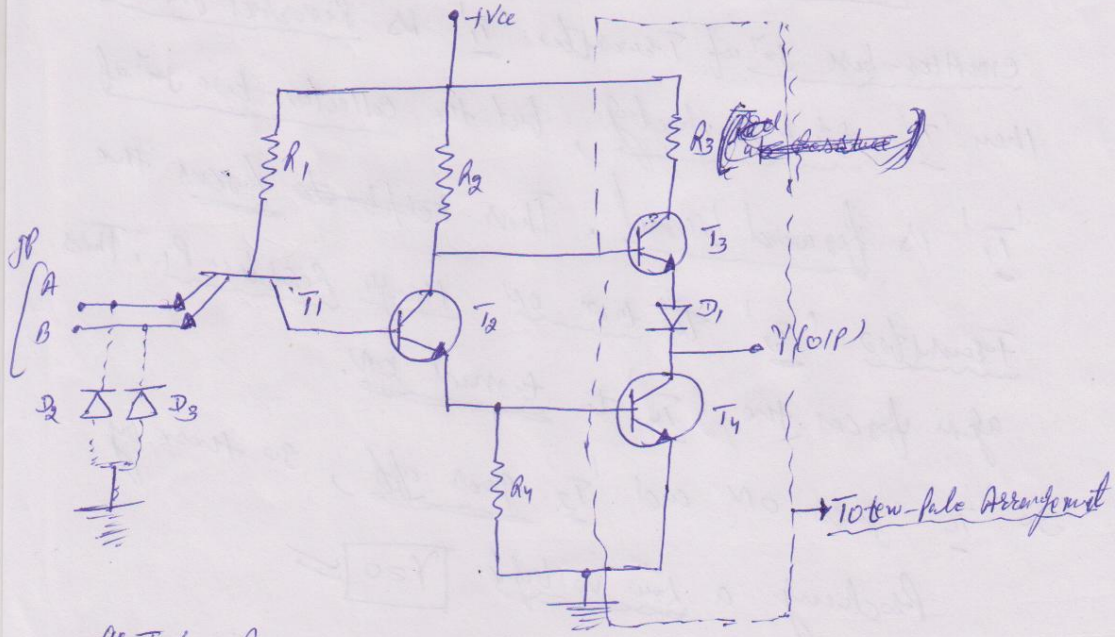
So 'T_4' goes ON and 'T_3' goes off, so thereby producing a low voltage Y=0

(2) Totem-pole output OR Active pull-up TTL Gate :=)

→ In this case, Transistor T_3 and T_4 with Diode D_1 and Resistance R_3 are connected in the form of Series arrangement, and this type of arrangement is called "Totem-pole arrangement."

→ Totem-pole Transistor are used because they gives "Low output Impedance". At a time, only one transistor will conduct. Both the transistor 'T_3' and 'T_4' cannot be ON or off Simultaneously.

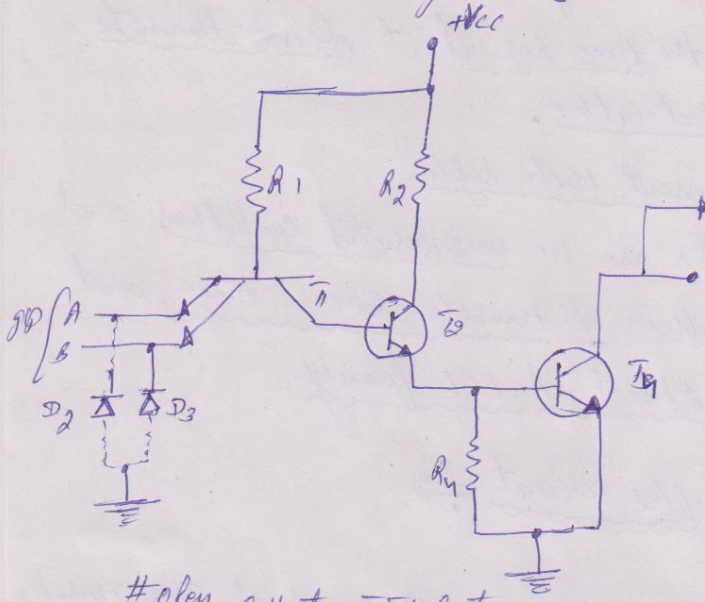
→ When Transistor 'T_4' is ON, the O/P Impedance is about 12Ω. whereas when 'T_3' is ON, the O/P Impedance is about 70Ω. In both the cases O/P Impedance is low. It clear that the O/P voltage can change Quickly from one State to another. Its working is same as that of two-input TTL NAND Gate.



Totem-pole O/P NAND Gate

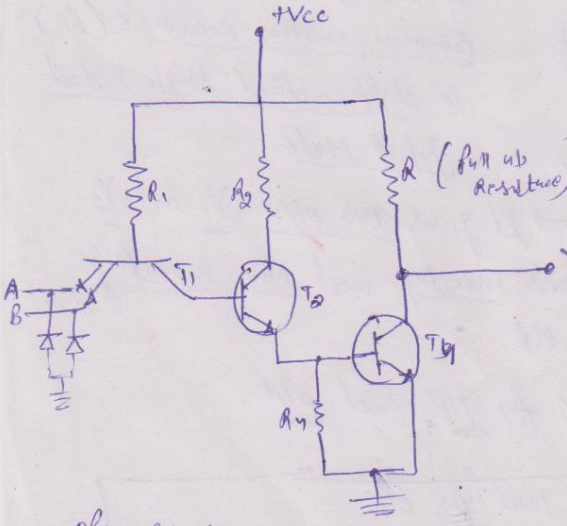
(3) Open-collector TTL gate ⇒ have an open-collector O/P instead of totem-pole output.

→ Open-collector TTL gate use only the transistor (T_4) of the totem-pole arrangement (lower transistor)



→ As the collector is open, gate will not work properly until an External pull-up Resistance is connected.

Open-collector TTL gate



Open Collector TTL gate with Pull up Resistance

→ when Transistor (T_4) is off, the o/p is pulled to +Vcc through the external pull-up resistor (R)

→ [when Transistor (T_4) is on, the o/p voltage is grounded through the saturated transistor]

→ The Pull-up Resistor (R) is selected only when one gate o/p goes high and other is low.

⇒ The disadvantage of OC gates are that, their switching speed is much slower than the T-Pole