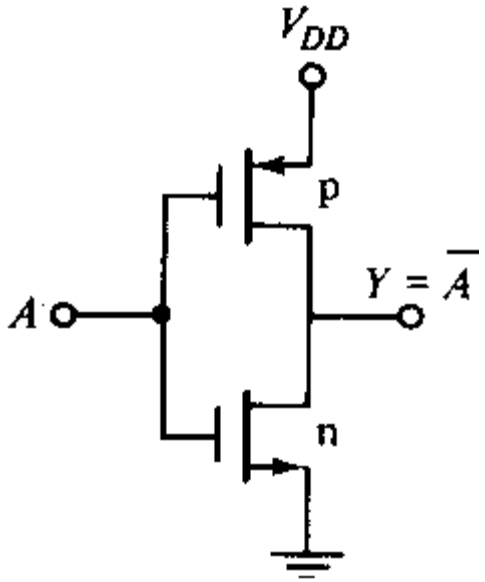
Complementary MOS (CMOS)

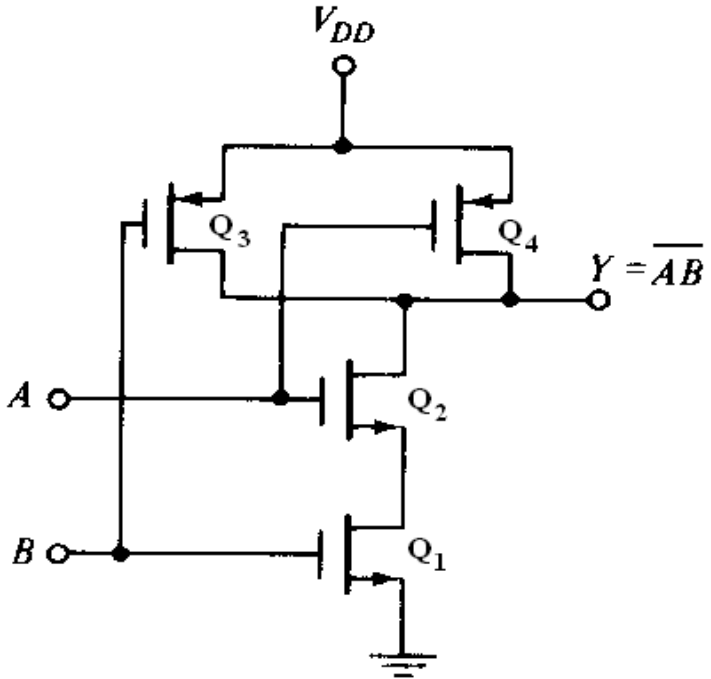
- Invertors NOT

A		O/P
0		1
1		0



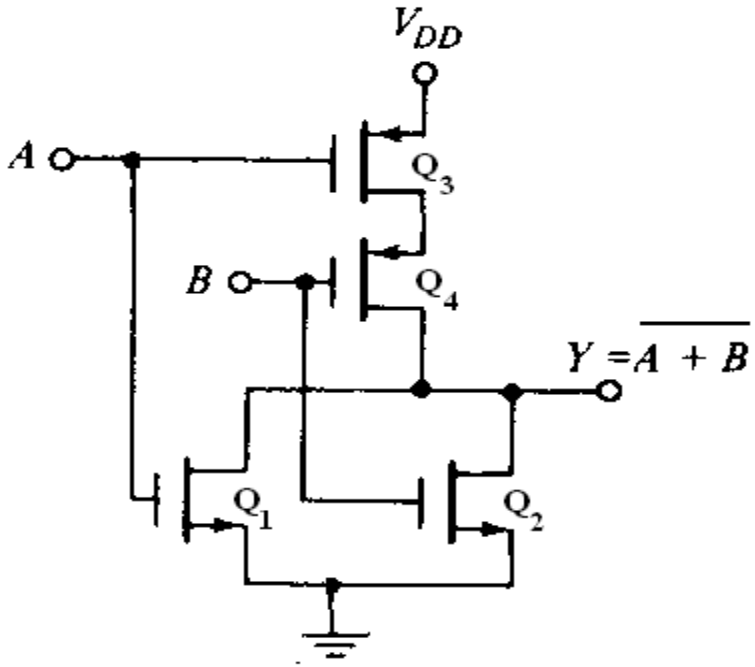
NAND gate

A	B		O/P
0	0		1
0	1		1
1	0		1
1	1		0



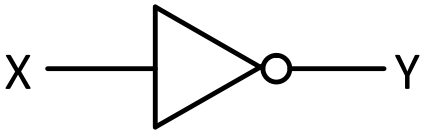
NOR Gate

A	B		O/P
0	0		1
0	1		0
1	0		0
1	1		0



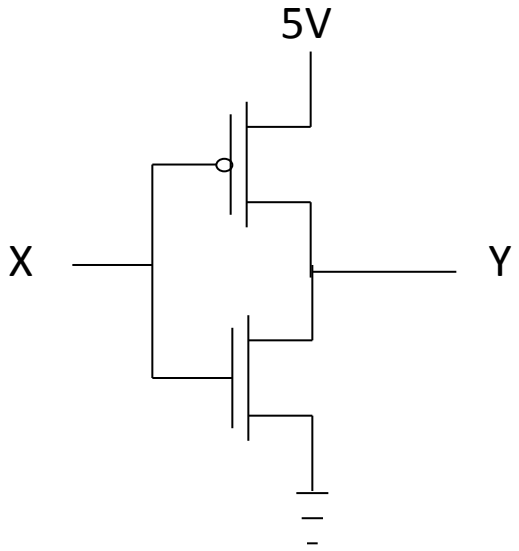
NOR gate

NOT Gate

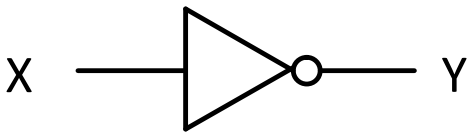


Y = ~X

X	Y
0	1
1	0

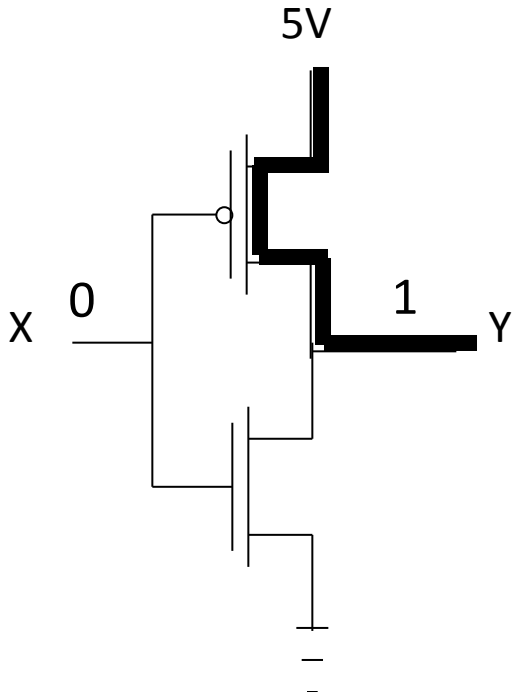


NOT Gate

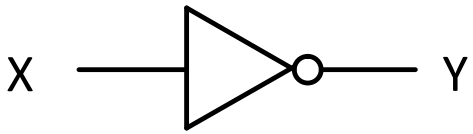


Y = ~X

X	Y
0	**1**
1	0



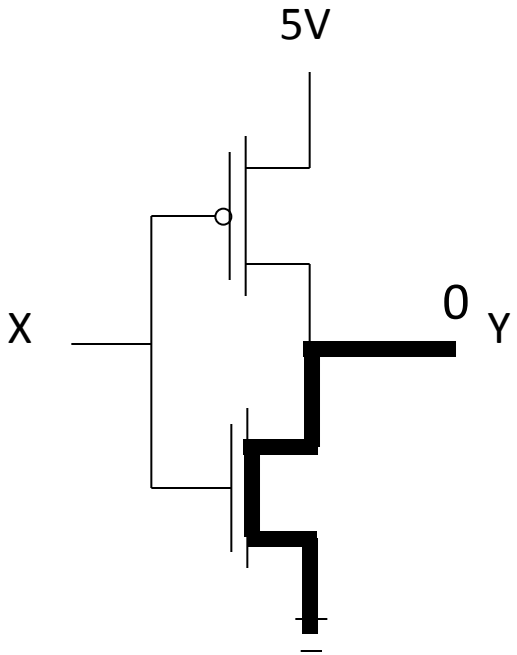
NOT Gate



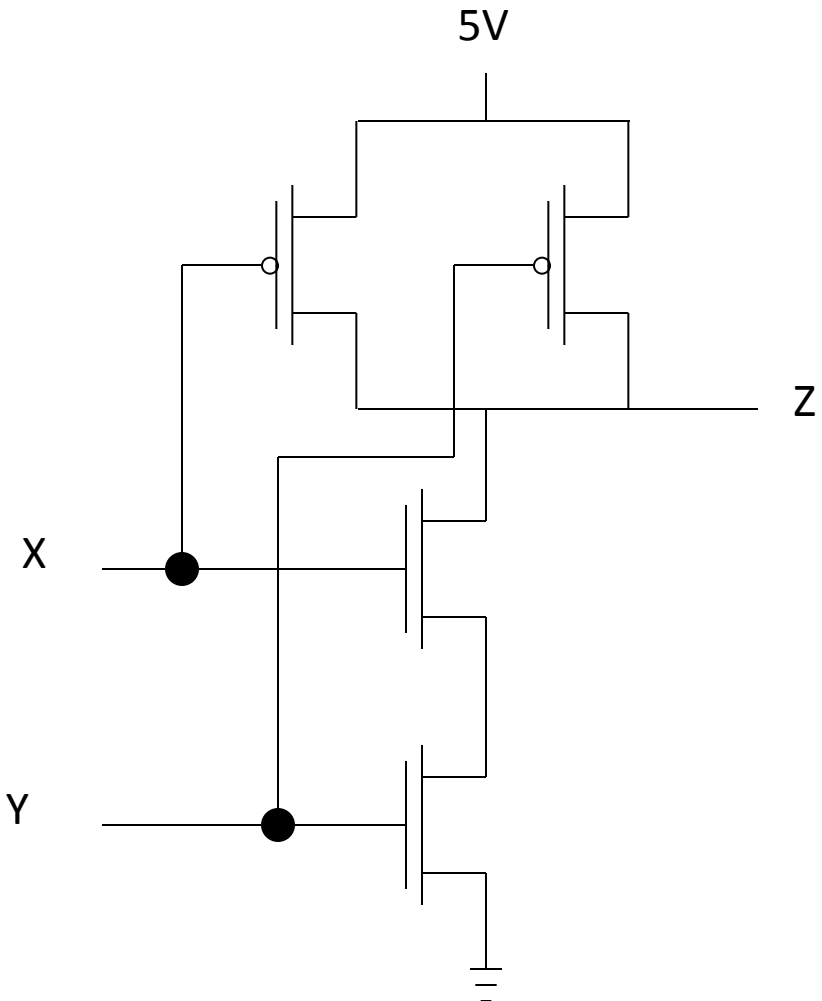
Y = ~X

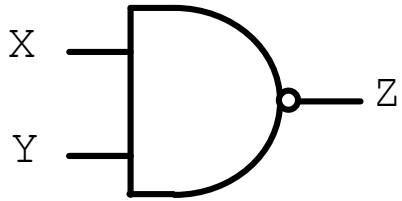
X	Y
0	1
1	**0**

1



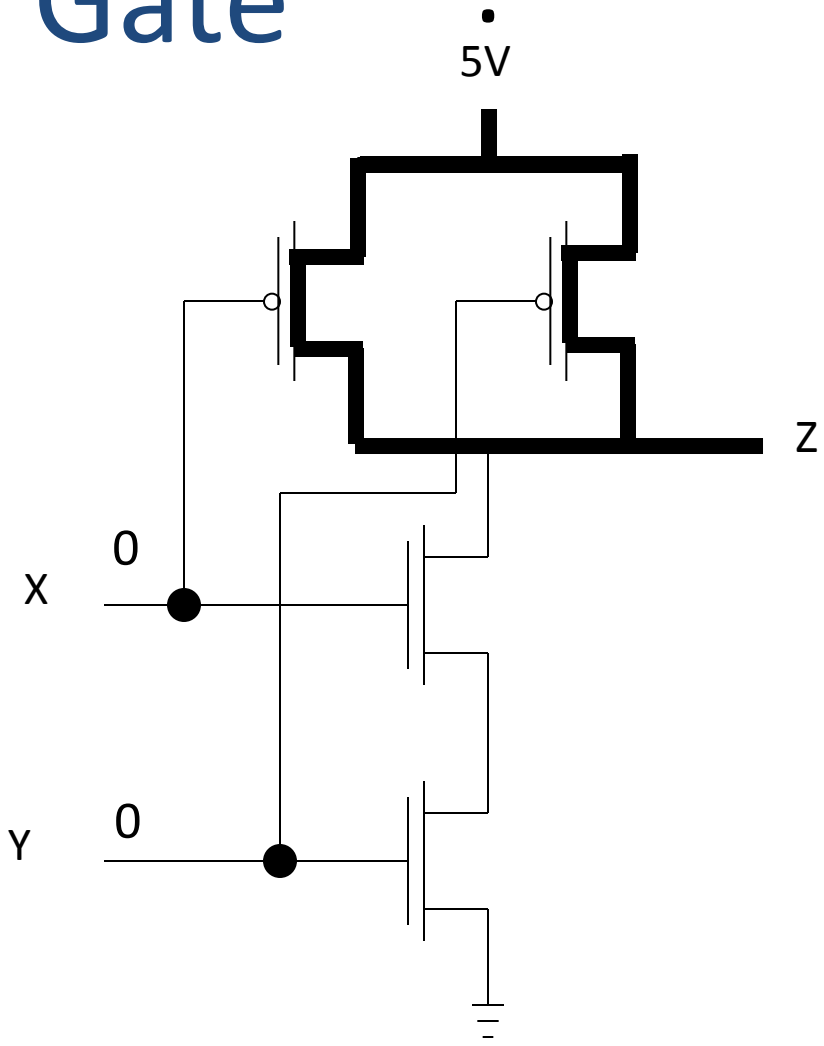
NAND Gate

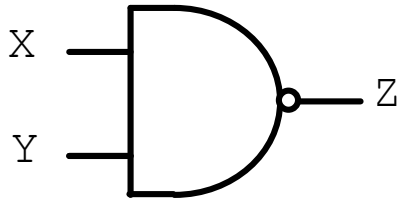




X	Y	Z
0	0	1
0	1	1
1	0	1
1	1	0

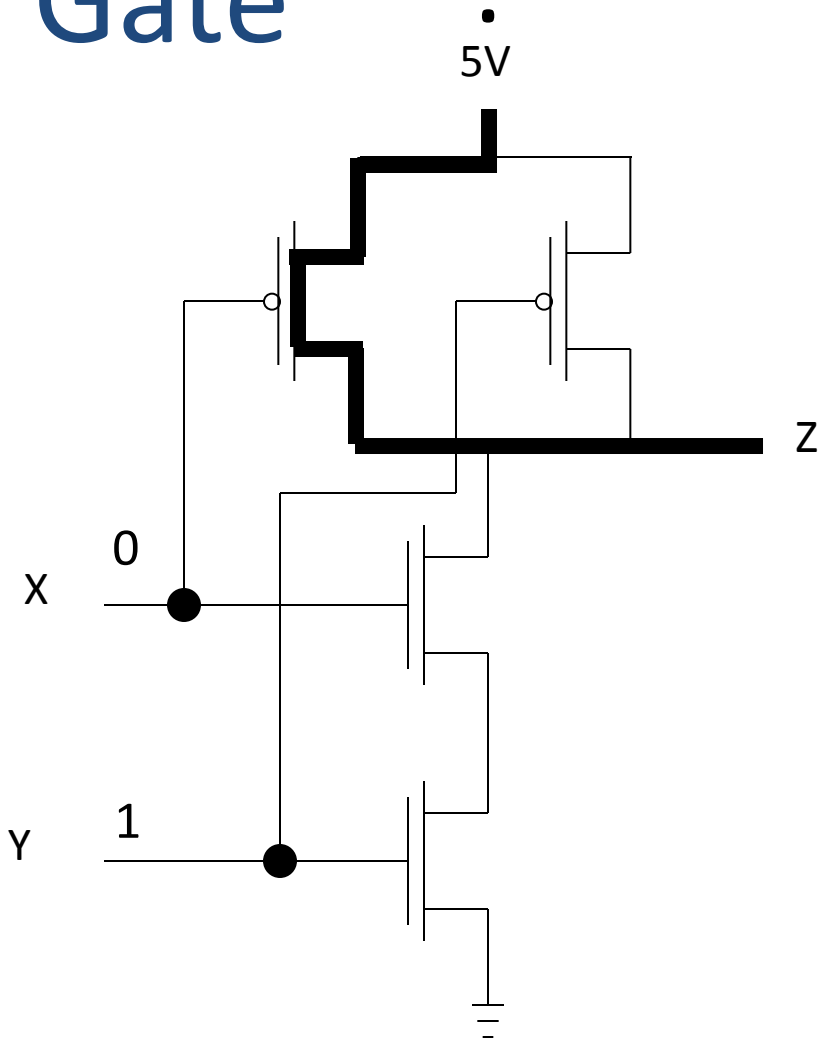
NAND Gate

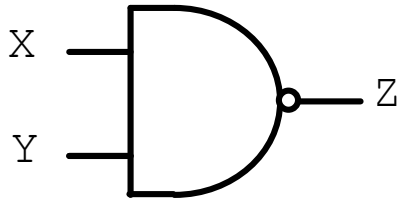




X	Y	Z
0	**0**	**1**
0	1	1
1	0	1
1	1	0

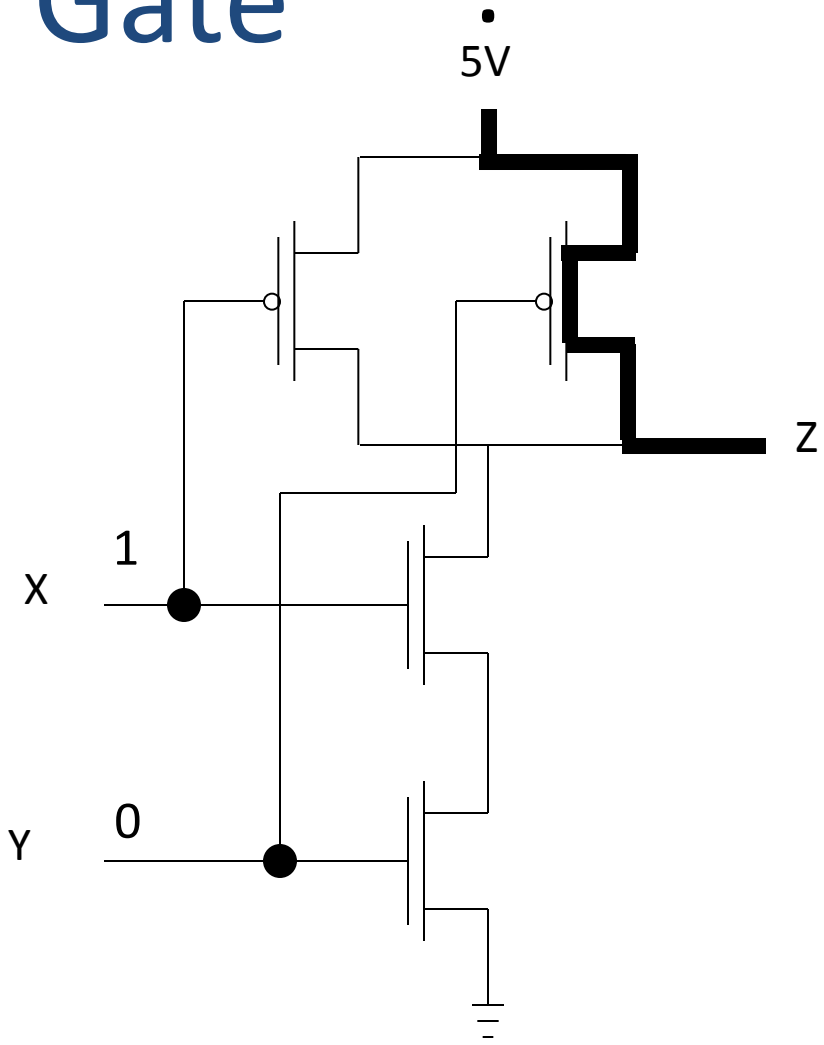
NAND Gate

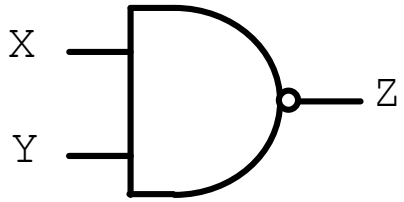




X	Y	Z
0	0	1
0	**1**	**1**
1	0	1
1	1	0

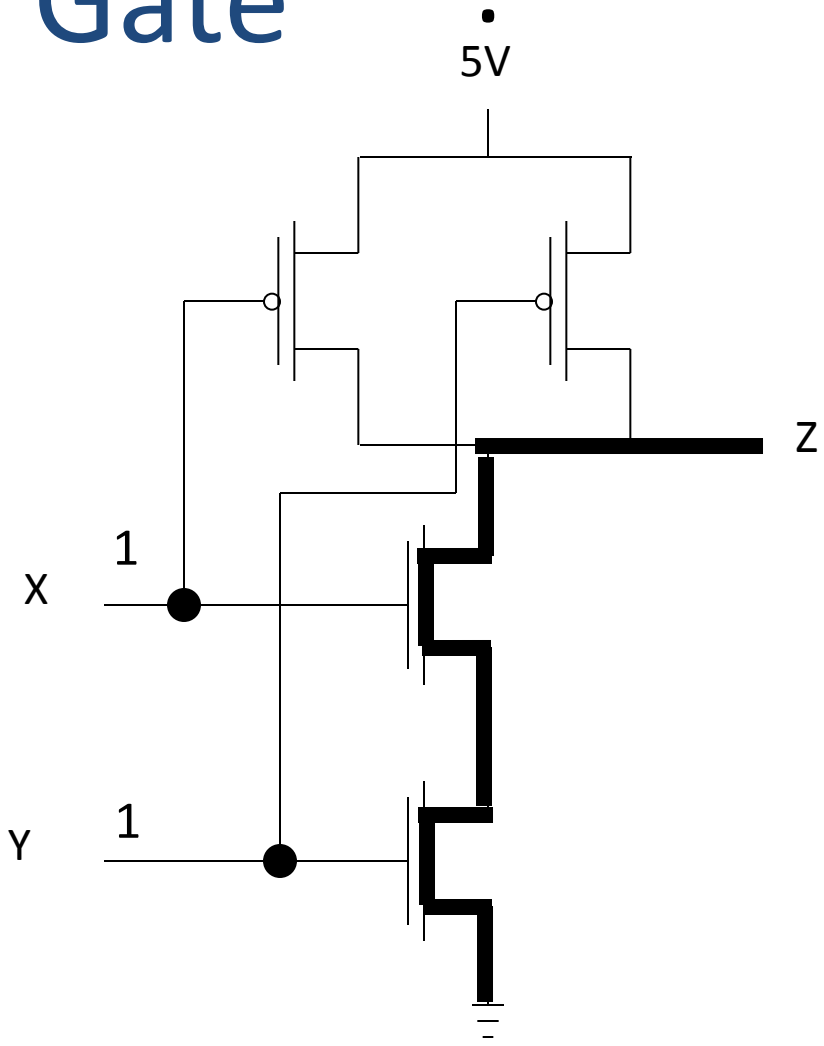
NAND Gate

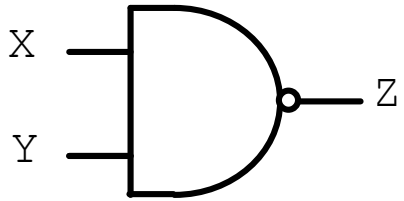




X	Y	Z
0	0	1
0	1	1
1	**0**	**1**
1	1	0

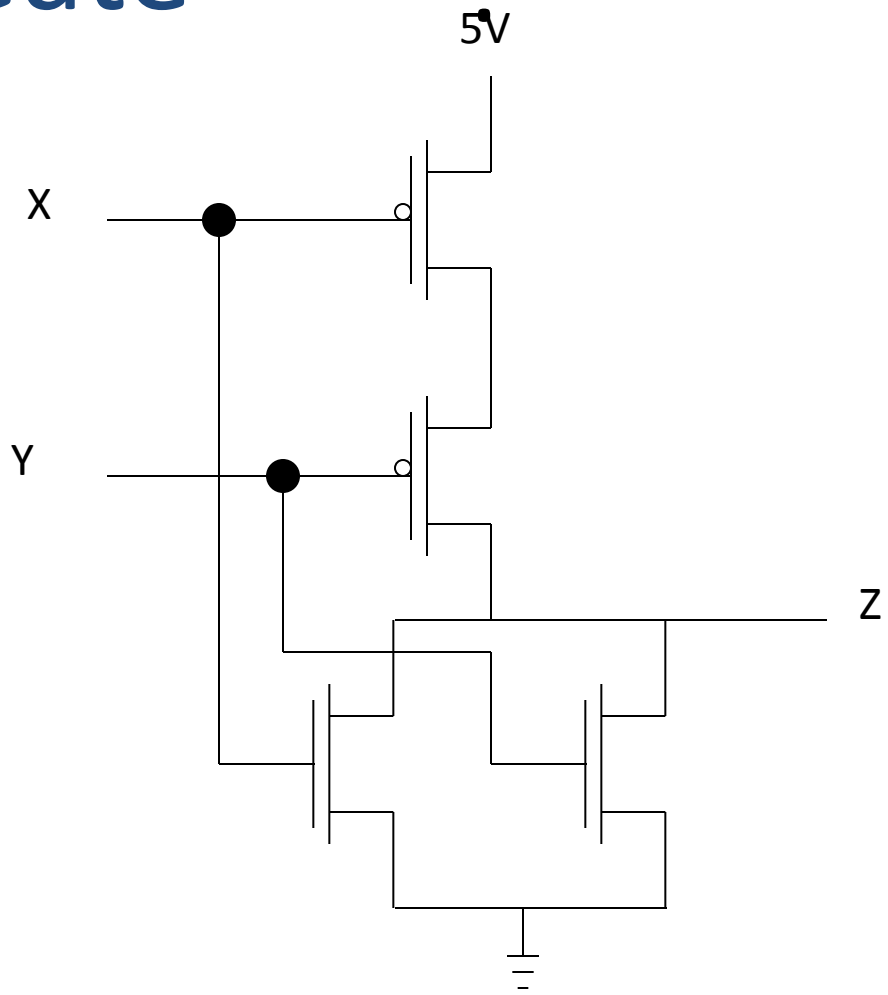
NAND Gate

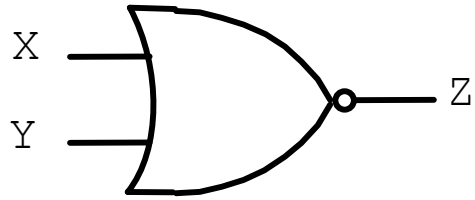




X	Y	Z
0	0	1
0	1	1
1	0	1
1	**1**	**0**

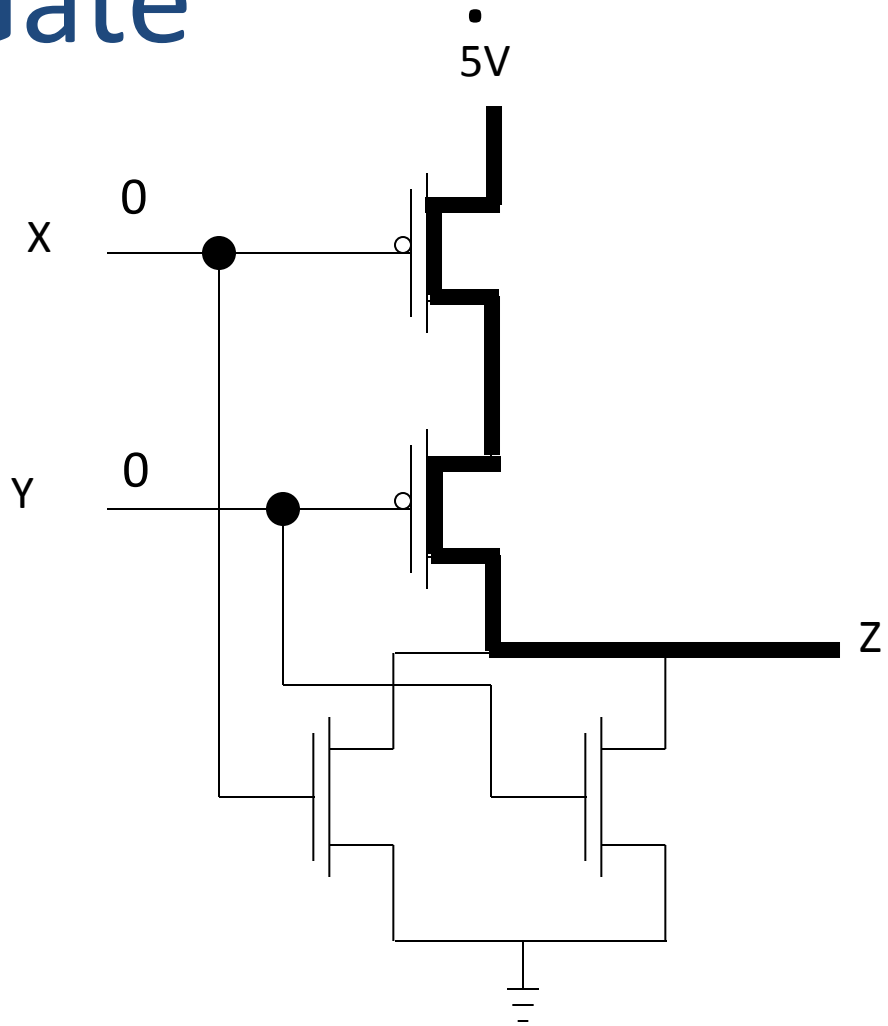
NOR Gate

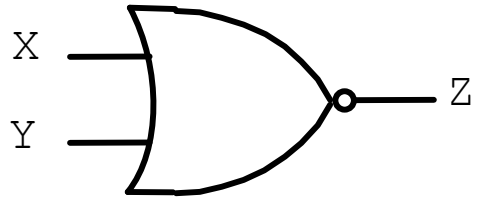




X	Y	Z
0	0	1
0	1	0
1	0	0
1	1	0

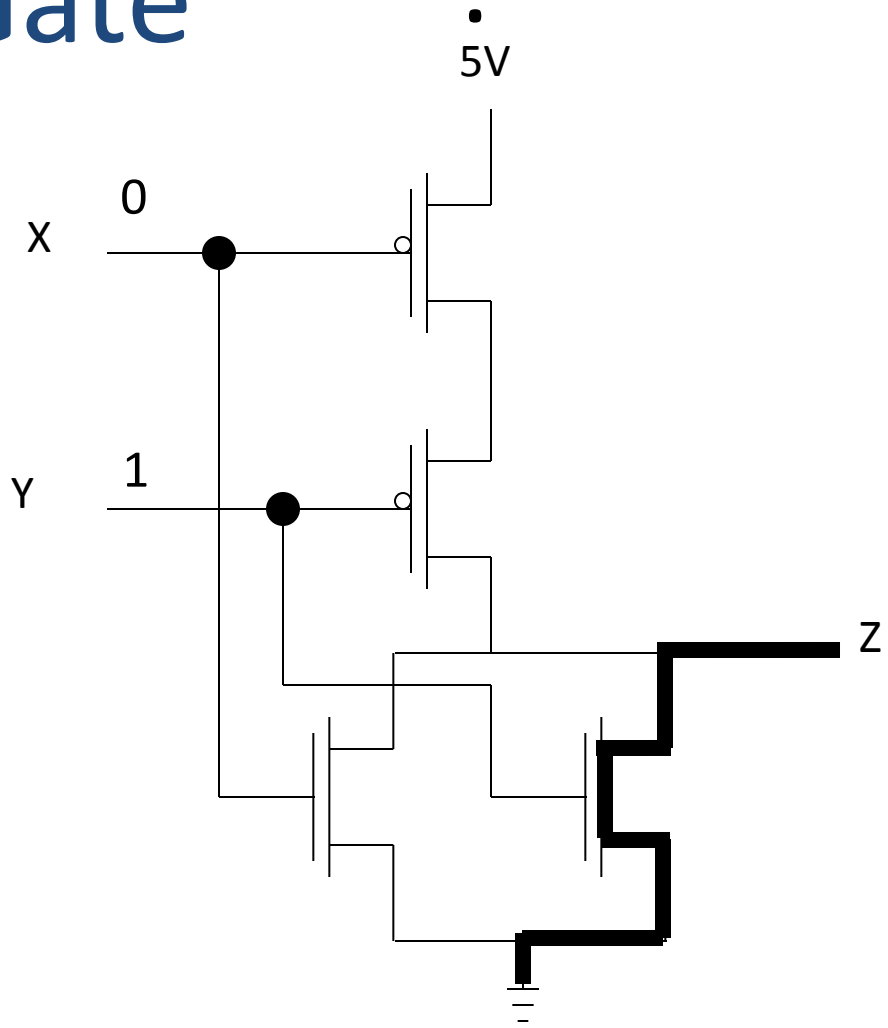
NOR Gate

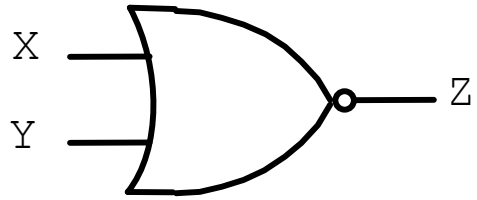




X	Y	Z
0	**0**	**1**
0	1	0
1	0	0
1	1	0

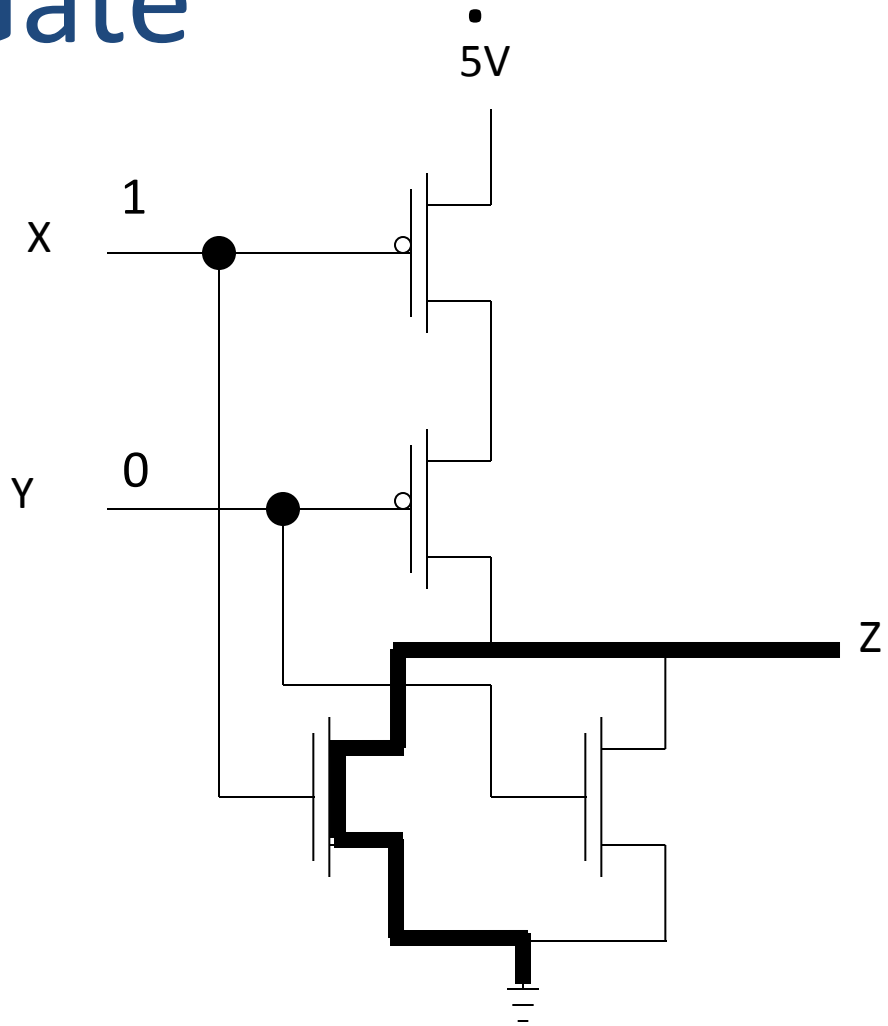
NOR Gate

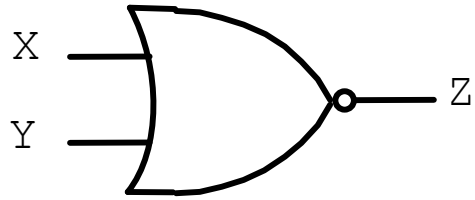




X	Y	Z
0	0	1
0	**1**	**0**
1	0	0
1	1	0

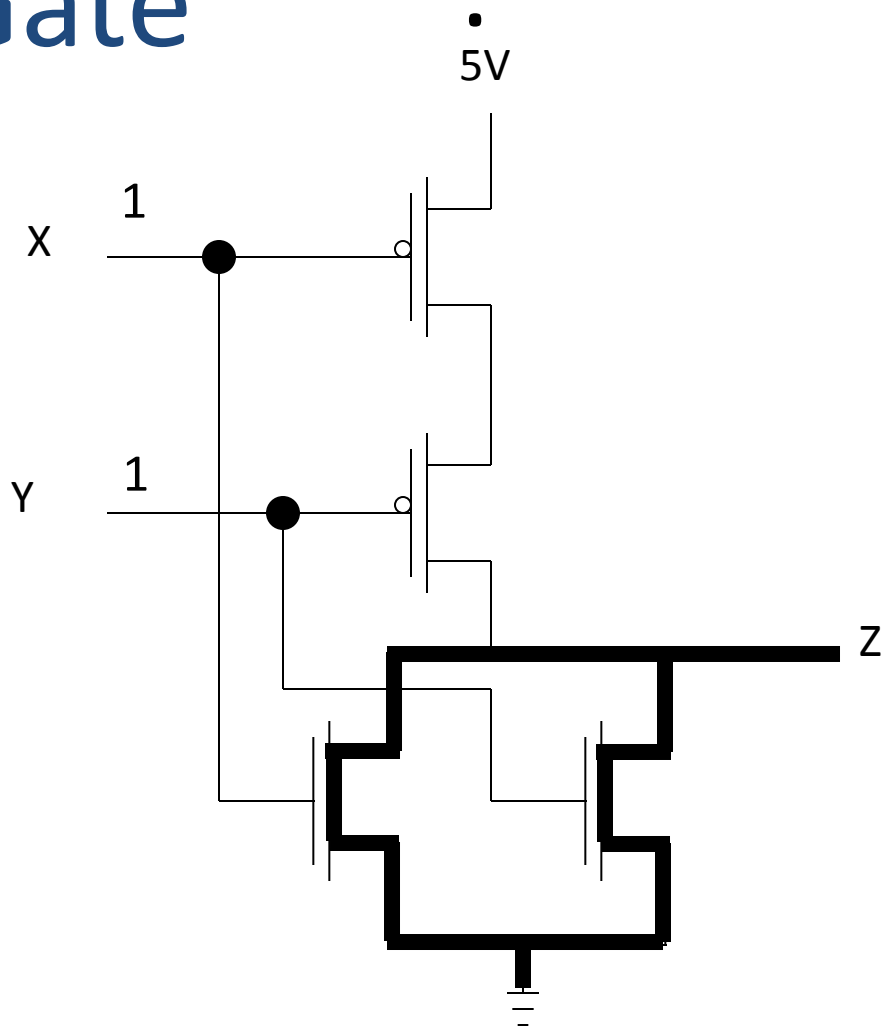
NOR Gate

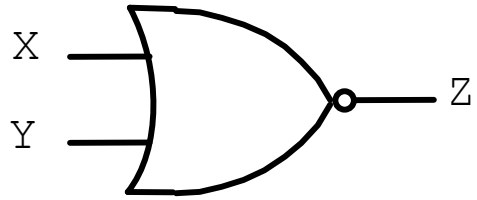


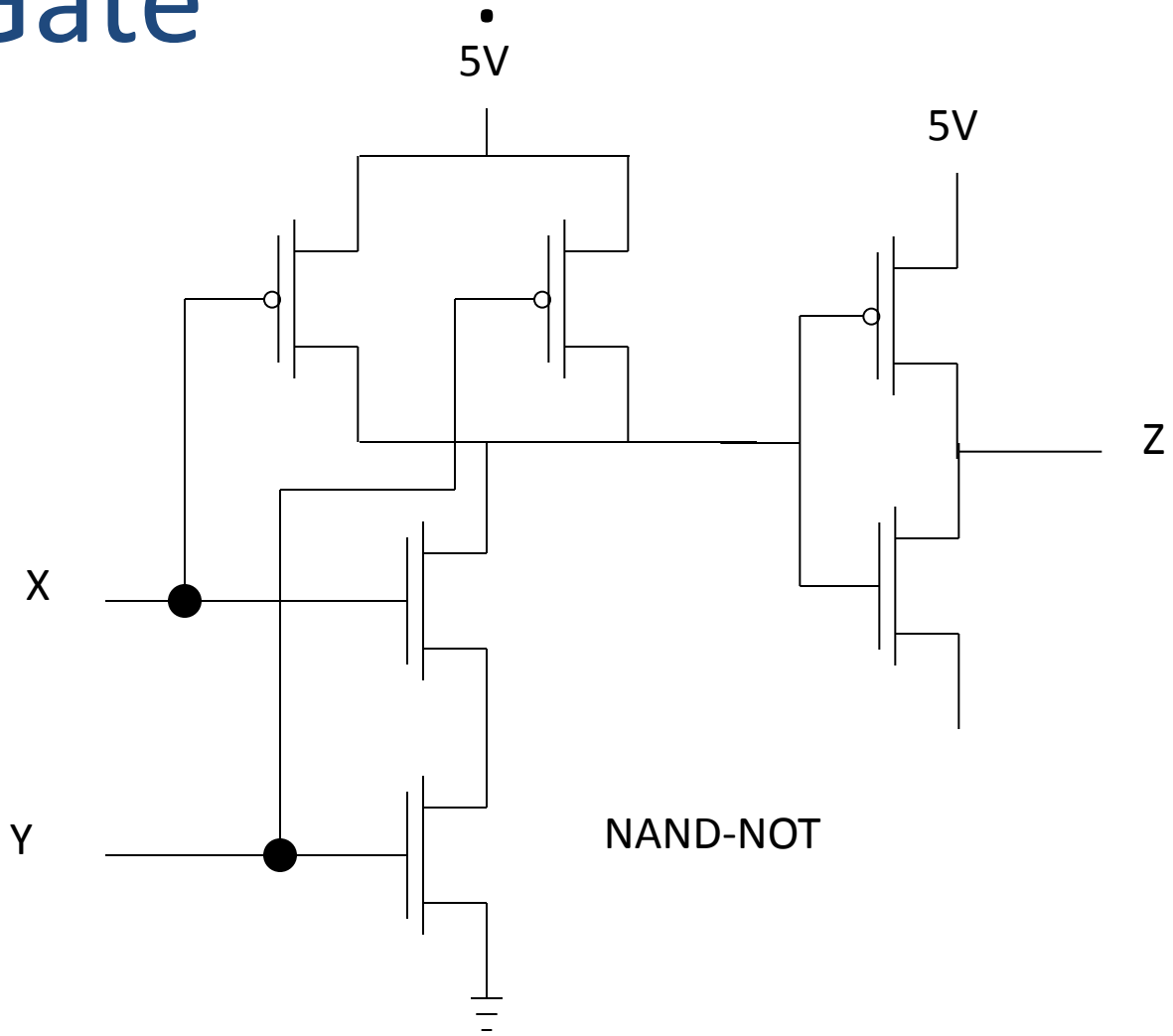


X	Y	Z
0	0	1
0	1	0
1	**0**	**0**
1	1	0

NOR Gate





X	Y	Z
0	0	1
0	1	0
1	0	0
1	**1**	**0**

AND Gate