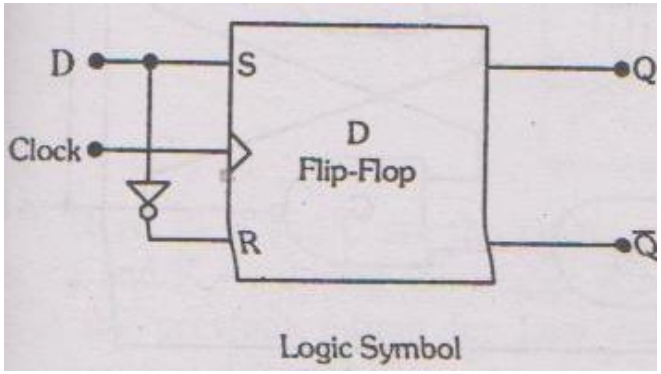
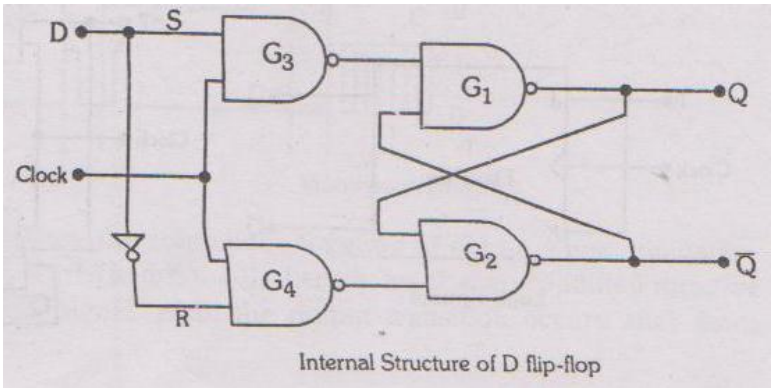
D Flip Flop

It can be designed from S R and J K flip flop by putting an inverter or Not Gate between (S and R) or (J and K)

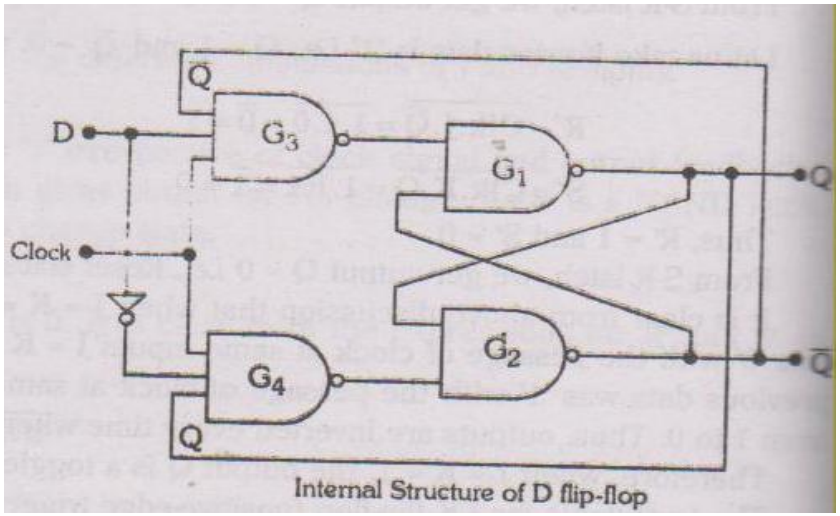


Logic Symbol



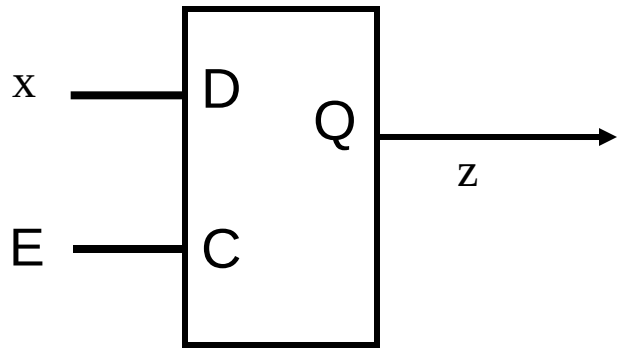
Internal Structure of D flip-flop

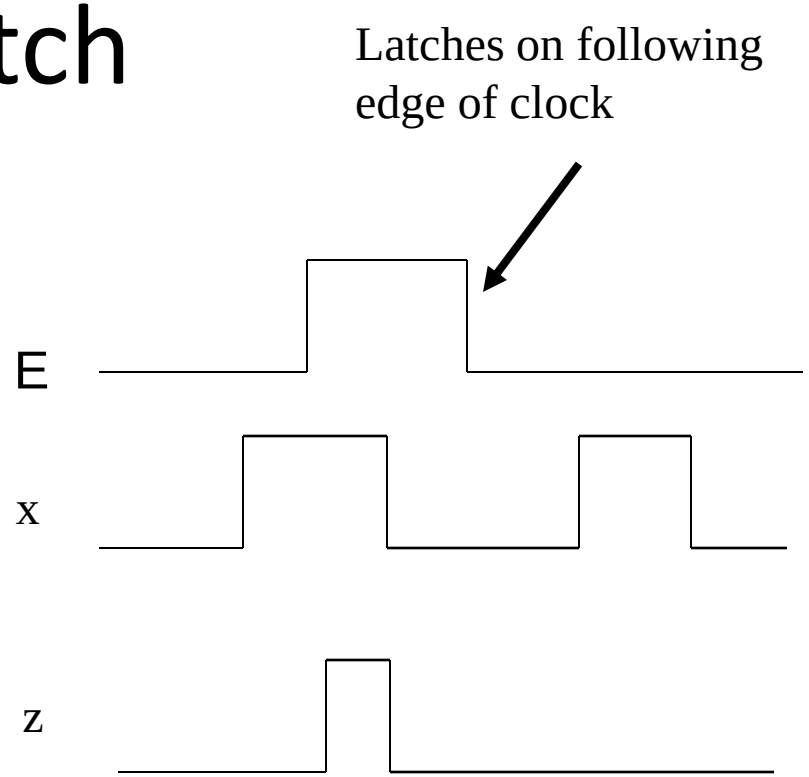
Inputs		Output	State
Clk	D	Q	
↑	0	0	Reset
↑	1	1	Set
0	X	Q	No Change



Internal Structure of D flip-flop

D Latch

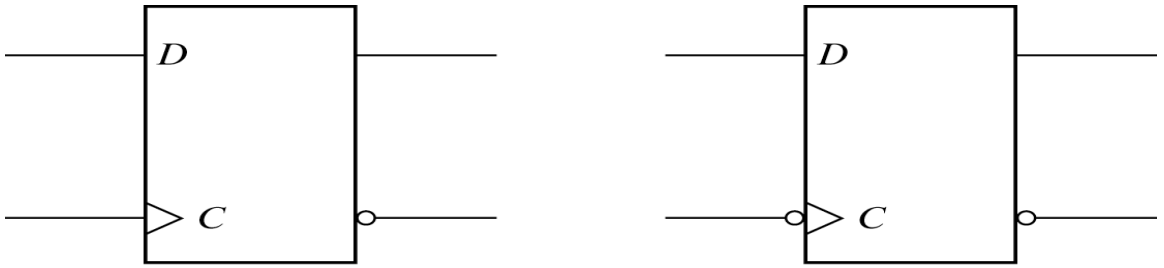




The D latch stores data indefinitely, regardless of input D values, if C = 0
Forms basic storage element in computers

Positive and Negative Edge D Flip-Flop

D flops can be triggered on positive or negative edge
Bubble before *Clock (C)* input indicates negative edge trigger



(a) Positive-edge (a) Negative-edge

Fig. 5-11 Graphic Symbol for Edge-Triggered *D* Flip-Flop

Lo-Hi edge

Hi-Lo edge