CHAPTER

A/D & D/A Converters

Converter ⇒ are used to convert one type of signal into another signal.

There are two types of converts

Analog to Digital converter

The process of conversion of signal from Analog signal to digital signal is referred to as A/D converter.

I. ~~Binary weighted~~
II. Single slop A/D Counter
III. Dual slop A/D Counter
IV. Continuous Counter A/D Converter
   or up/down counter A/D Converter
V. Successive Approximation A/D converter

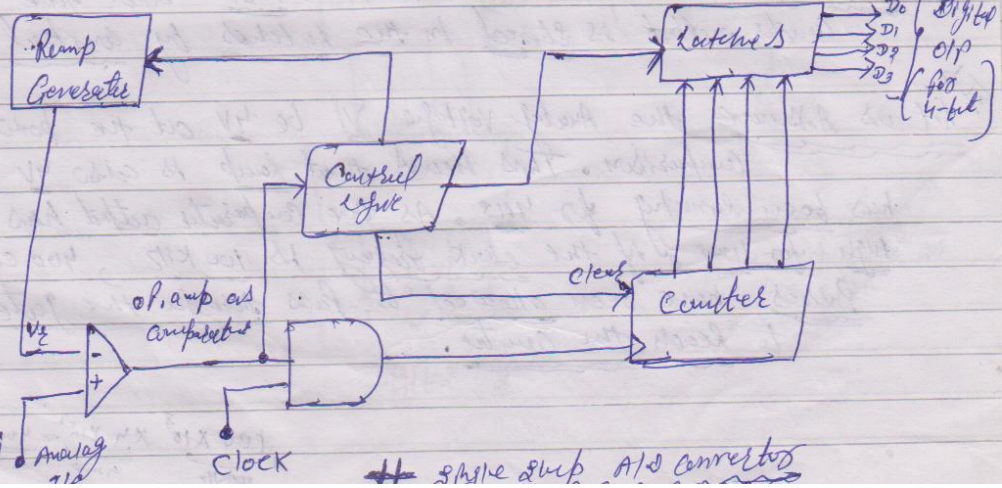
Digital to Analog converter

The process of conversion of signal from Digital signal to Analog signal is referred to as D/A Converter.

I. Binary weighted Resistance D/A converter
II. R-2R ladder D/A converter

Single slope A/D converter

* It is not used D/A converter, but it uses a Ramp generator to produce a constant slope reference voltage, It is shown as:



Single slop A/D converter

Its Main Components are

(I) Ramp Generators (II) Comparator (III) Counter
(IV) AND gate (V) Control Logic (VI) Latches

→ The counter is Reset initially, o/p is 0.000 (If 4-bit counter is used) and the Ramp generator o/p is zero volt (0V)

→ So, the input voltage V_i is greater than the Reference voltage (V_R) at this point and gives a high o/p from comparator. This high o/p from the comparator enables the clock to the counter and starts the Ramp Generator.

⇒ AND gate is used because if comparator o/p goes Low, then clock will be disabled and Counter stop, Because of any one i/p to the AND gate is goes low then output will be Low,

⇒ Let us assume, that the slope of the Ramp generator is 1V/ms. Ramp o/p will increase until equal the Analog Input, at this point → The Ramp is Reset and the Counter output is stored in the latches by control logic.

Eg:
Let us Assume the Analog voltage V_i be 4V at the point of comparison. This means that Ramp is also 4V and has been Running for 4ms. As the comparator output has been high for 4ms, if the clock frequency is 100 kHz, 400 clk pulses have been allowed to pass through the gate to Reach the Counter.

$100 \times 10^3 \times 4 \times 10^{-3} = 400$ clk
(100 kHz, 4ms)

→ At the point of comparison, the counter is in the binary state representing 400. with proper scaling and decoding, this binary number can be displayed as 4V. This concept is used in Digital voltmeter.

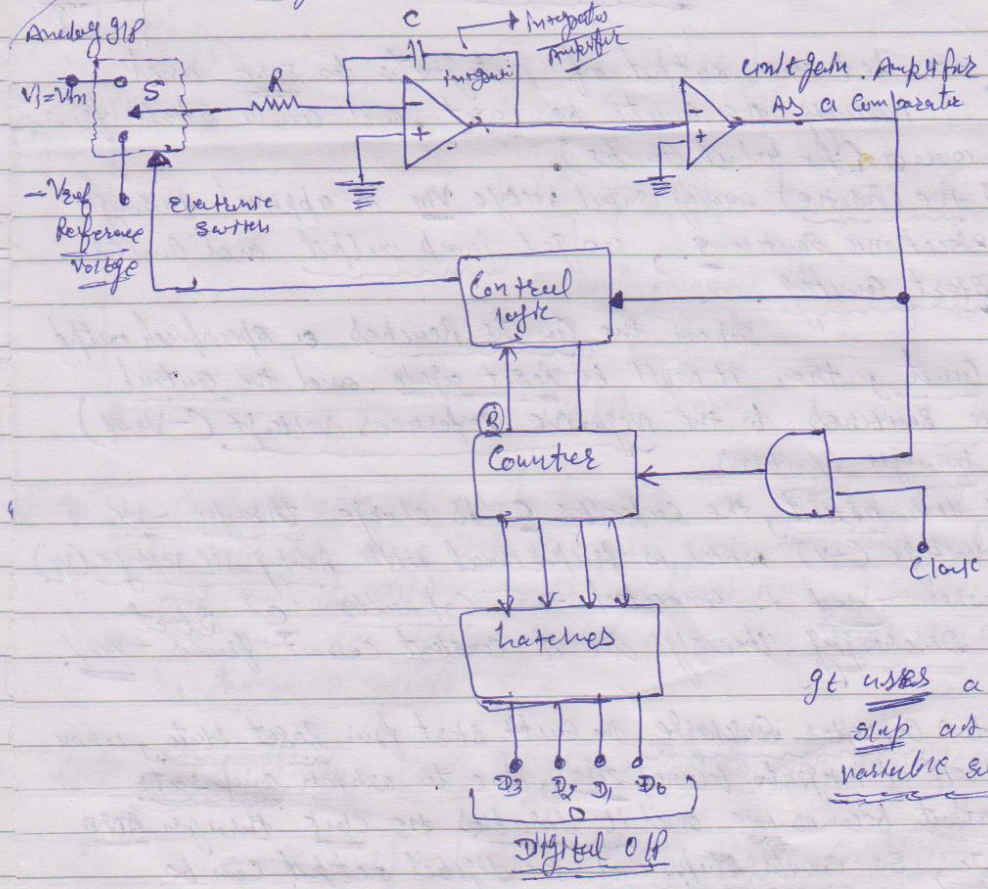
Dual Slope A/D Converter

→ Dual Slope A/D Converter is used because it is free from the noise which is not overcome by Single Slope A/D Converter.

→ It uses Op-Amp. as Integrator amplifier for Ramp generator.

→ It is called Dual Slop because it uses a fixed slop as well as variable Slope Ramp.

→ circuit diagram is shown below ⇒



It uses a fixed slop and well as variable slop

→ The Integrator Op-Amp uses a capacitor in the feedback path.

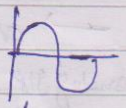
O/P of Integrator Op-Amp is given by:

$$V_{out} = -\frac{1}{RC}\int V_{in}\,dt$$

⇒ The o/p voltage is Integral of Analog input voltage.

(i). If V_{in} is constant, then we get an $o/p = -\frac{V_{in}\,t}{RC}$, which is fixed Ramp

(ii) If V_{in} is varying, we get the Ramp fixed as well as variable slope at its O/P.



Working ⇒ Let the output of Integrator be zero and initially the counter be Reset, and counter starts from zero (for 4-bit counter).

→ A +ve (positive) analog input voltage V_{in} is applied through Electronic Switch S, we get Ramp output and counter start counting.

When the counter Reaches a specified output or Count, then it will be Reset again and the control logic switches to the Negative Reference voltage (−Vref) through switches

→ At this instant, the capacitor C is charge through −ve voltage (−V) which is precharged with Analog I/P voltage (V_i)

→ when −Vref is connected the Capacitor (C) start Discharging linearly due to constant current from −Vref.

→ As the Capacitor Discharge, the counter start from Reset state, when the o/p of Integrator becomes zero, due to when comparator output becomes low and it disables the clock through AND gate, so Counter stops and the digital output can be obtained from latches. This complete one conversion cycle.

Successive Approximation A/D Converter

It is the most widely used in A/D converter. It has more complex circuit than the digital ramp A/D converter, but it has more shorter time conversion.

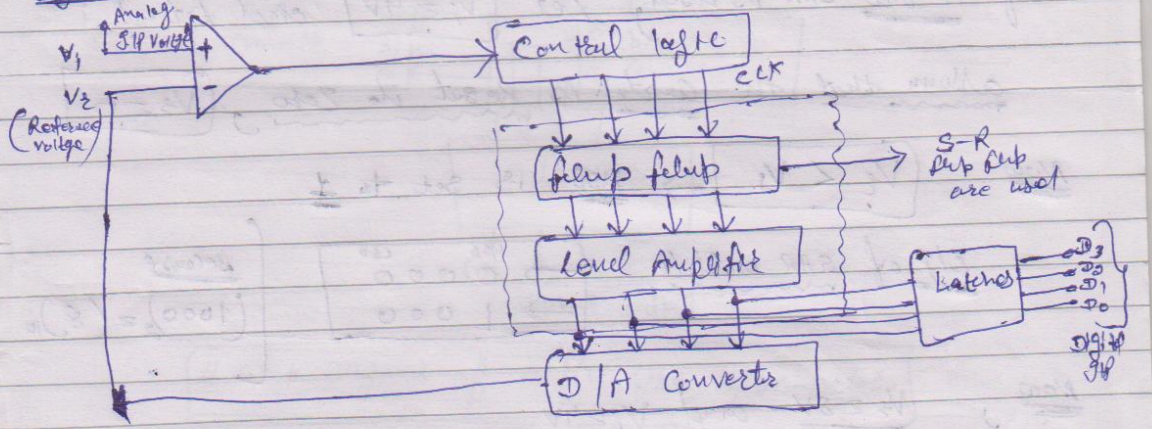
⟹ for n-bit A/D Converter, n-successive steps are required for completing the approximation process.

The various functional block of successive approximation A/D converter are

→ SAR consist of the flip flop and level amplifier.

(I) Comparator (II) D/A Converter (Binary ladder may be used)
(III) Control Logic (IV) Successive approximation Register (SAR)

figure shown as:



↔ The Control logic is used to set or Reset the flip flop. The O/P of these flip flop are given to Level Amplifier and from the D/A Converter comes is Binary ladder Network.
→ It gives the digital o/p as well as the analog Reference voltage V_2

↔ Initially the Control logic → Resets all the flip flop
→ Depend upon three Basic condition

(1) If $V_2 < V_1$ — Reference voltage from D/A conv. is less than the I/P voltage (Analog) then MSB is set to '1' by control logic.

(2) If $V_2 > V_1$ → then MSB is Reset to '0' and Next bit is set to '1'.

(3) If $V_2 = V_1$, then, the control logic Disable the clock to F-F and we get Digital O/P from SAR by using latches.

Let us consider an example for its working:

→ If 4-bit SAR is used, Let $V_i = 4V$ and let us assum that the counter is Reset to zero, $V_2 = 0$

Now $V_2 < V_1$ → MSB is set to 1

O/P of SAR will be → 1000 (MSB ... LSB)

[Because $(1000)_2 = (8)_{10}$]

Now, $V_2 = 8V$ and $V_1 = 4V$

So $V_2 > V_1$ → Next MSB is set to 1 and first one Reset to zero

O/P of SAR will be → 0100

[Because, $(0100)_2 = (4)_8$, $V_2 = 4V$, $V_1 = 4$]

Now, $V_2 = 4V$ and $V_1 = 4V$

So, $V_2 = V_1$, clock is Disable by control logic and we get 4V as Analog voltage in digital o/p