FPGA ⇒ Field Programmable gate array consist of logic blocks or an array of circuit elements.

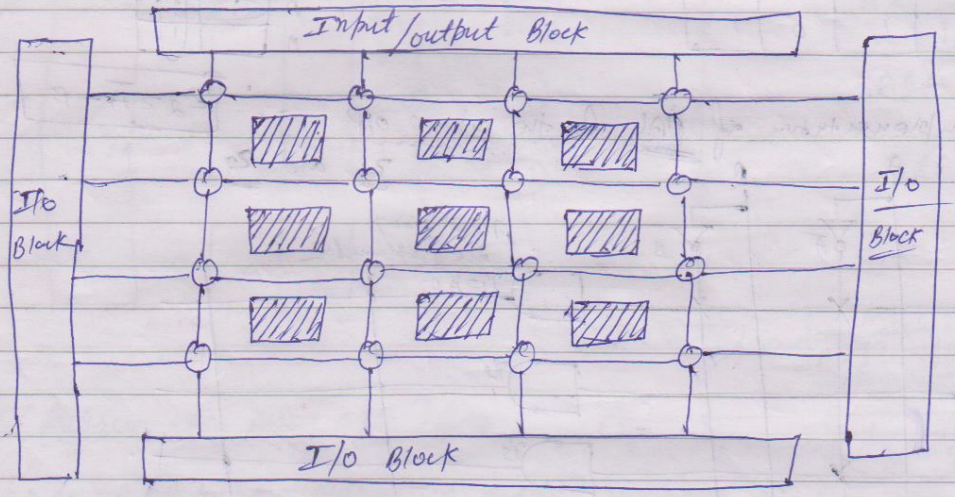
⇒ In FPGA, Programming is done by the customer and not by the manufacturer.

⇒ FPGA structure is a two dimensional array of logic blocks interconnected by vertical and horizontal wires.

⇒ SRAM or antifuse are used as switches for interconnection of blocks.

FPGA's are used to implement large logic circuits because of their very high logic densities.

→ A typical structure of FPGA is shown below, consist with number of independent configurable logic block (CLB), configurable I/O blocks and programmable interconnecting switches.



Structure of Field Programmable Gate Array

⇒ FPGA is an eg. of SPD (Sequential Programmable Devices), PLD are the combinational circuit having gates only, but SPD are the devices having gates as well as flip flop and

FPGA are used in various application such as Communi-
-cation Encoding, Communication filtering, device
Controller

Charge coupled device (CCD) memory

→ CCD was introduced in 1970. It is a sequential memory used to shift and store digital information.

→ It consist with MOS capacitor each cell as dynamic shift register. CCD memory is used bcoz, it is simple accessible and low cost device.

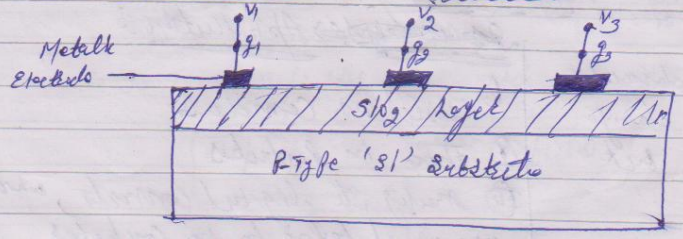
→ In MOS device, a logic '1' is stored if the charge is present in the depletion layer and a logic '0' is stored if the depletion layer is empty.

Operation of CCD's steps are -

1. Digital input is converted into charge.
2. Transfer of charge in sequential manner through various stages.
3. Stored charge is converted into digital signal.

Construction ⇒ CCD is a semiconductor device. It consist with P-type silicon substrate covered with a thin layer of SiO_2 (silicon dioxide). It has closely spaced Metal Electrode (gate). Large number of gates are fabricated closely between source & drain of MOSFET.

→ Each gate electrode and substrate forms MOS capacitor.



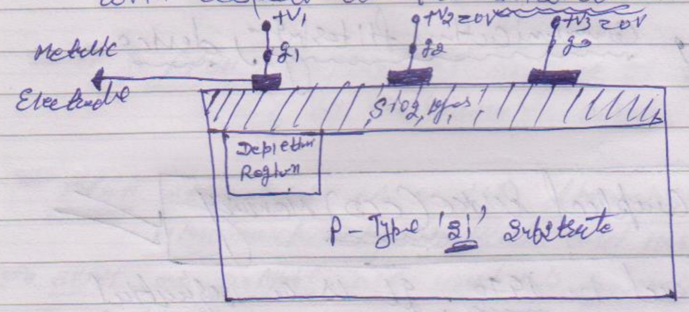
MOSFET without Any N+ type

5cr

(M-14)

Working ⇒

when a positive potential is applied at a gate with respect to the substrate.



MOSFET with positive potential at gate g1.

→ Here '+V1' is applied at gate 'g1', a potential is developed under the gate, and other two gates 'g2' and 'g3' are at zero voltage. A depletion layer is formed below the gate 'g1' in the substrate

⇒ If a negative charge is deposited into depletion region it can move freely with in the depletion region. The -ve charge will be held there as long as positive voltage is applied at the gate 'g1'. It means negative charge is stored, a logic '1' is stored.

In this way CCD store the digital information. It is possible to move the stored charge from left to right by applying voltage at the gate 'g2' and 'g3' in sequence.

→ The clock signal is given to CCD gate for controlling the shifting of charges.

⇒ It is assumed that a logic '1' is stored, when -ve charge is held in the depletion region and a logic '0' is stored when the depletion region is empty.

Advantages ⇒

1. These are low cost devices
2. These are simple to design
3. These have very high bit packing density

~~Disadvantages~~ ⇒ **Application!**

1. used in cameras
2. These in Robots
3. Analog to digital converter, which