Emitter Coupled Logic (ECL)

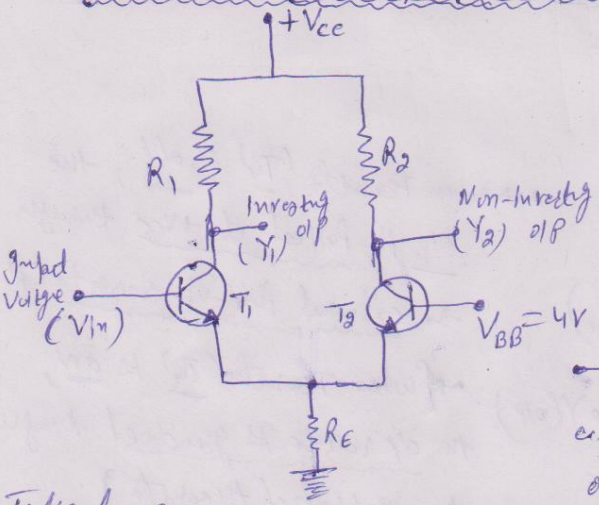
→ ECL is the fastest of all the logic family and used in application where very high speed is essential.

→ In saturated transistor, the major problem arises due to the storage time. It is the time required to derive transistor a transistor out of saturation.

→ ECL is also called "Current Mode Logic".

→ In case of ECL, Transistors are in unsaturated conditions and this overcomes the problem of transistor storage time, and help to increase the speed of ECL family.

⟸ Basic ECL Inverter/Buffer circuit ⟹



→ It consist of Two Transistor T_1 and T_2 connected with common emitter Resistance (R_E) in differential Single Ended Input Mode

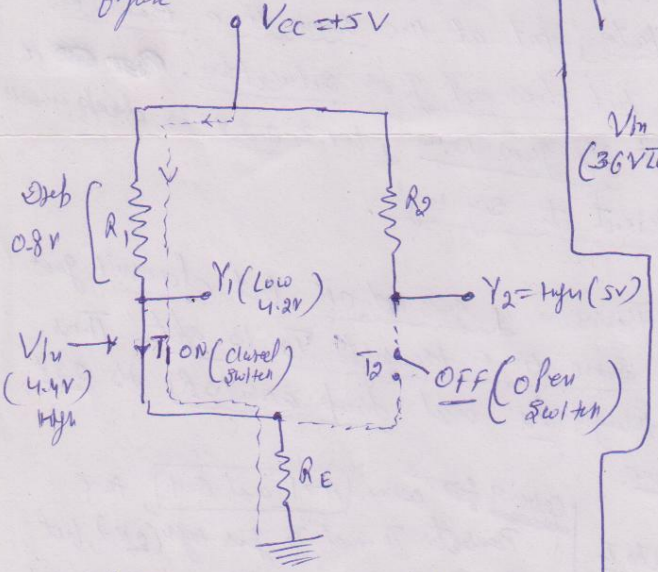
→ It gives two o/ps Y_1 and Y_2 as Inverting and Non-Inverting o/p

Table for ECL Inverter ckt sheet Show the Low and high voltage level for i/p and o/p.

Voltage levels for i/p		Voltage level for o/p	
Low	High	Low	High
3.6 V (Low input)	4.4 V (High input)	4.2 V (Low o/p)	5.0 V (High o/p)

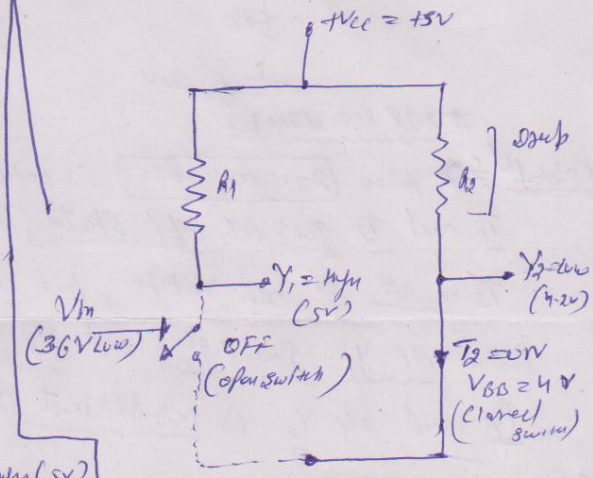
→ when input voltage (V_{in}) is high, i.e (4.4 V), transistor T_1 is ON but does not goes to saturation and at the same time transistor T_2 is off.

→ Due to this, the o/p Y_2 is pulled high (5 V) through Resistor R_2. Also the 0.8 V is drop across Resistor R_1, the o/p Y_1 goes low (4.2) V. It is clear from figure



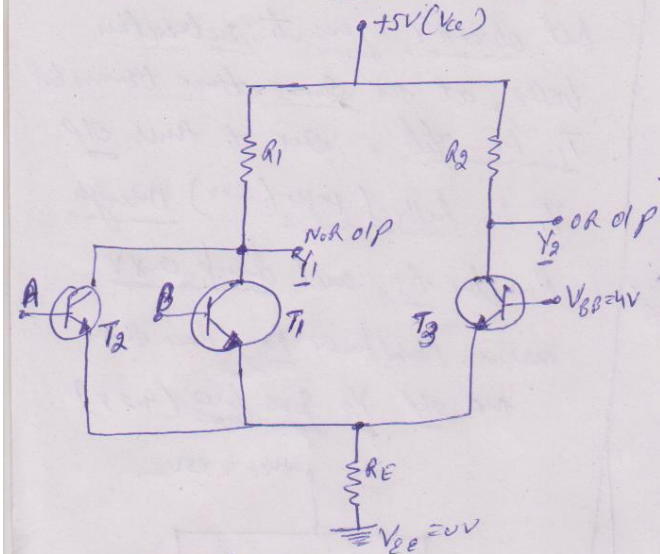
Basic ECL Inverter/Buffer ckt using Switch Representation

→ when input voltage (V_{in}) is low i.e (3.6 V), the transistor T_2 is ON but does not goes to saturation, at the same time transistor T_1 is off. Due to this o/p Y_1 is pulled high (5 V) through Resistor R_1, and drop 0.8 V across Resistance R_2, then the o/p Y_2 goes low (4.2 V)



Basic ECL Inverter/Buffer Circuit using Switching Representation

⇒ Two input ECL OR/NOR Gate : has an additional transistor connected in parallel with input transistor of an ECL inverter.



2-I/P ECL OR/NOR gate

verification by T-Table OR/NOR gates

I/P		O/P's	
A	B	Y_1 (NOR gate)	OR gate
0	0	1	0
0	1	0	1
1	0	0	1
1	1	0	1

Case-1st :⇒ when A=0 and B=0 ∴ Both the inputs are low, The transistors T_1 and T_2 goes into off state, but at the same time transistor T_3 is ON by V_{BB} voltage, but does not goes Saturation. it causes o/p Y_1 goes high and Y_2 goes low ; because 0.8 V is drop across R_2 and o/p Y_2 is insufficient to say high.

Case-2 :⇒ when A=0 & B=1 ∴ The Transistor T_2 goes ON but doesn't goes to Saturation and at the same time transistor T_3 is off. Thus Y_2 (O/P) is Pulled high through R_2 and drop across R_1 is 0.8V so that the O/P Y_1 is low.

Case-3 : when A=1 & B=0 ∴ The Transistor T_2 goes ON but doesn't goes to Saturation because at the same time Transistor T_3 is off. Thus, Y_2 is Pulled high through R_2 and voltage drop across R_1 is 0.8V, so the output Y_1 is Low

∴ A=0, B=1, the O/P Y1=0 & Y2=1

Case-4 :⇒ when A=1 and B=1, the Transistor T_1 and T_2 goes high(ON), but doesn't goes to Saturation and at the same time T_3 is off. Thus Y_2 is Pulled high through R_2 and voltage drop across R_1 is 0.8V, so that the O/P Y_1 is Low.

∴ for A=1 B=1, the O/P Y1=0 & Y2=1