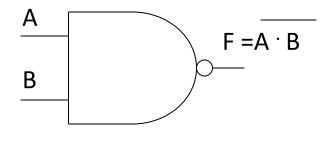
## .Universal Gate

## NAND

Α	В	A · B
0	0	1
0	1	1
1	0	1
1	1	0
1		[



## **NOR**

Α	В	A + B
0	0	1
0	1	0
1	0	0
1	1	0

