Case 3: when $A=B=1$ ∴ Both inputs are high.

Both the Transistor goes into Saturation and output voltage equal to the Saturation voltage (i.e low)

∴ for $A=B=1$, $Y=0$

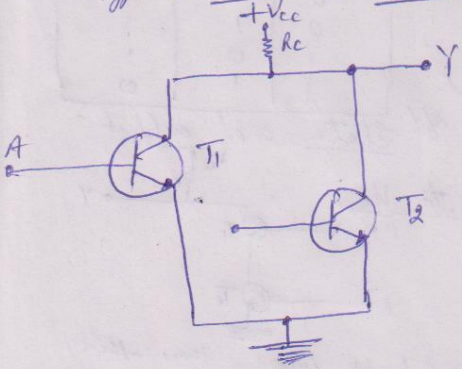
Verification by Truth Table of NOR gate

Inputs		o/p
A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

DCTL (Direct coupled Transistor logic)

→ Logic gates can be made by direct interconnection of transistor.

→ Typical NOR and NAND gates using DCTL are shown below:



DCTL NOR Gate

Input		output
A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

Verification by Truth Table of NOR gate

Case 1st: when $A=0, B=0$ ∴ Both inputs are Low. So NOR gate both Transistor T_1 and T_2 goes into cut off state and o/p goes to high.

∴ $A=B=0$, $Y=1$ ∴ Because No current flow through Rc and drop across Rc is zero.

Case-2nd : when A=0 and B=0 or A=1 and B=0 } ∴ one input is high, then corresponding transistor goes to Saturation and other transistor goes to cut off where input is Low. This increases the voltage drop across the collector Resistor and decrease the positive output voltage.

output voltage, $V_0 = V_{CE}(Sat)$, i.e 0

∴ for (A=0 and B=1 or A=1 & B=0) so O/P = 0 ✓

Case-3rd : when A=B=1 ∴ both inputs are high. Both Transistor goes to Saturation and o/p voltage is equal to Saturation voltage

∴ A=B=1, Y=0 ✓

DCTL NAND Gate

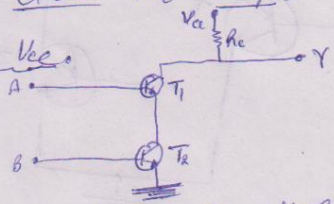
Inputs		outputs
A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

(O/P Remains high when one I/P is Low.)

Operation

Case-1st : when A=B=0, both inputs are Low, both transistor T_1 and T_2 goes to Cut off State and output voltage and output voltage equal to Vcc.

A=B=0, Y=1 ✓



Case-2nd : when (A=0 and B=1 or A=1 and B=0) ∴ Any one input is Low, then the Corresponding transistor goes to cut off State and output voltage equal to Vcc.

Y=1

Case-3rd : when A=B=1 ∴ when both inputes are high, Transistor T_1 & T_2 goes into Saturation State and output voltage is insufficient to consider as "1", Because current flow through Rc, T_1 and T_2, this create a drop across Rc and o/p voltage at Y becomes Low. Y=0 ✓

Q. A gate draws 2.8 mA currents for high o/p and 5.2 mA current for low o/p. Calculate the avg. power dissipation if $V_{cc} = 10V$ and it is operated on a 50% duty cycle

Ans ⇒ The avg. power dissipation is given by:

$$P_{D(avg)} = I_{cc(avg)} \times V_{cc}$$

$$I_{cc(avg)} = \frac{I_{ccH} + I_{ccL}}{2}$$

$$= \frac{2.8 + 5.2}{2} = \frac{8}{2} = 4mA$$

$$\therefore P_{D(avg)} = 4 \times 10^{-3} \times 10$$

$$P_{D(avg)} = 40\ mW$$

Q. Calculate the fan-out of following values of currents are given:

$I_{OL(Max)} = 15mA$

$I_{OH(Max)} = 1mA$

$I_{IL(Max)} = 0.2mA$

$I_{IH(Max)} = 8\mu A$

Ans: fan-out for low state is given by:

$$\text{fan-out (Low)} = \frac{I_{OL(Max)}}{I_{IL(Max)}} = \frac{15 \times 10^{-3}}{0.2 \times 10^{-3}} = \frac{15}{0.2}$$

$$\text{fanout (Low)} = 75$$

⇒ fan-out for high state $\therefore \frac{I_{OH(Max)}}{I_{IH(Max)}} = \frac{1 \times 10^{-3}}{8 \times 10^{-6}} = \frac{125}{1000} \times 8$

$$\text{fan-out (High)} = 125$$

Q. Cal. the Speed-power product for an IC family having avg. power dissipation of 5mW and propagation delay time of 6 nsec.

Ans $SPP = P_d \times P_{D(avg)} = 6 \times 10^{-9} \times 5 \times 10^{-3} = 30$ Pico Joules

$= 30$ (PJ)