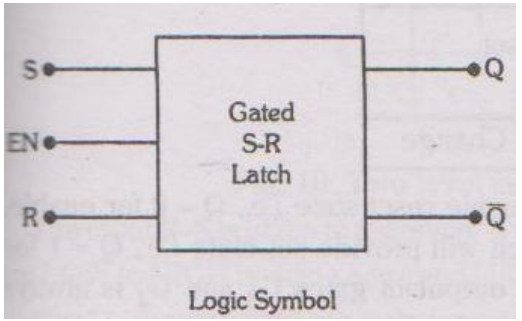
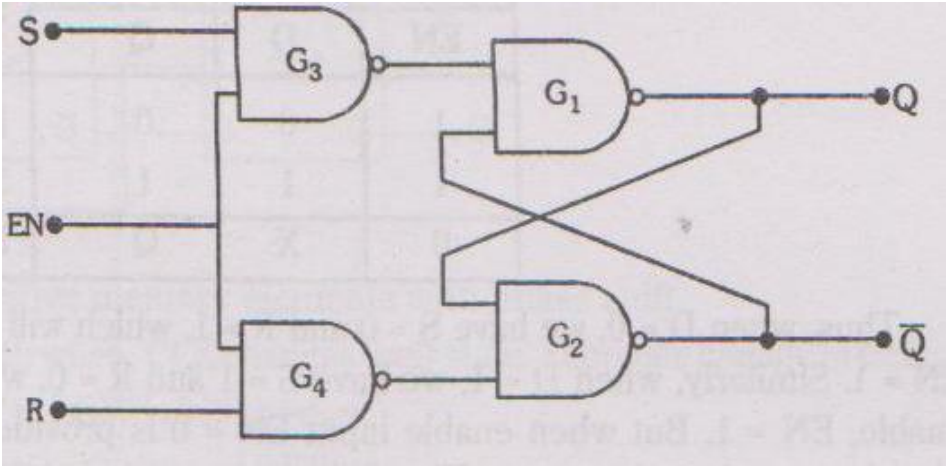
Gated latches(Clocked Flip Flop)

S-R Latch with control input



C = 0 disables all latch state changes
Control signal enables data change when C = 1



C	S	R	Next state of Q
0	X	X	No change
1	0	0	No change
1	0	1	$Q = 0$; Reset state
1	1	0	$Q = 1$; set state
1	1	1	Indeterminate

(b) Function table

Case I : when S = 0 , R = 0

Output of gates **G3 and g4** are always ‘1’ irrespective of clock signal

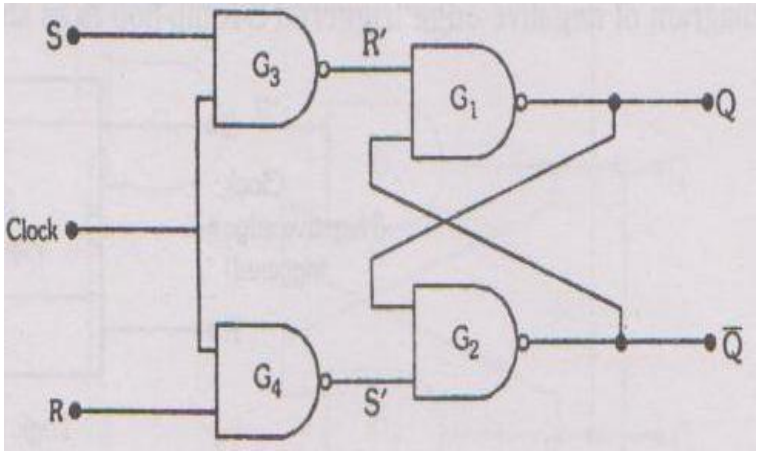
Inputs		Output	
S	R	Q	State
0	0	X	Invalid
0	1	0	Reset
1	0	1	Set
1	1	Q	No Change

Thus ‘1’ is input to gates **G1 and g2** which provides the output for no change

Case II : when S = 0 , R = 1

Output of gates **G3 is** always ‘1’ **and g4** is always ‘0’ irrespective of clock signal

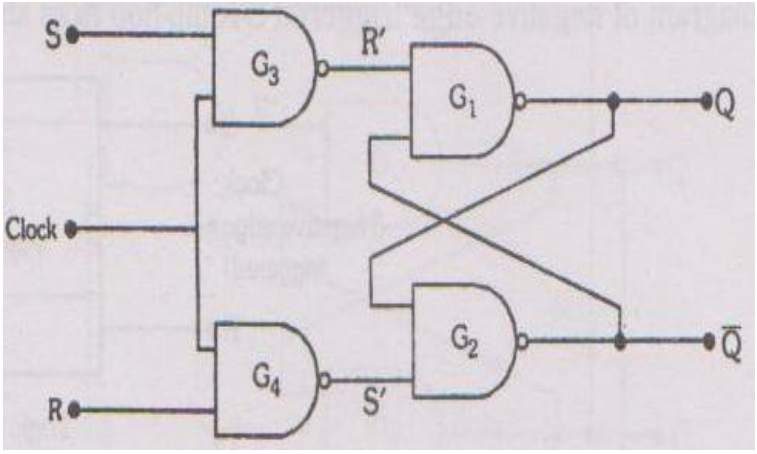
Thus the is input to gates **G1 and g2** are ‘1’ and ‘0’ respectively



Case III : when S = 1 , R = 0

Output of gates **G3 is** always '0' **and g4** is always '1' irrespective of clock signal

Thus the is input to gates **G1 and g2** are '0' and '1' respectively



Case IV : when S = 1 , R = 1

Output of gates **G3 and g4** are always '0' irrespective of clock signal

Thus the is input to gates **G1 and g** are '0' respectively

Inputs			Output	State	
Clk	S	R	Q		
↑	0	0	Q	No Change	Positive Edge Triggered Clock
↑	0	1	0	Reset	
↑	1	0	1	Set	
↑	1	1	X	Invalid	
0	X	X	Q	No Change	Flip-flop is disabled
1	X	X	Q	No Change	
↓	X	X	Q	No Change	