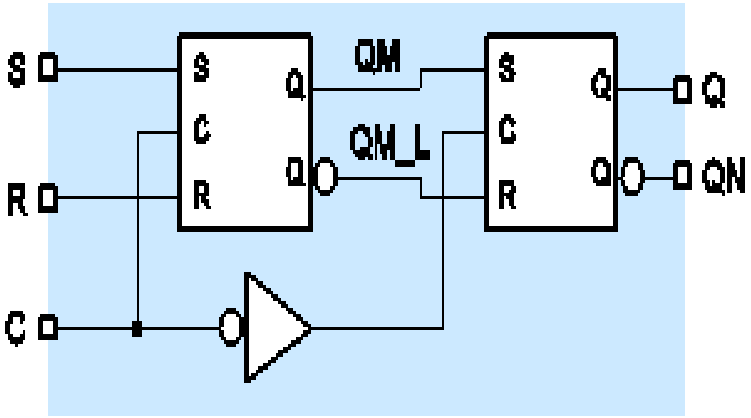
Master/Slave S-R Flip-Flop

- The *postponed output indicator* shows that the output signal does not change until the enable C input is negated.
- Flip-flops with this kind of behavior are called *pulse-triggered* flip-flops.
- Q* = S+R'Q
- SR = 0

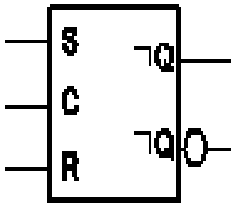
(a)



(b)

S	R	C	Q	QN
x	x	0	last Q	last QN
0	0	⊓	last Q	last QN
0	1	⊓	0	1
1	0	⊓	1	0
1	1	⊓	undef.	undef.

(c)

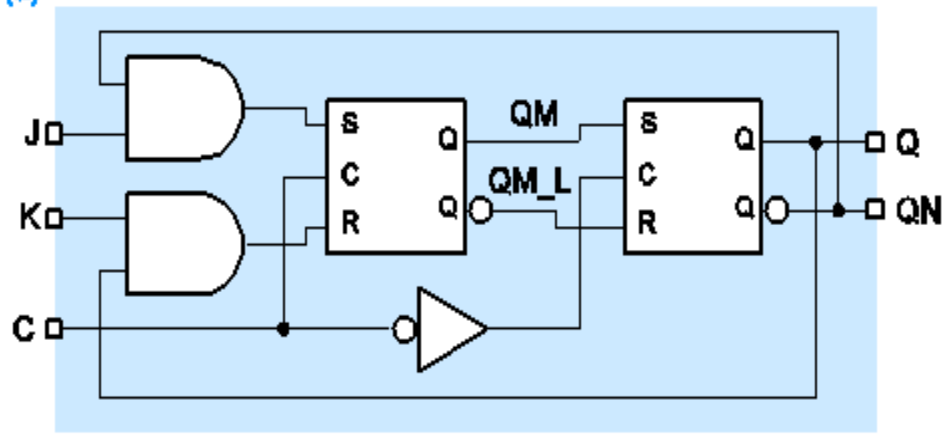


Master/Slave J-K Flip-Flop

- The J and K inputs of the J-K flip-flop are analogous to the S and R inputs of the S-R flip-flop,

- except in the case where J=K=1. In this case the outputs of the J-K flip-flop will toggle to the opposite state.

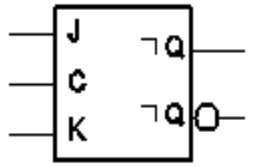
(a)



(b)

J	K	C	Q	QN
x	x	0	last Q	last QN
0	0	⊓	last Q	last QN
0	1	⊓	0	1
1	0	⊓	1	0
1	1	⊓	last QN	last Q

(c)



Master-Slave D Flip Flop

Consider two latches combined together
Only one *C* value active at a time
Output changes on falling edge of the clock

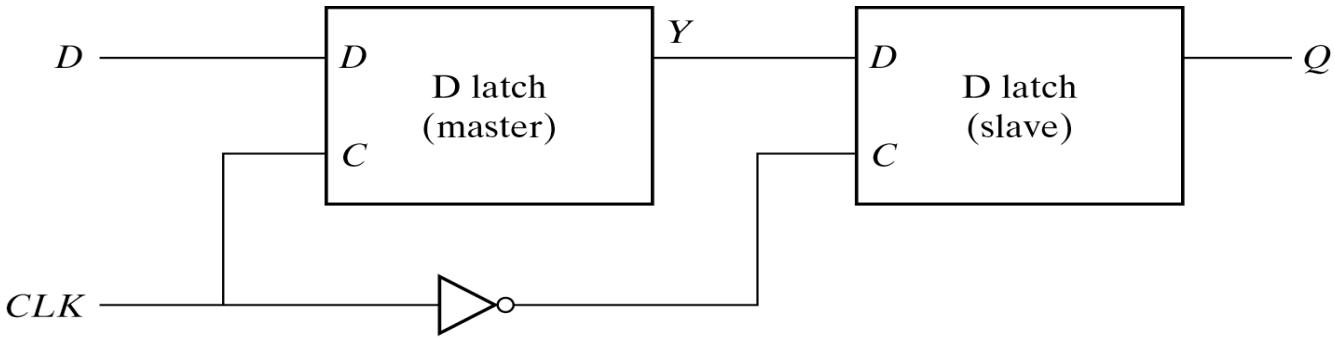


Fig. 5-9 Master-Slave *D* Flip-Flop