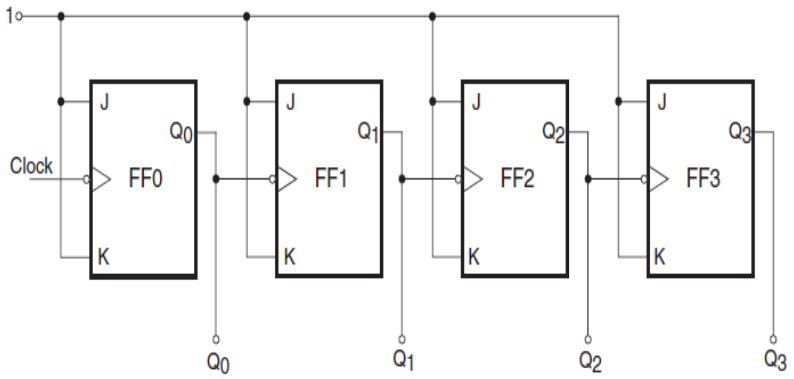
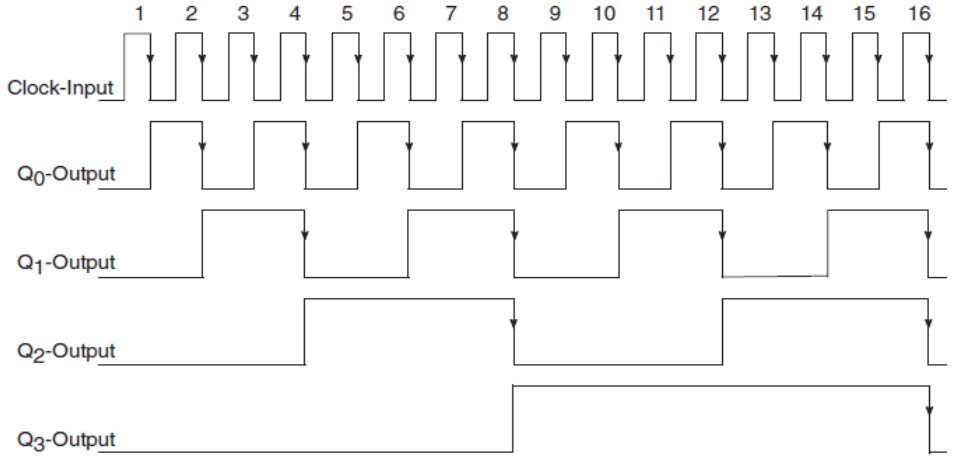
Modulus of a Counter

Binary Ripple Counter – Operational Basics

- The operation of a binary ripple counter can be best explained with the help of a typical counter of this type.
- Figure shows a four-bit ripple counter implemented with negative edge-triggered J-*K* *flip-flops wired as toggle flip-flops.*

- The output of the first flip-flop feeds the clock input of the second, and the output of the second flip-flop feeds the clock input of the third, the output of which in turn feeds the clock input of the fourth flip-flop.
- The outputs of the four flip-flops are designated as Q0 (LSB flip-flop), Q1, Q2 and Q3 (MSB flip-flop).

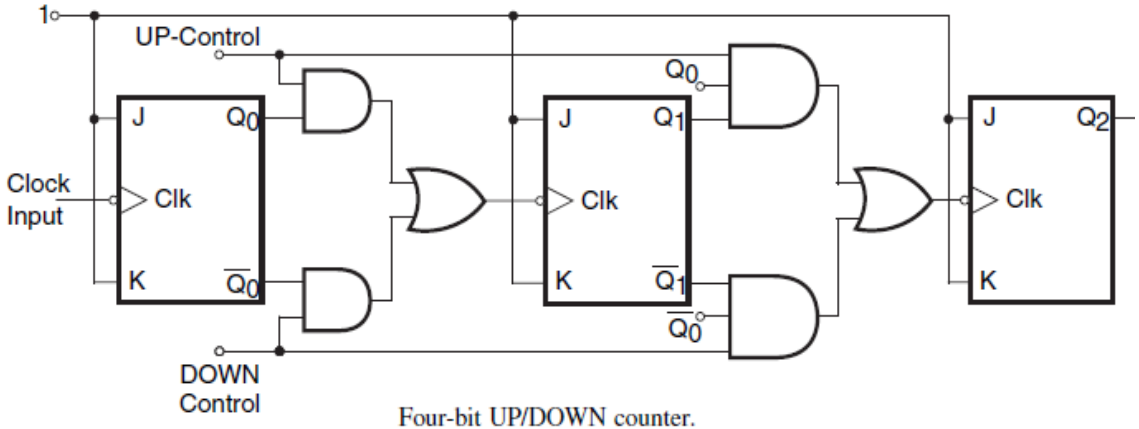




UP/DOWN Counters

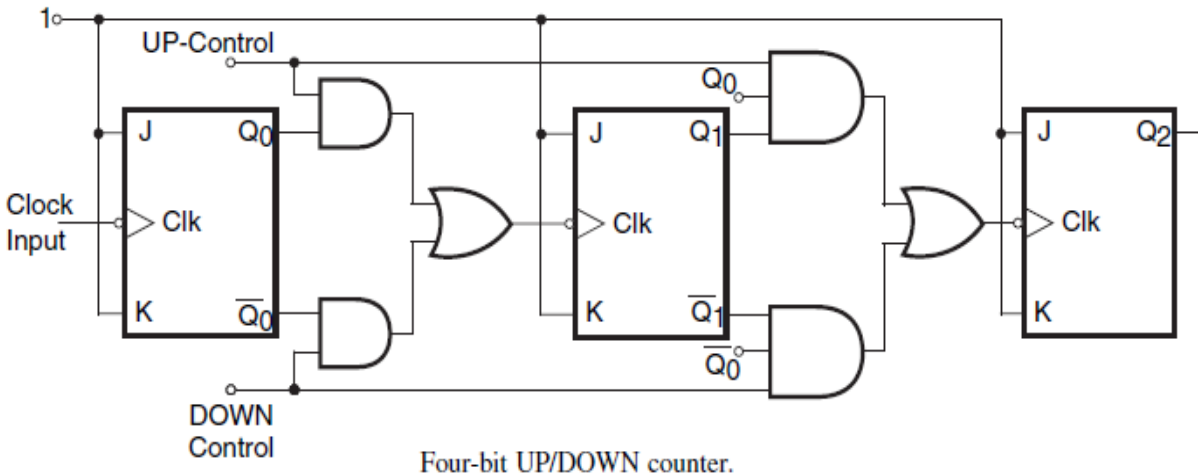
- Counters are also available in integrated circuit form as UP/DOWN counters, which can be made to operate as either UP or DOWN counters.
- UP counter is one that counts upwards or in the forward direction by one LSB every time it is clocked.
- A four-bit binary UP counter will count as 0000, 0001, 0010, 0011, 0100, 0101, 0110, 0111, 1000, 1001, 1010, 1011, 1100, 1101, 1110, 1111, 0000, 0001, and so on.

- DOWN counter counts in the reverse direction or downwards by one LSB every time it is clocked. The four-bit binary DOWN counter will count as 0000, 1111, 1110, 1101, 1100, 1011, 1010, 1001, 1000, 0111, 0110, 0101, 0100, 0011, 0010, 0001, 0000, 1111



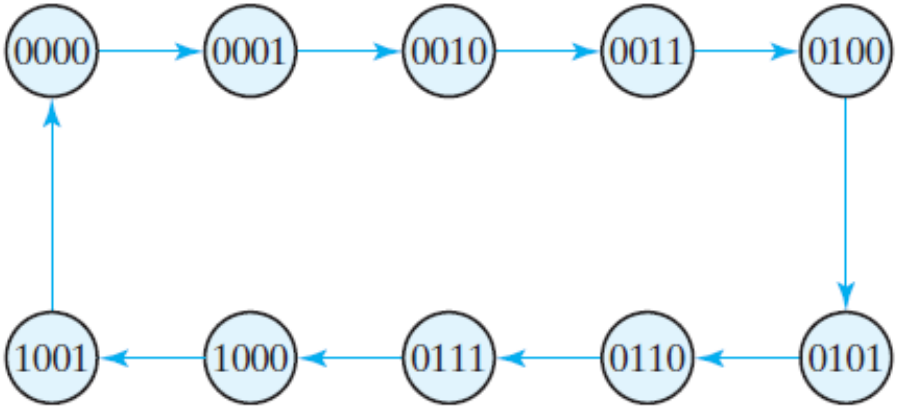
Four-bit UP/DOWN counter.

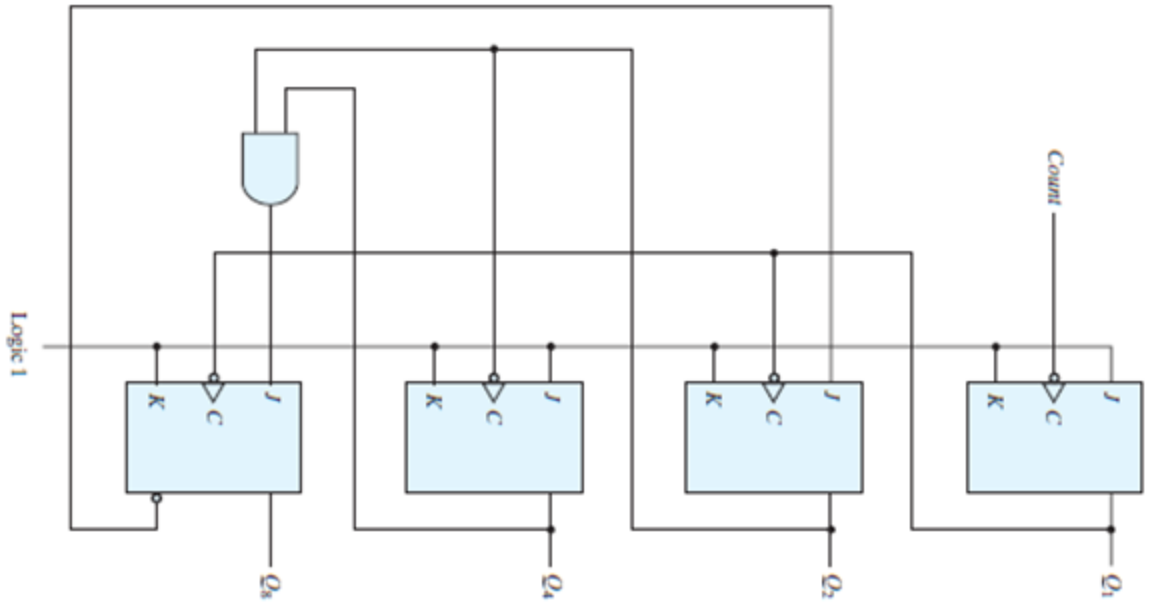
- shows a three-bit binary UP/DOWN counter. This is only one possible logic arrangement. As we can see, the counter counts upwards when UP control is logic ‘1’ and DOWN Control is logic ‘0’.
- In this case the clock input of each flip-flop other than the LSB flip-flop is fed from the normal output of the immediately preceding flip-flop. The counter counts downwards when the UP control input is logic ‘0’ and DOWN control is logic ‘1’.



Four-bit UP/DOWN counter.

BCD Counter: State Diagram





Qn	Qn+1		J	K
0	0		0	X
0	1		1	X
1	0		X	1
1	1		X	0

Table 11.12 Example 11.9.

Present state			Next state					Inputs			
C	B	A	C	B	A	J_C	K_C	J_B	K_B	J_A	K_A
0	0	0	0	1	0	0	X	1	X	0	X
0	0	1	0	0	0	0	X	0	X	X	1
0	1	0	1	0	1	1	X	X	1	1	X
0	1	1	0	0	0	0	X	X	1	X	1
1	0	0	0	0	0	X	1	0	X	0	X
1	0	1	1	1	0	X	0	1	X	X	1
1	1	0	0	0	0	X	1	X	1	0	X
1	1	1	0	0	0	X	1	X	1	X	1

Solution

- The number of flip-flops required is three.
- Table 11.12 shows the desired circuit excitation table.
- The Karnaugh maps for J_A, K_A, J_B, K_B, J_C and K_C are shown in Figs 11.30(a) to (f) respectively.
- The simplified Boolean expressions are as follows:

$$J_A = B.\overline{C}$$

$$K_A = 1$$

	$\overline{A}$	A
$\overline{C}\overline{B}$		X
$\overline{C}B$	1	X
CB		X
$C\overline{B}$		X

(a)

	$\overline{A}$	A
$\overline{C}\overline{B}$	X	1
$\overline{C}B$	X	1
CB	X	1
$C\overline{B}$	X	1

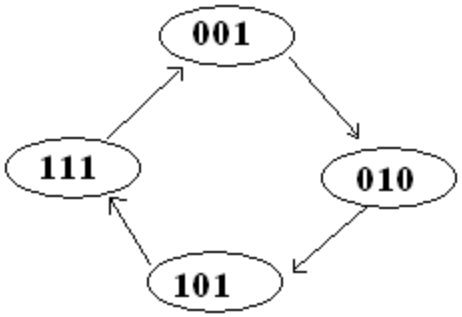
(b)

$$J_B = A.C + \overline{A}.\overline{C}$$

	$\overline{A}$	A
$\overline{C}\overline{B}$	1	
$\overline{C}B$	X	X
CB	X	X
$C\overline{B}$		1

(c)

Example



Qn	Qn +1		J	K
0	0		0	X
0	1		1	X
1	0		X	1
1	1		X	0

P.S				N.S		
Q2	Q1	Q0		Q2	Q1	Q0
0	0	1		0	1	0
0	1	0		1	0	1
1	0	1		1	1	1
1	1	1		0	0	1

J_{Q2}	K_{Q2}
0	x
1	x
x	0
x	1

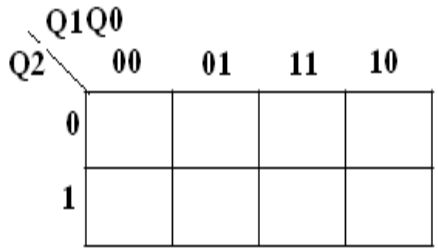
J_{Q1}	K_{Q1}
1	x
x	1
1	x
x	1

J_{Q0}	K_{Q0}
x	1
1	x
x	0
x	0

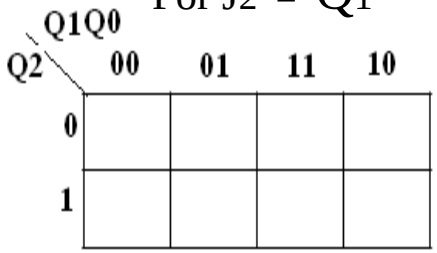
P.S				N.S			J_{Q2}	K_{Q2}	J_{Q1}	K_{Q1}	J_{Q0}	K_{Q0}
Q2	Q1	Q0		Q2	Q1	Q0						
0	0	1		0	1	0	0	x	1	x	x	1
0	1	0		1	0	1	1	x	x	1	1	x
1	0	1		1	1	1	x	0	1	x	x	0
1	1	1		0	0	1	x	1	x	1	x	0

Step 4: drown the K map

For J_{Q2} and K_{Q2}

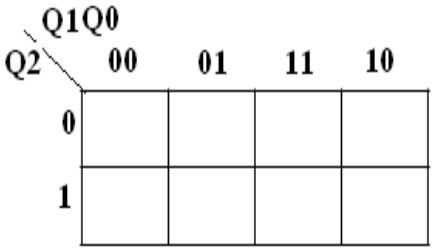


For $J_2 = Q_1$

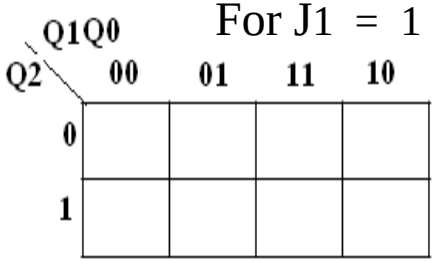


For $K_2 = Q_1$

For J_{Q1} and K_{Q1}

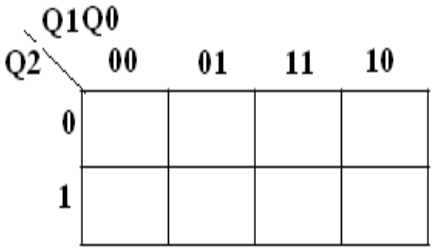


For $J_1 = 1$

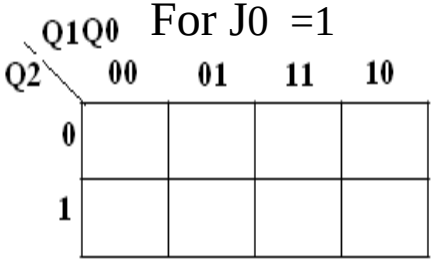


For $K_1 = 1$

For J_{Q0} and K_{Q0}



For $J_0 = 1$



For $K_0 = Q'_2$

Step 5

$J_0 = 1, \quad K_0 = Q'_2$

$J_1 = 1, \quad K_1 = 1$

$J_2 = Q_1, \quad K_2 = Q_1$

Step 6: drown the circuit diagram