PLD (Programmable Logic Devices) ⇒

are Special type of IC's, used by the user and are programmed before use.

→ Different type of logic fn" can be implemented by using Single programmed chip of PLD's.

PLD can be Reprogrammed because these are based on Re-writable memory technologies.

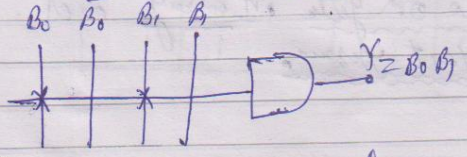
⇒ When number of AND gate are used together they formed AND Array, & when number of OR gate are used to-gether they formed OR Array.

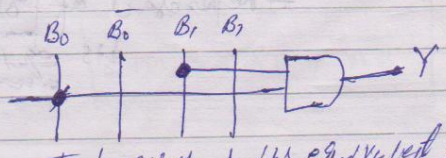
A PLD Contains OR Arrays, AND Arrays, and various types of buffers.

→ fuse link technique is used to programmed the PLD by the user, depending upon the type of PLD to be manufactured.

AND MATRIX or AND Array ⇒ These gives the logical Product terms. I/P of input buffers are connected to AND gate to get the desired O/P in the product terms

→ 'X' sign shows the fuse link, inter connection. If 'X' is not present, then it shows the off fuse.

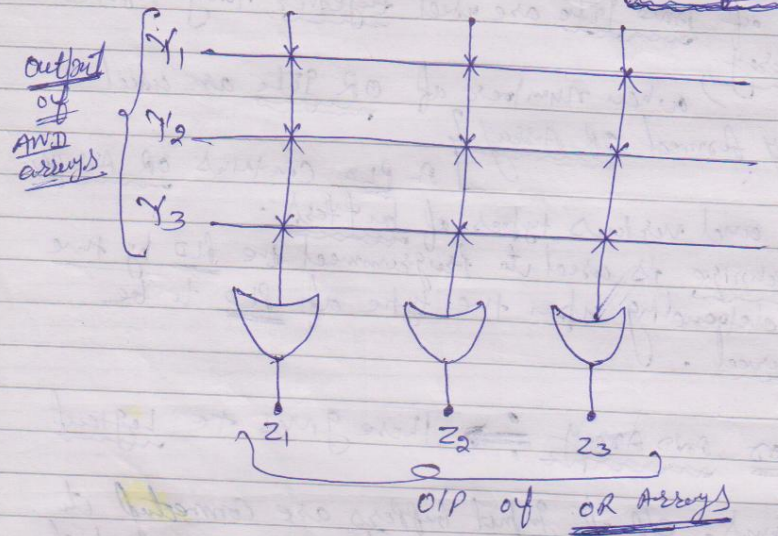




Below depiction of single AND gate in Array is its equivalent form

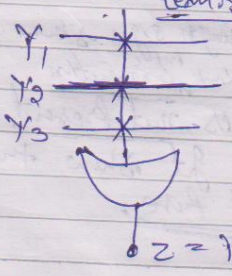
⇒ O/P of $Y = B_0 B_1$, bcoz fuse link 'x' is present at B_0 and B_1 input buffers. The output of AND gate is $B_0 B_1$.

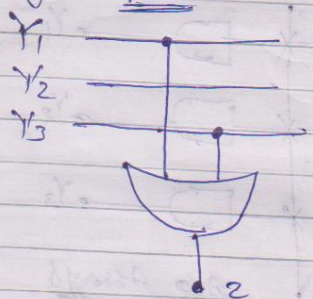
OR MATRIX or OR Array ⇒ These gives the logical Sum terms of output from AND arrays.



OR Arrays

→ AND Arrey are giving product terms, OR Arrays gives Sum terms in the logical form.





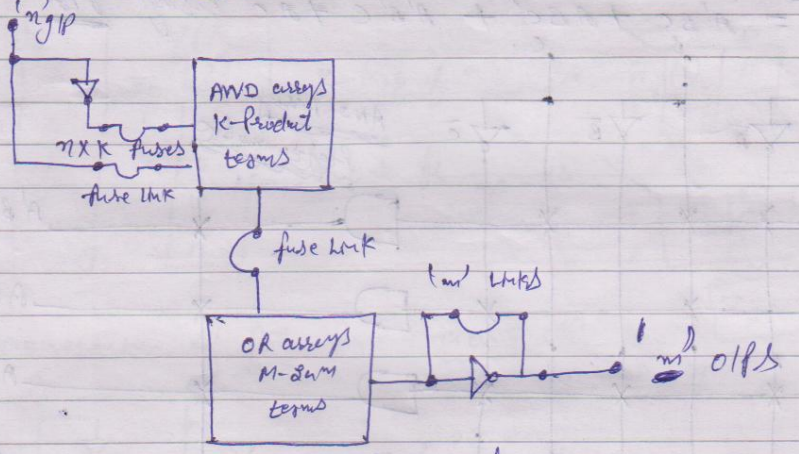
Represent of Style OR gate in arrey and its equivalent terms.

Types of PLD

① PLA (Programmable Logic Array) ② PAL (Programmable Array Logic)
③ FPGA (Field Programmable Gate Array).

PLA (Prog. Logic Array) ⟹ In PLA both AND gate and OR gate are programmable. The AND gate and OR gates are fixed in number for any PLA chip. It depend upon the number of inputs and output of PLA.

Block Diagram of PLA:



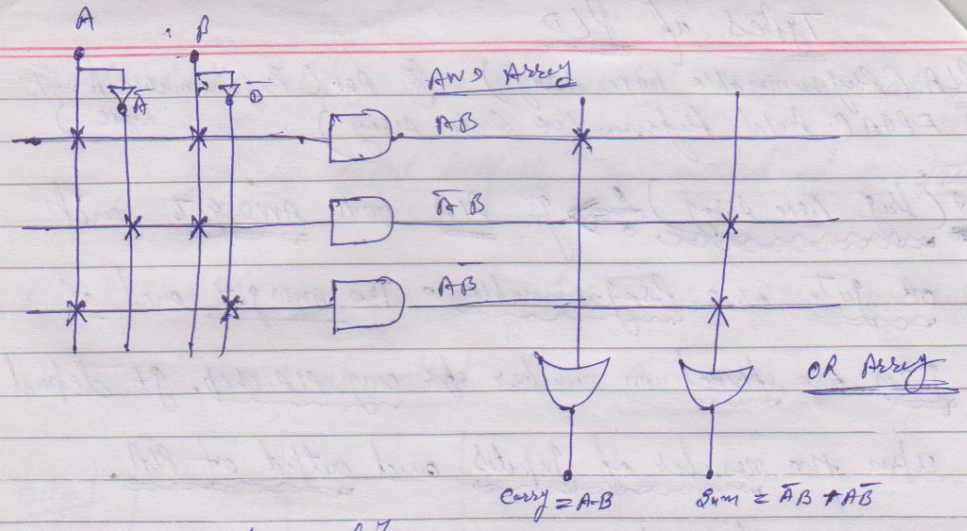
Block Diagram of PLA

for eg. design an Half adder can be done using a PLA.

Input		Outputs	
A	B	Carry	Sum
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

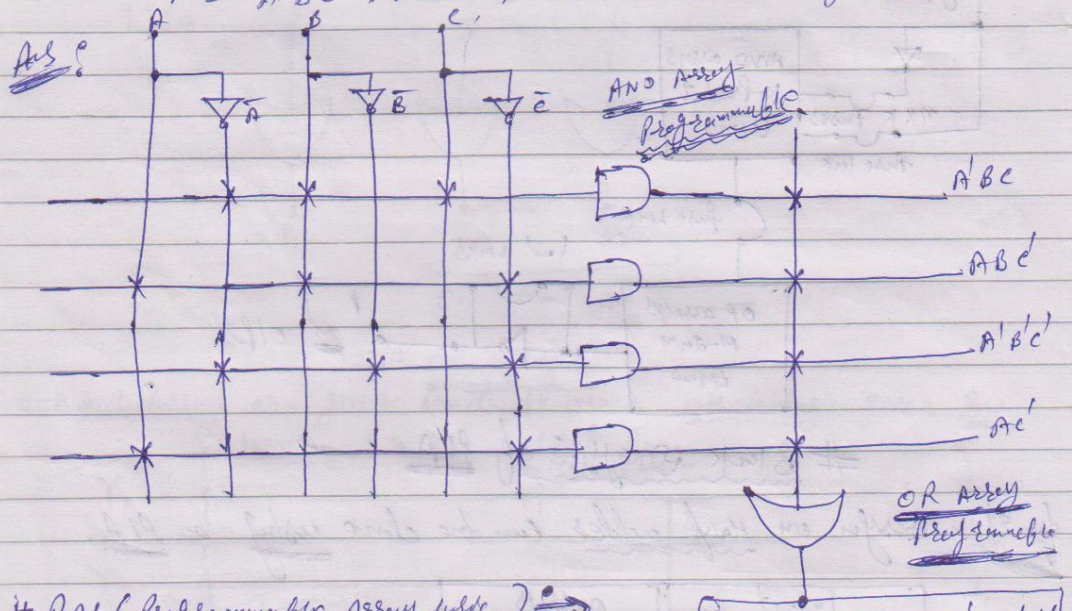
Carry = A·B

Sum = $\bar{A}B + A\bar{B}$



Q- Implement the fn' $F = A'BC + AB\bar{C} + A'B'C + A\bar{C}$ using PLA

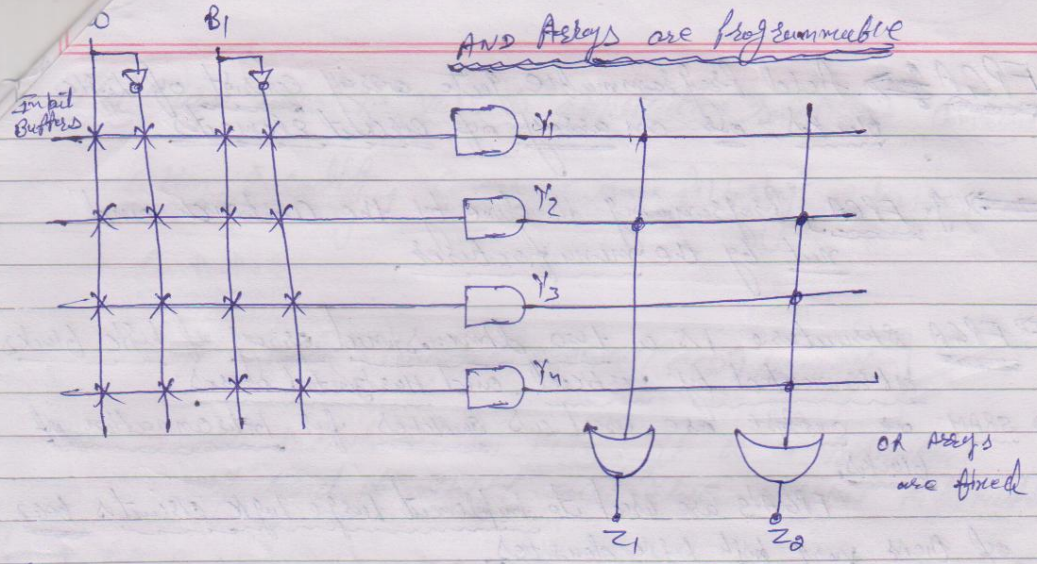
Ans:



PAL (Programmable Array Logic) ⟹

In PLA → AND & OR both are Programmable, But in case of PAL, the Prog. AND Arrays and fixed OR Array are used. This is the only difference b/w PLA and PAL.

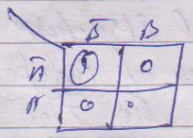
Due to this reason, PAL is more flexible and faster in speed as compare to PLA



Eg: T.T is given for any fn. and PAL can be implemented

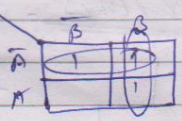
I/P		O/P	
A	B	Z_1	Z_2
0	0	1	1
0	1	0	1
1	0	0	0
1	1	0	1

K-Map for Z_1 is



$Z_1 = \bar{A}\bar{B}$

K-Map for Z_2 is



$Z_2 = \bar{A} + B$

Implementation of PAL for the above O/P Z_1 and Z_2