GATE Question

February 5, 2024

1. Consider a 4-bit counter constructed out of four flip-flops.It is formed by connecting the J and K inputs to logic high and feeding the Q output to the clock input of the following flip-flop (see the figure).The input signal to the counter is a series of square pulses and the change of state is triggered by the falling edge.At time t=t0 the outputs are in logic low state (Q0 = Q1 = Q2 = Q3 = 0).Then at t=t1,the logic state of the outputs is (GATE-PH2020,30)

   (a) Q0 = 1, Q1 = 0, Q2 = 0 and Q3 = 0

   (b) Q0 = 0, Q1 = 0, Q2 = 0 and Q3 = 1

   (c) Q0 = 1, Q1 = 0, Q2 = 1 and Q3 = 0

   (d) Q0 = 0, Q1 = 1, Q2 = 1 and Q3 = 1

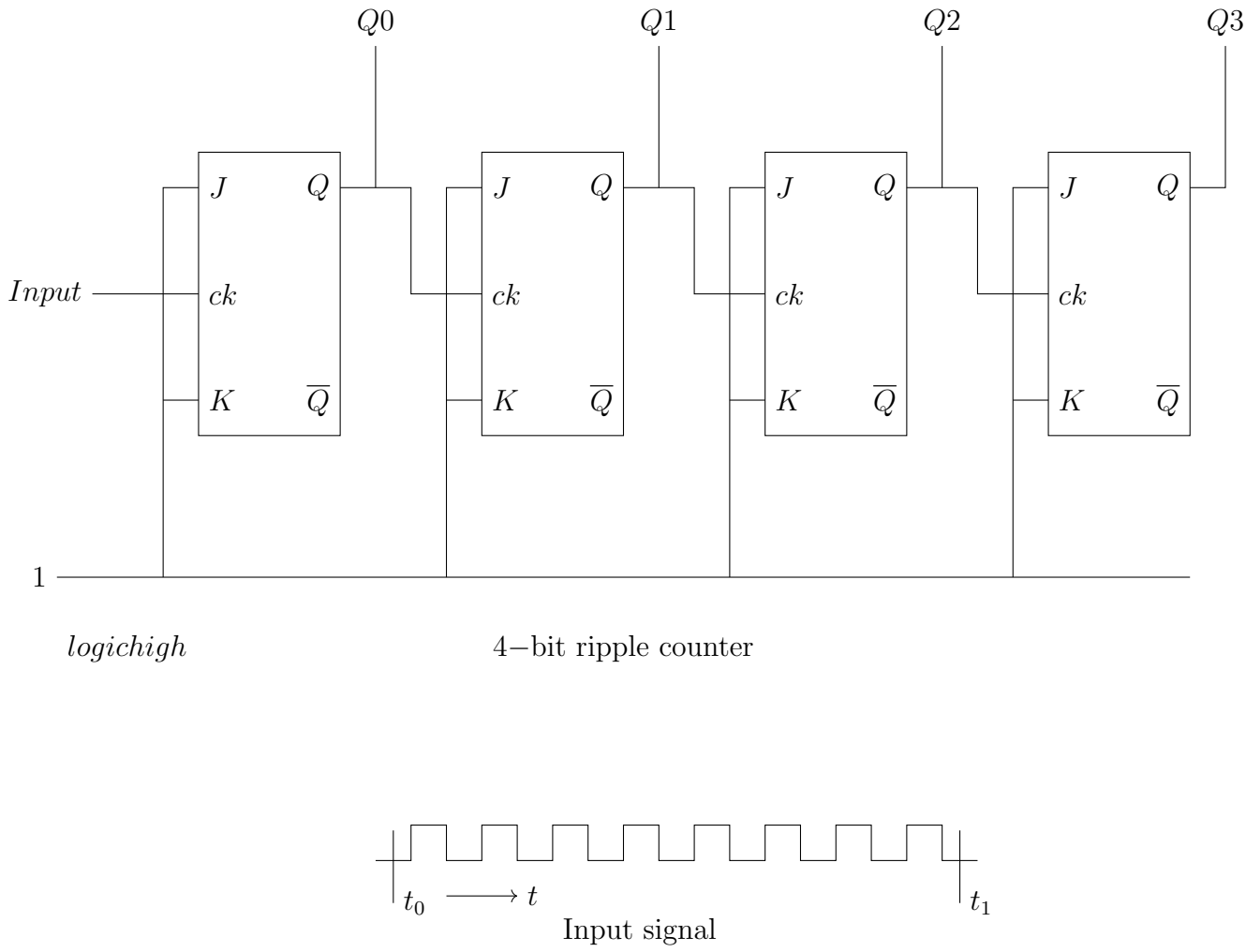

Figure 1: Ripple Counter