ELECTRONIC PRINCIPLES AND DEVICES

Department of Electronics and Communication Engineering

ELECTRONIC PRINCIPLES AND DEVICES

Course Content

Department of Electronics and Communication.

Electronic Principles and Devices

Course Content

Unit 1: Semiconductor DIODE

Unit 2: Diode applications

Unit 3: Transistors and Operational Amplifiers

Unit 4: Digital Electronics

Electronic Principles and Devices - UNIT 1

- Semiconductor diode under Forward and Reverse bias
- Shockley's equation
- Zener and Avalanche breakdown
- Temperature effects
- Ideal versus Practical diode
- Diode resistances
- Diode equivalent circuits

- Series diode configurations
- Parallel and Series-Parallel configurations
- Logical operations using diode
- Diode Clippers and Clampers
- **Hardware Lab:** Diode characteristics, Clipper and Clamper circuits.

Electronic Principles and Devices

UNIT 2

- Block diagram of regulated power supply
- Half-wave, Full-wave and bridge rectifier, Ripple factor and Peak inverse voltage derivations
- Shunt capacitor filter-working, output waveform and ripple factor equation.
- Zener diode characteristics
- Zener diode voltage regulator

Electronic Principles and Devices

UNIT 3

- Transistors: Construction, operation
- Transistor configurations - Common base and common emitter configurations – input and output characteristics.
- Transistor amplifying action.
- Limits of operation, Operating point.
- Biasing circuits: Fixed bias, Emitter bias, Voltage divider bias
- Bias circuit design, Bias stabilization
- Single stage CE Amplifier.

Electronic Principles and Devices

UNIT 3

- **Op-Amp:** Introduction, Op-Amp Basics
- Ideal voltage transfer curve
- Op-Amp parameters and its values for Op-Amp 741 – Input and output offset voltages, Input and output resistances, GBW, SR, CMRR (Definitions and significance only), Ideal Op-amp
- Negative feedback.
- Practical Op-Amp circuits: Inverting Amplifier, Non-inverting Amplifier, Voltage follower, Summing Amplifier, Constant Gain Amplifier, Voltage Subtraction, Integrator, Differentiator.
- **Simulation Experiments** on BJT and Op-amp

Electronic Principles and Devices

UNIT 4

- Number Systems – binary and hexadecimal
- Binary Addition and Subtraction
- 2’s complement subtraction
- Boolean Algebra
- Logic gates
- Basic Theorem and Properties of Boolean Algebra
- Boolean Functions

Electronic Principles and Devices

UNIT 4

- Canonical and Standard Form
- Other Logical Operations
- Combinational Logic Circuits & Sequential Logic Circuits
- Half Adder and Full adder
- Sequential Circuits: Flip-Flops-RS, D, T, JK
- Registers: SISO
- Counters: 3Bit Synchronous and Asynchronous counter

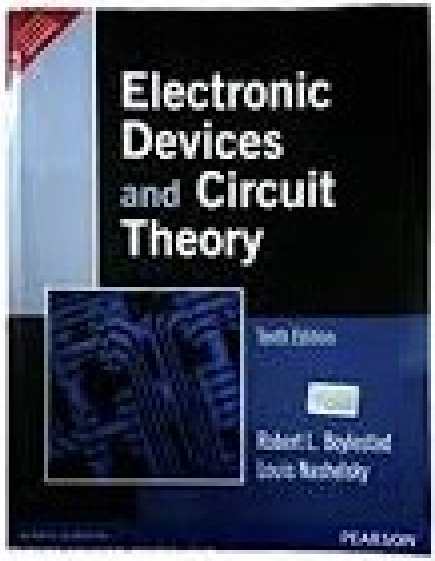
Electronic Principles and Devices

UNIT 4

- Introduction to Embedded Systems: Definition, Block Diagram of Embedded System
- Characteristics of Embedded Systems
- General Purpose and domain specific processors
- Applications of Embedded Systems
- **Hardware Lab using Digital Trainer kit:** TT Verification of Logic Gates, Adders

- Text book for UNIT 1, 2 and 3

http://www.rtna.ac.th/departments/elect/Data/EE306/Electronic%20Devices%20and%20Circuit%20Theory.pdf

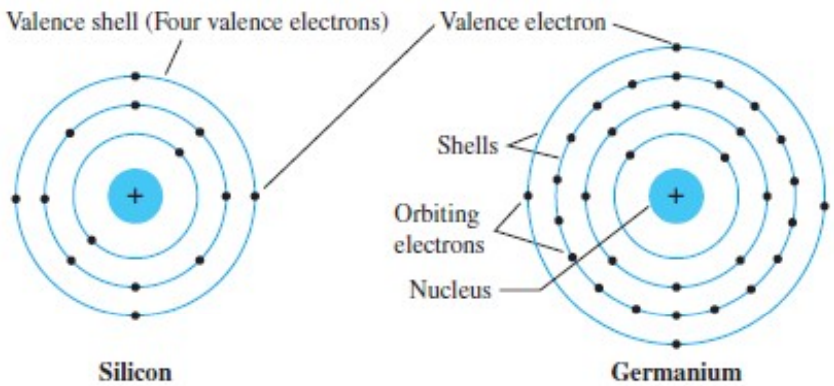


ELECTRONIC PRINCIPLES AND DEVICES

Unit 1 - Introduction to Electronics and Semiconductor Diodes

ELECTRONIC PRINCIPLES AND DEVICES

Introduction to Semiconductors

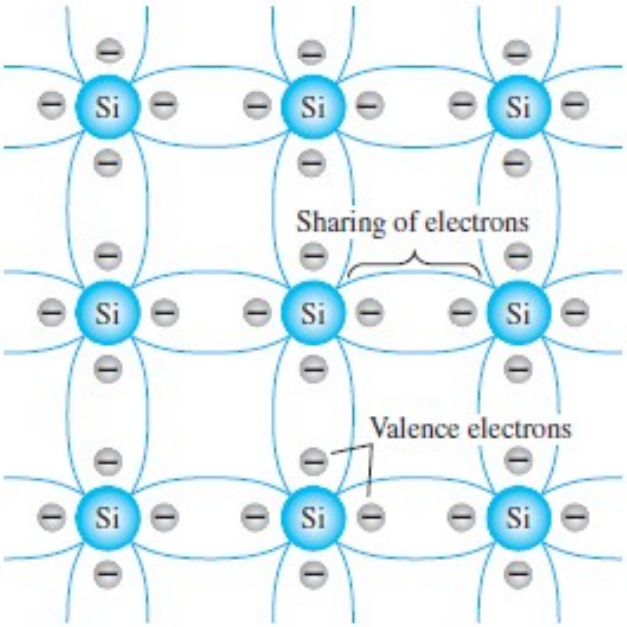


atomic number of silicon=14

$1s^2 2s^2 2p^6 3s^2 3p^2$

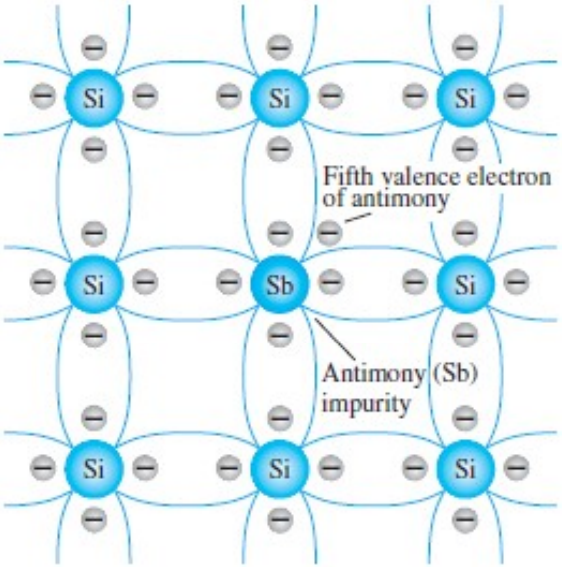
atomic number of germanium=32

$1s^2 2s^2 2p^6 3s^2 3p^6 3d^{10} 4s^2 4p^2$.

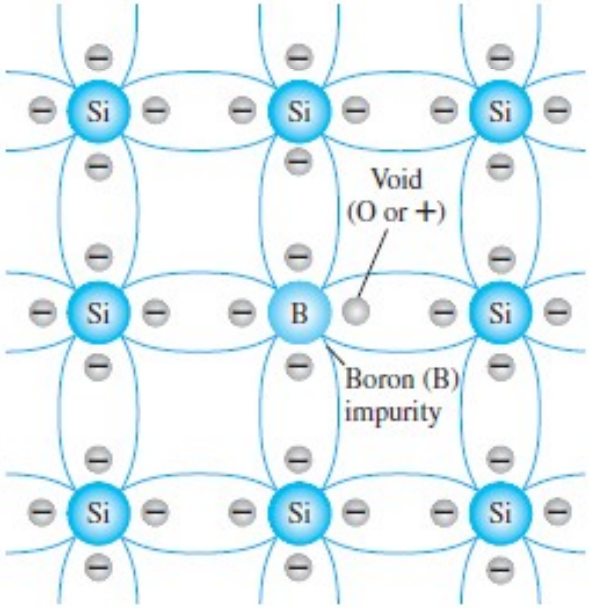


ELECTRONIC PRINCIPLES AND DEVICES

Introduction to Semiconductors



An *n -type material is created by introducing impurity elements that* have *five valence electrons (pentavalent), such as antimony , arsenic , and phosphorus.*

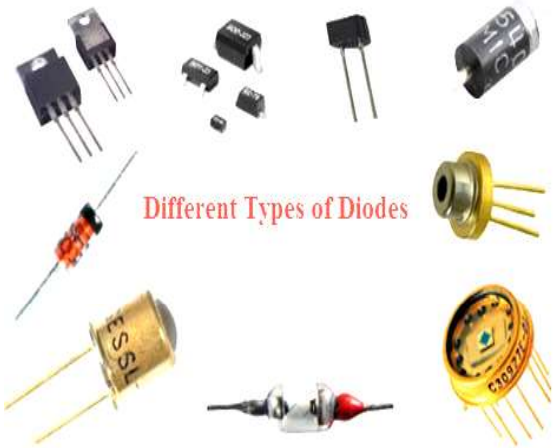


The *p-type material is formed by doping with impurity* atoms having *three valence electrons(trivalent) such as boron , gallium , and indium.*

An Introduction to Semiconductor Diode

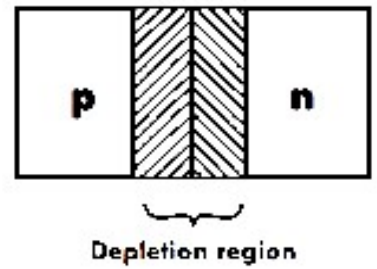
Diode : Two – electrodes

- p-type and n-type material sandwiched together to form a depletion region between the two.
- Semiconductor diode may be either of Silicon or Germanium material

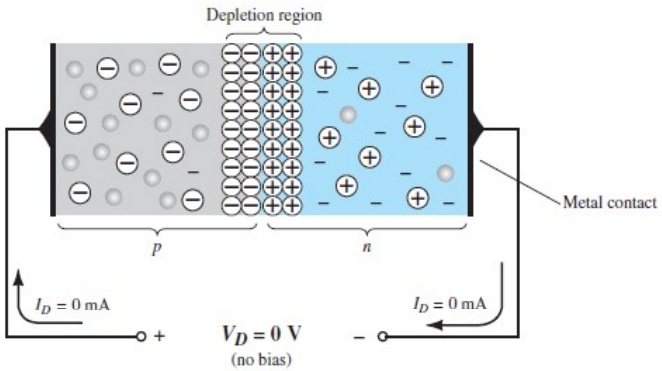


Biasing of diodes :

- Forward Bias: A material type connected to the same polarity terminal of the voltage source
- Reverse Bias: A material type connected to the opposite polarity terminal of the voltage source



Diode under different biasing conditions



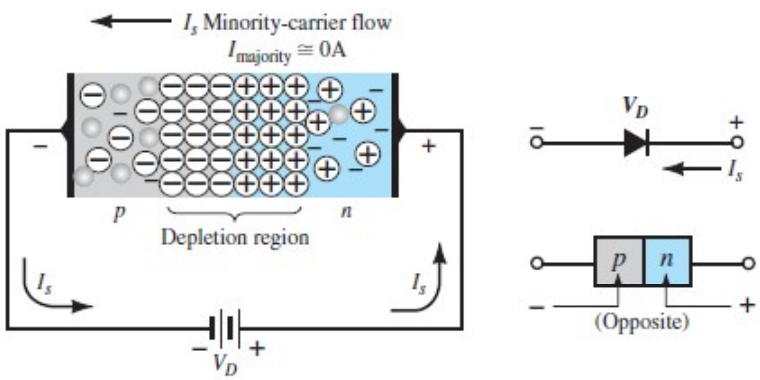
No bias

In the absence of an applied bias across a semiconductor diode, the net flow of charge in one direction is zero.

No – bias condition:

- At the instant the two materials are "joined" the electrons and the holes in the region of the junction will combine, resulting in a lack of free carriers in the region near the junction, as shown in Fig.
- Note in Fig. that the only particles displayed in this region are the positive and the negative ions remaining once the free carriers have been absorbed.
- ***This region of uncovered positive and negative ions is called the depletion region due to the "depletion" of free carriers in the region.***

Diode under different biasing conditions



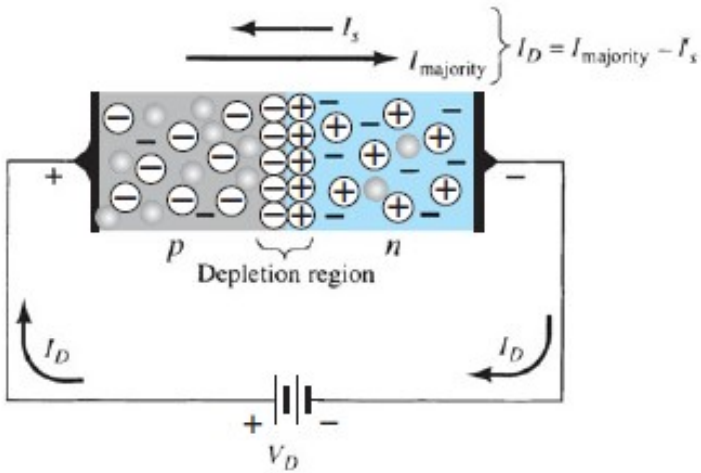
Reverse Bias

The current that exists under reverse-bias conditions is called the reverse saturation current and is represented by Is.

Reverse – bias condition:

- When a pn junction is reverse-biased as shown in Fig., the number of uncovered positive ions in the depletion region of the *n*-type material will increase due to the large number of free electrons drawn to the positive potential of the applied voltage.
- For similar reasons, the number of uncovered negative ions will increase in the *p*-type material.
- The net effect, therefore, is a widening of the depletion region. This widening of the depletion region will establish too great a barrier for the majority carriers to overcome, effectively reducing the majority carrier flow to zero.

Diode under different biasing conditions



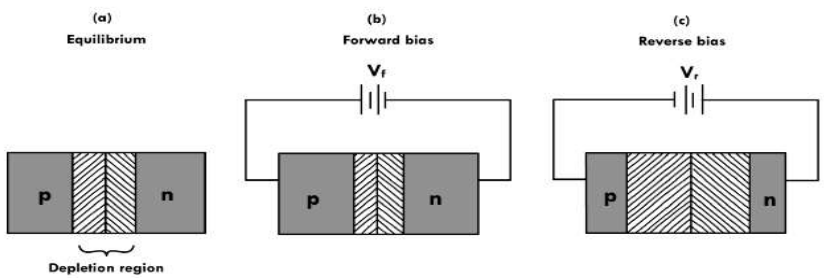
Forward Bias

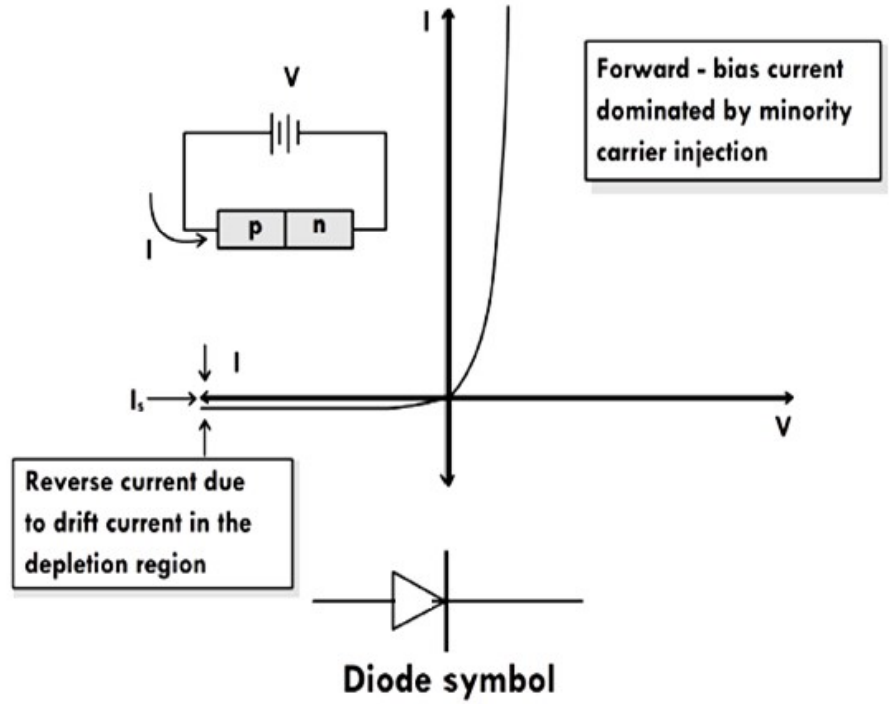
Forward – bias condition

- A *forward-bias* or "on" condition is established by applying the positive potential to the *p*-type material and the negative potential to the *n*-type material as shown in Fig.
- The application of a forward-bias potential V_D will "pressure" electrons in the *n*-type material and holes in the *p*-type material to recombine with the ions near the boundary and reduce the width of the depletion region as shown in Fig.

Semiconductor Diode – Forward & Reverse Characteristics

- **Knee voltage** (Vk) is also known as **cut- in** voltage. The minimum voltage across the diode for it to start conducting is known as knee voltage or cut in voltage.
- The forward voltage at which the current through PN junction starts increasing rapidly is known as knee voltage.





Diode's Current Expression (Shockley's Current Equation)

Shockley's Equation also called the **diode equation** helps us determine the current at a given temperature knowing the diode voltage and saturation current

$$I_D = I_S\left(e^{\frac{qV_D}{nkT}} - 1\right)$$

k = 1.380 649 x10^-23 Joule/Kelvin.

q=1.602176634 × 10^{-19} **coulomb**

- When V_D is negative

$$I_D \sim -I_S$$

- When V_D is positive

$$I_D \sim I_S e^{\frac{qV_D}{nkT}}$$

Where

I_D and V_D are the diode current and voltage, respectively

q is the charge on the electron

n is the ideality factor: n = 1 for indirect semiconductors (Si, Ge, etc.)
n = 2 for direct semiconductors (GaAs, InP, etc.)

k is Boltzmann's constant

T is temperature in Kelvin

Diode's Current Expression (Shockley's Current Equation)

$$I_D = I_S\left(e^{\frac{qV_D}{nkT}} - 1\right)$$

k = 1.380 649 . 10^-23 Joule/Kelvin.

q=1.602176634 × 10^{-19} coulomb

kT/q is also known as V_{th}, the thermal voltage. At 300K (room temperature), kT/q = 25.9mV

EXAMPLE 1.1 At a temperature of 27°C (common temperature for components in an enclosed operating system), determine the thermal voltage V_T.

Solution: Substituting into Eq. (1.3), we obtain

$$T = 273 + °C = 273 + 27 = 300\text{ K}$$

$$V_T = \frac{kT_K}{q} = \frac{(1.38 \times 10^{-23}\text{ J/K})(30\text{ K})}{1.6 \times 10^{-19}\text{ C}}$$

$$= 25.875\text{ mV} \cong 26\text{ mV}$$

Q. No 1 Calculate the thermal voltage when the temperature is 25°C

Solution:

k = 1.380 649 x10^-23 Joule/Kelvin.

Thermal voltage $V_T = k\,T/q$

q=1.602176634 × 10^{-19} coulomb

Where k is the Boltzmann constant and q is the charge of electron. This can be reduced to

$$I_D = I_S\left(e^{\frac{qV_D}{nkT}} - 1\right)$$

$V_T = T/11600$ q/k=11600

Therefore, $V_T = 298/11600 = 0.0257V$

$V_T = 25.7mV$

Q.No.2 Calculate the forward bias current of a Si diode when forward bias voltage of 0.4V is applied, the reverse saturation current is 1.17×10^{-9}A and the thermal voltage is 25.2mV.

Solution: $I_D = I_s(e^{V_D/\eta V_T} - 1)$; I_s = reverse saturation current

$$I_D = I_S\left(e^{\frac{qV_D}{nkT}} - 1\right)$$

η = ideality factor, V_T = thermal voltage, V_D = applied voltage

Since in this question ideality factor is not mentioned it can be taken as one.

$I_s = 1.17 \times 10^{-9}$A, $V_T = V_T = k\,T/q = 0.0252$V, η = 1, $V_D = 0.4$V

Therefore, $I_D = 1.17\times10^{-9} \times (e^{0.4/0.0252} - 1)$

I_D= 9.156mA.

Numerical on Diode's Current Equations

Q. No 3 Given a diode current of 8 mA and n=1, find the reverse saturation current (Is) if the applied voltage is 0.5 V and the room temperature is 25°C.

Solution: Equation for diode current (Shockley's Equation) $I_D = I_s(e^{V_D/nV_T} - 1)$

Given: I_D = **diode current = 8 mA**, η = ideality factor = 1, V_D = Applied voltage = 0.5V

Find V_T = Thermal voltage and Reverse saturation current I_s

$$V_T = \frac{kT_K}{q} = \frac{(1.38 \times 10^{-23}\ \text{J/K})(25°\text{C} + 273°\text{C})}{1.6 \times 10^{-19}\ \text{C}}$$

$$= 25.70\ \text{mV}$$

$$8\text{mA} = I_s(e^{(0.5\text{V})/(1)(25.70\ \text{mV})} - 1) = I_s(28 \times 10^8)$$

$$I_s = \frac{8\ \text{mA}}{2.8 \times 10^8} = \mathbf{28.57\ pA}$$

Numerical on Diode's Current Equations

Q. No 4: Calculate the applied voltage V_D, if diode current is 6 mA, Thermal Voltage is 26 mV, Ideality factor is 1, and Reverse saturation current is 1 nA.

Solution: **Given:** I_D = 6 mA, V_T = 26 mV, η = 1, I_S = 1 nA, V_D = Applied voltage = ...V

Equation for diode current (Shockley's Equation)

$$I_D = I_s(e^{V_D/\eta V_T} - 1)$$

$$6\text{ mA} = 1\text{ nA}(e^{V_D/(1)(26\text{ mV})} - 1)$$

$$6 \times 10^6 = e^{V_D/26\text{ mV}} - 1$$

$$e^{V_D/26\text{ mV}} = 6 \times 10^6 - 1 \cong 6 \times 10^6$$

$$\log_e e^{V_D/26\text{ mV}} = \log_e 6 \times 10^6$$

$$\frac{V_D}{26\text{ mV}} = 15.61$$

$$V_D = 15.61(26\text{ mV}) \cong \mathbf{0.41\text{ V}}$$

Q. No 5 Consider a silicon diode with η=1.2. Find change in voltage if the current changes from 0.1mA to 10mA.

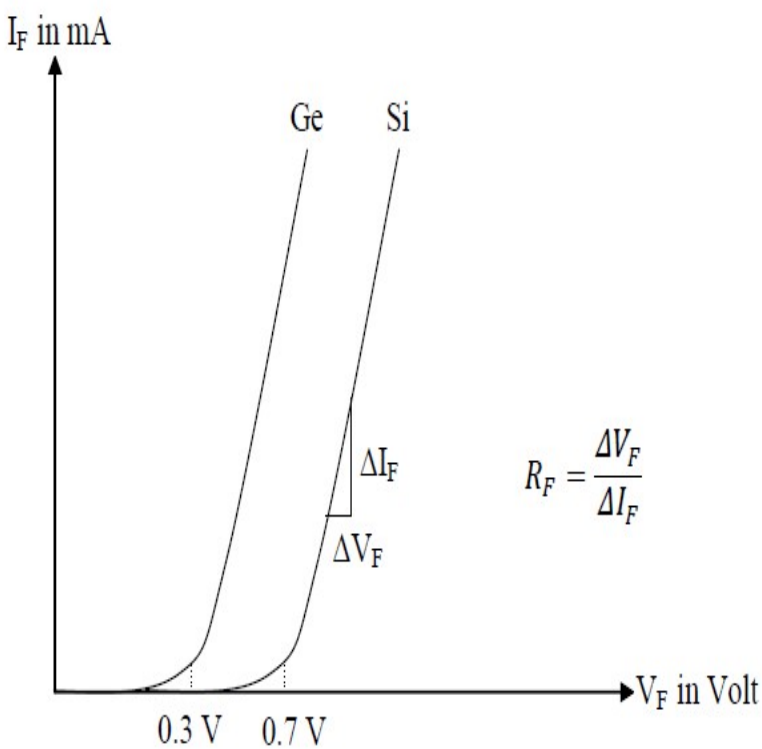
Solution: Equation for diode current $I=I_0\times(e^{(V/\eta V_T)}-1)$

Where I_0 = reverse saturation current, η = ideality factor
V_T = thermal voltage, V = applied voltage

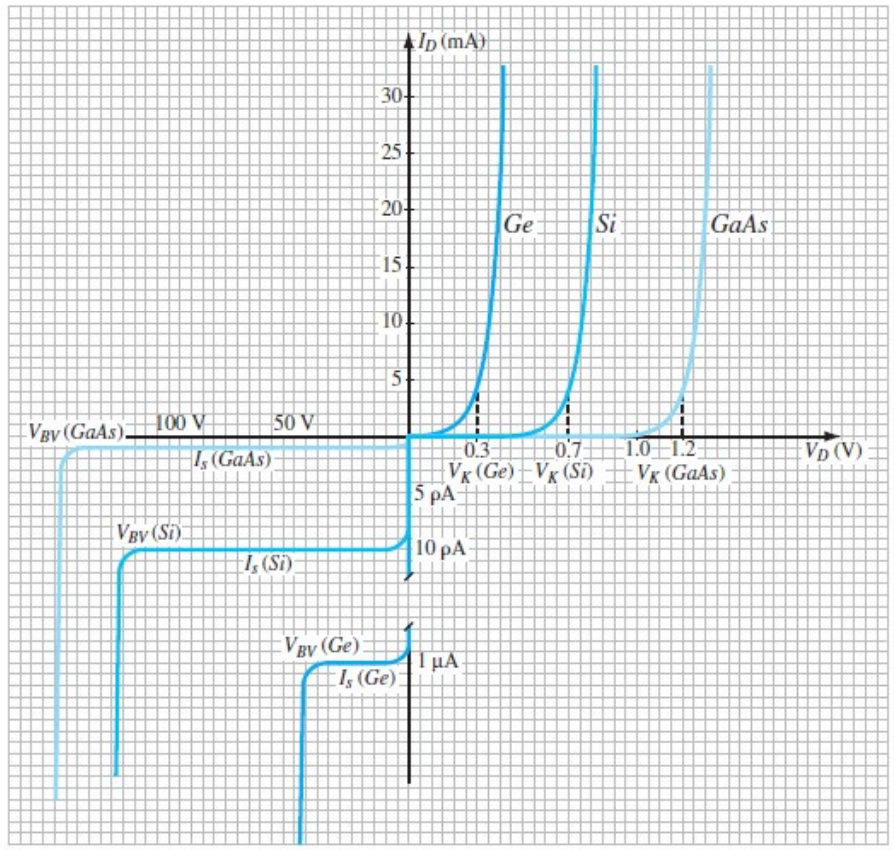
η = 1.2, I_2 = 10mA, I_1 = 0.1mA and take V_T = 0.026V

$$\text{Change in voltage } \Delta V = \eta V_T \ln\left(\frac{I_2}{I_1}\right) = 1.2\text{x}0.026\text{x}\ln\left(10 \times \frac{10^{-3}}{0.1\times10^{-3}}\right) = 0.143\text{V}$$

Diode's Current Expression (Shockley's Current Equation)



$$R_F = \frac{\Delta V_F}{\Delta I_F}$$



Semiconductor Diode's Characteristics & Parameters

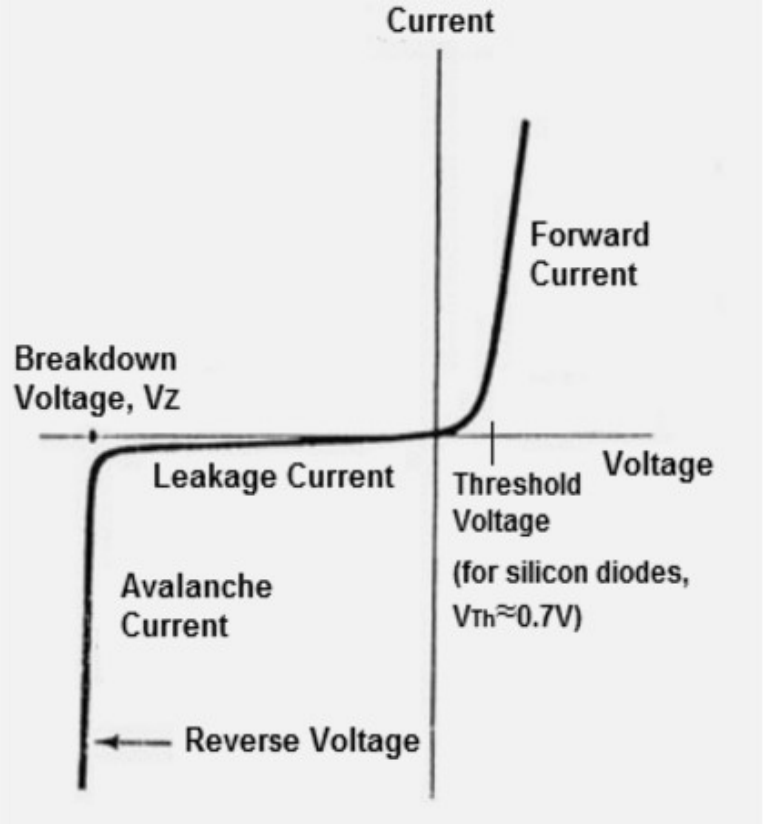
From the characteristics curve of a semiconductor diode the following parameters have been observed under,

Forward Bias

- Knee Voltage
- Forward Current Rating
- Maximum Power Dissipation

Reverse Bias

- Reverse Saturation Current
- Break down Voltage
- Peak Inverse Voltage Rating

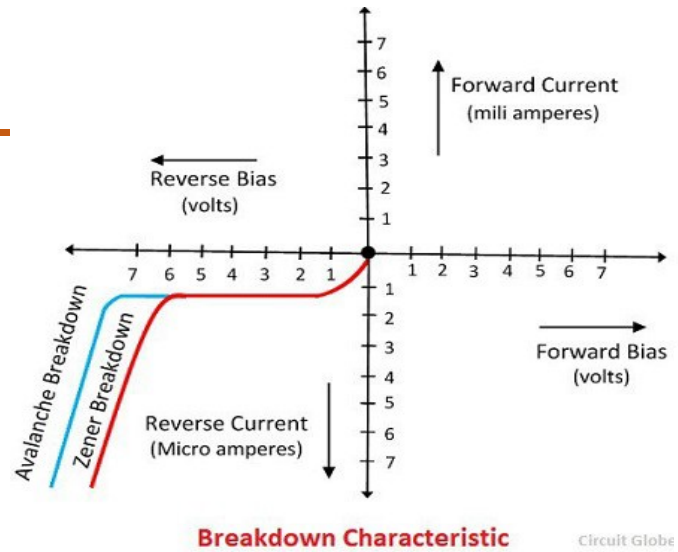


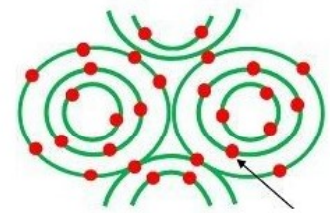
Types of Diode Breakdown

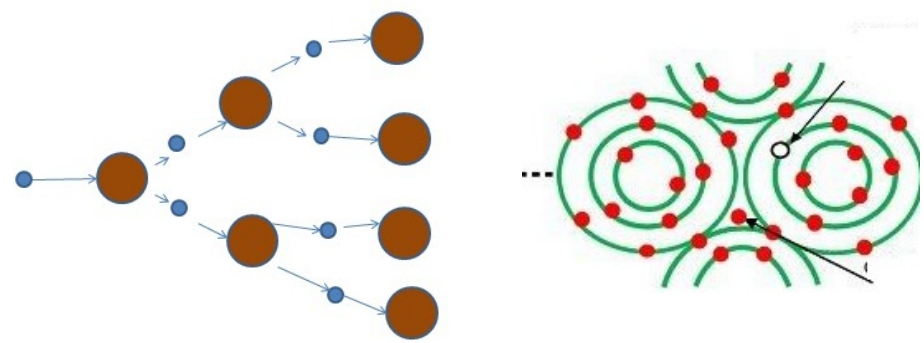
Avalanche breakdown : In the reverse bias condition as the voltage increases the free charge carriers obtain velocity and associated kinetic energy and release additional carriers through collision with other atomic structures.

Hence Covalent bonds are broken and electron–hole are generated.

These charge carriers acquire energy from the applied potential and produce more and more free charge carriers. This cumulative process is called Avalanche multiplication or ionization process.







Carrier Multiplication or avalanche breakdown

Types of Diode Breakdown

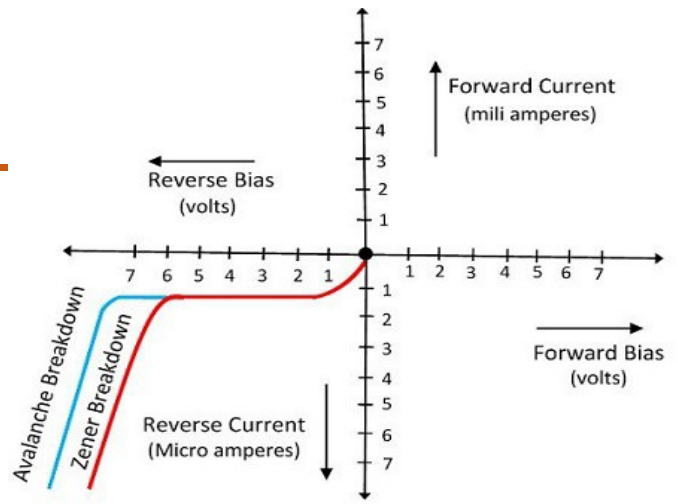
Zener breakdown :

Zener break down occurs when both P and N type material are heavily doped in a semiconductor diode.

Hence the depletion layer region is narrow down.

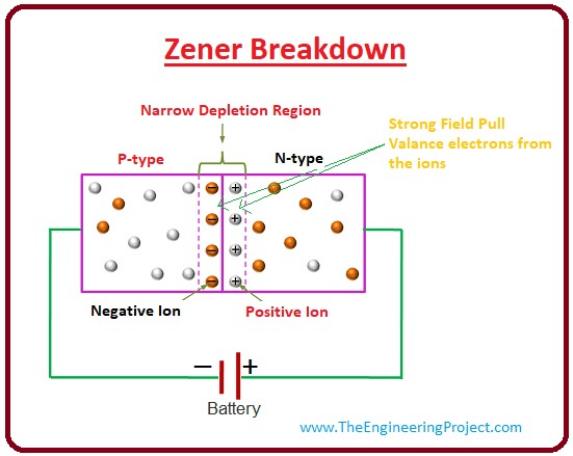
When a small reverse bias voltage is applied across a diode a very strong electric fied is produced.

Due to this electric field covalent bond breaks and produces large number of free charge carriers.



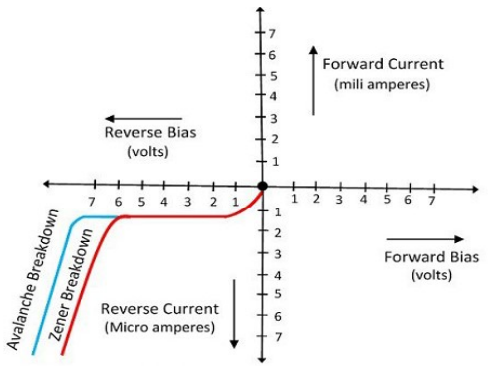
Breakdown Characteristic

Circuit Globe



Types of Diode Breakdown

	ZENER BREAKDOWN	AVALANCHE BREAKDOWN
01	The process in which the electrons move across the barrier from the valence band of p-type material to the conduction band of n-type material is known as Zener breakdown.	The process of applying high voltage and increasing the free electrons or electric current in semiconductors and insulating materials is called an avalanche breakdown.
02	This is observed in Zener diodes having a Zener breakdown voltage Vz of 5 to 8 volts.	This is observed in Zener diode having a Zener breakdown voltage Vz greater than 8 volts.
03	The valence electrons are pulled into conduction due to the high electric field in the narrow depletion region.	The valence electrons are pushed to conduction due to the energy imparted by accelerated electrons, which gain their velocity due to their collision with other atoms.
04	The increase in temperature decreases the breakdown voltage.	The increase in temperature increases the breakdown voltage.
05	The VI characteristics of a Zener breakdown has a sharp curve.	The VI characteristic curve of the avalanche breakdown is not as sharp as the Zener breakdown.
06	It occurs in diodes that are highly doped.	It occurs in diodes that are lightly doped.



Breakdown Characteristic

Circuit Globe

Temperature Effects on V-I Characteristics of a Diode

- The Effect of variation in temperature across a semiconductor diode is observed both in the forward as well as in reverse characteristics.

- Rise in temperature generates more electron-hole pair thus conductivity increases and thus increases in current.

- PN junction diode parameters like reverse saturation current, bias current, reverse breakdown voltage and barrier voltage are dependent on temperature.

- Increase in the temperature increases carrier concentration. As a result, knee voltage decreases & breakdown voltage increases while reverse saturation current increases.

Temperature Effects on V-I Characteristics of a Diode

Under Forward Bias the Change in Temperature across the diode: Barrier voltage is dependent on temperature hence it decreases by 2.5mV/ °C rise in temperature for both germanium and silicon.

Under Reverse Bias the Change in Temperature across the diode: Reverse saturation current (I_S) of diode increases with increase in the temperature. The rise is 7%/°C for both germanium & silicon and approximately doubles for every 10°C rise in temperature.

Reverse breakdown voltage (V_R) also increases as the temperature increases

Temperature Effects on V-I Characteristics of a Diode

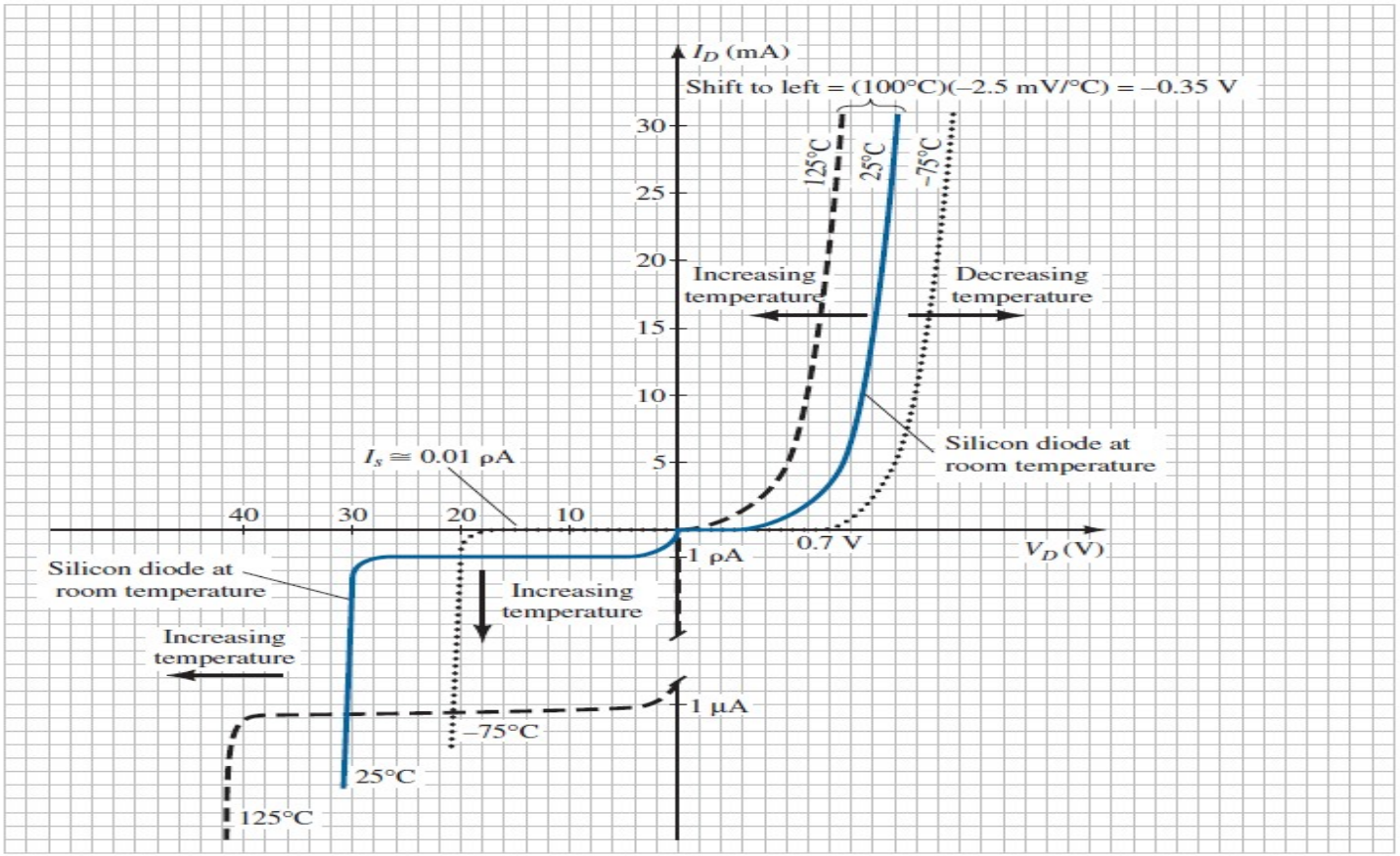


FIG. 19
Variation in Si diode characteristics with temperature change.

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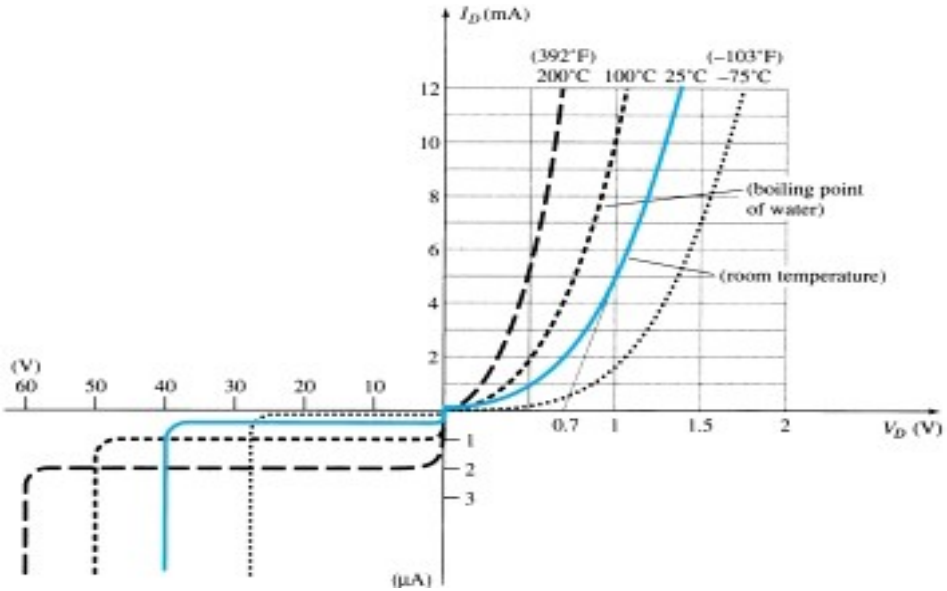
Temperature Effects: Numerical

1. The reverse saturation current Is will double in magnitude for every 10°C increase in temperature.



2. The Knee voltage shifts to the left at a rate of 2.5mV per degree centigrade increase in temperature

Reference :ELECTRONIC DEVICES AND CIRCUIT THEORY ROBERT BOYLESTAD LOUIS NASHELSKY

Temperature Effects: Numerical

1. The knee voltage of a Si diode is 0.7V and its reverse Saturation current is 20nA at 25°C. Determine these values at 40°C.

Solution:

Knee voltage shift left at a rate of 2.5mV per centigrade degree increase in temperature.

Therefore for a Change in temperature is = 40°C-25°C =15°C

Change in knee voltage will be =2.5mV X 15= 0.0375V

Hence V_K at 40°C = 0.7-0.0375= 0.6625 V,

Reverse Saturation Current doubles for every 10°C rise in Temperature
I_S at 40°C = 2^ (40-25/10) X 20nA = 2.82X20nA = 56.56nA.

Temperature Effects: Numerical

2.The reverse saturation current of a Germanium diode is 200µA at room temperature of 27°C. Calculate the current in forward biased condition, if forward biased voltage is 0.2V at room temperature. If temperature is increased by 30°C, calculate the reverse saturation current and the forward current for the same forward voltage at new temperature.

Solution:

$V_T = kT/q = 25.9mV$ k = 1.380 649 . 10^-23 Joule/Kelvin. $q = 1.602176634 \times 10^{-19}$ coulomb

$I = I_s \times (e^{(VD/\eta V_T)} - 1) = 200\mu A \times e^{0.2/.0259} = 0.451A$

If the temperature is increased by 30°C New temperature is 27+30= 57°C

Therefore Is= 200µ X2^3= 1600 µA therefore at new V_T at 57°C is 28.4mV

Hence I_D at 57°C = 1.83A.

Temperature Effects: Numerical

3. A Ge diode has a reverse saturation current of 5μA at temperature 300K find diode current at 40°C . When forward bias voltage is 0.27.

Solution:

$q = 1.602176634 \times 10^{-19}$ coulomb

k = 1.380 649 . 10^-23 Joule/Kelvin.

Given Is at 27°C is 5μA

Therefore, Is at 40°C is = $5\mu \times 2^{(40-27/10)}$

$= 5\mu \times 2.462$

$= 12.31\ \mu A$

Hence V_T at 40°C = kT/q= 26.9mV

Therefore $I = I_s \times (e^{(VD/\eta V_T)} - 1) = 12.31\mu A \times e^{(VD/\eta V_T)} = 281.49mA$

Temperature Effects: Numerical

4. The reverse saturation current of a Si diode is 2pA at 27°C. Determine the forward biased voltage across the diode at 57°C, if the forward current through the diode at 57°C is 50mA.

Solution:

Reverse saturation current doubles for every 10°C rise in temperature

Hence at if reverse saturation current at 27°C is 2pA

Then reverse saturation current at 37°C is 4pA

Then reverse saturation current at 47°C is 8pA

Then reverse saturation current at 57°C is 16pA

$q = 1.602176634 \times 10^{-19}$ coulomb

$k = 1.380\,649 \,.\, 10^{-23}$ Joule/Kelvin.

Therefore V_T 57°C is $= k \times 330/q = 28.42$mV

Hence by using $I_D = I_s \times (e^{(VD/\eta V_T)} - 1) = 50$mA

$50/16 = e^{VD/\eta V_T} \rightarrow \ln(50/16) = VD/28.42m \rightarrow V_D = 0.686$V at 57°C.

Temperature Effects: Numerical

5.The reverse saturation current of a Germanium diode is 100µA at room temperature of 28°C. Calculate the current in forward biased condition, if forward biased voltage is 0.3V at room temperature. If temperature is increased by 25°C, calculate the reverse saturation current and the forward current for the same forward voltage at new temperature.

Solution:

$V_T = kT/q = 25.9mV$ k = 1.380 649 . 10^-23 Joule/Kelvin. $q = 1.602176634 \times 10^{-19}$ coulomb

$I = I_s \times (e^{(VD/\eta V_T)} - 1)$

If the temperature is increased by 28°C New temperature is 28+25= 53°C

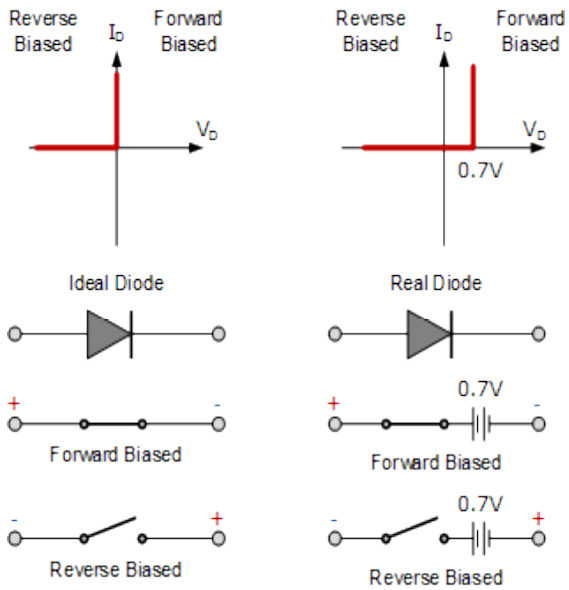
Therefore Is= 100µ X2^2.5= 565.68 µA. Therefore, new V_T at 53°C is 28.117 mV

Hence I_D at 53°C = 24.31 A.

Ideal and Practical Diode Characteristics:

Ideal Diode: When an ideal diode is forward biased, it offers no resistance & acts like a closed switch. Likewise, the ideal diode under reverse bias offers infinite resistance hence, it acts like open switch.

Practical Diode: A diode which is said to be forward biased it starts conducting at knee voltage & under reverse bias no current due to majority charges hence a practical diode is considered to be open switch (minority charges current ignored).



Resistance of a Semiconductor Diode

- An actual diode offers a very small resistance (not zero) when forward biased and is called a forward resistance
- Whereas, it offers a very high resistance (not infinite) when reverse biased and is called as a reverse resistance

- Type of applied voltage or signal will define

the following resistance levels

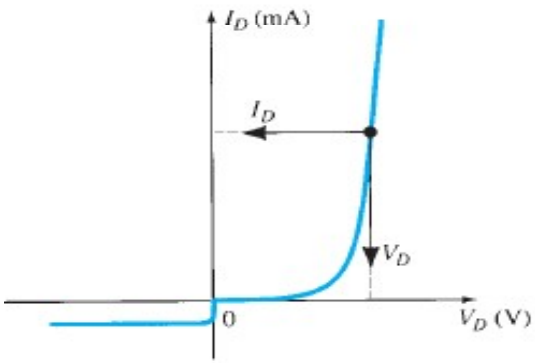
i. DC or Static Resistance

ii. AC or Dynamic Resistance

iii. Average AC Resistance

DC or Static Resistance

- The application of a dc voltage to a circuit containing a semiconductor diode will result in an operating point on the semiconductor diode characteristic curve.
- Finding the corresponding levels of V_D and I_D at particular operating point gives the DC resistance.



$$R_D = \frac{V_D}{I_D}$$

- Typically, the dc resistance of a diode in:

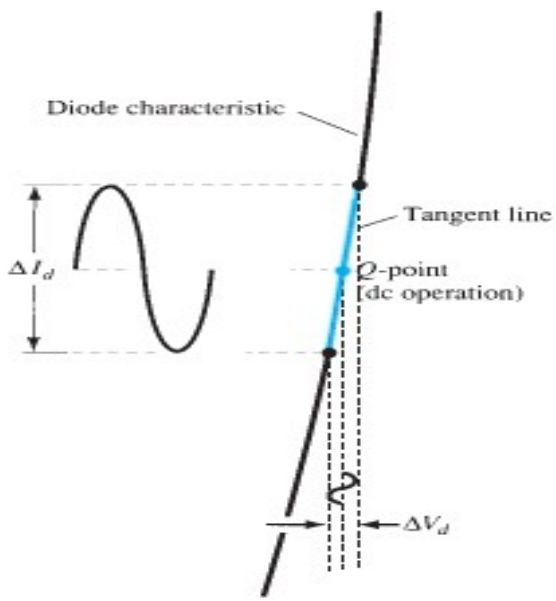
Forward bias : 10 Ω to 80 Ω

Reverse Bias: 10 MΩ

AC or Dynamic Resistance

- The application of a small AC voltage to a circuit containing a semiconductor diode offers AC resistance.
- A straight line drawn tangent to the curve through the Q –point will define a particular change in voltage and current determines the ac or dynamic resistance for this region of the diode characteristics.

$$r_d = \frac{\Delta V_d}{\Delta I_d}$$



AC or Dynamic Resistance

- Dynamic resistance can be found simply by substituting the quiescent value of the diode current into the equation also

$$r_d = \frac{26\text{ mV}}{I_D}$$

$$r'_d = \frac{26\text{ mV}}{I_D} + r_B \quad \text{ohms}$$

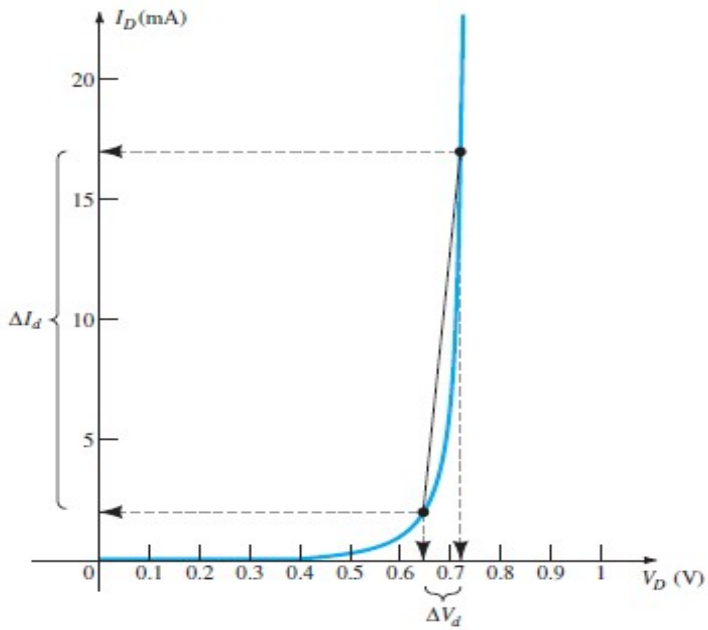
- Where r_B is bulk or body resistance

Typically, the ac resistance of a diode in the active region will range from 1 Ω to 100 Ω.

Average AC Resistance

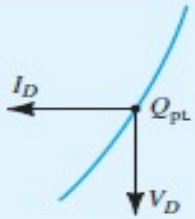
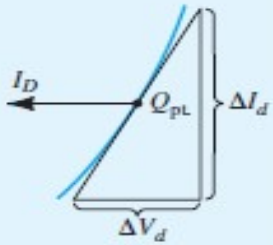
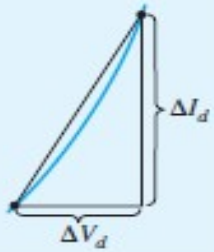
If applied input signal is sufficiently large to produce a broad swing and the resistance determined by a straight line drawn between the two intersections established by the maximum and minimum values of input voltage is called Average AC Resistance

$$r_{av} = \left.\frac{\Delta V_d}{\Delta I_d}\right|_{\text{pt. to pt.}}$$



ELECTRONIC PRINCIPLES AND DEVICES

Summary of Resistances

Type	Equation	Special Characteristics	Graphical Determination
DC or static	$R_D = \frac{V_D}{I_D}$	Defined as a point on the characteristics	
AC or dynamic	$r_d = \frac{\Delta V_d}{\Delta I_d} = \frac{26\text{ mV}}{I_D}$	Defined by a tangent line at the Q-point	
Average ac	$r_{av} = \left.\frac{\Delta V_d}{\Delta I_d}\right\|_{\text{pt. to pt.}}$	Defined by a straight line between limits of operation	

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the following resistance levels

i. DC or Static Resistance

ii. AC or Dynamic Resistance

iii. Average AC Resistance

Diode Resistance: Numerical

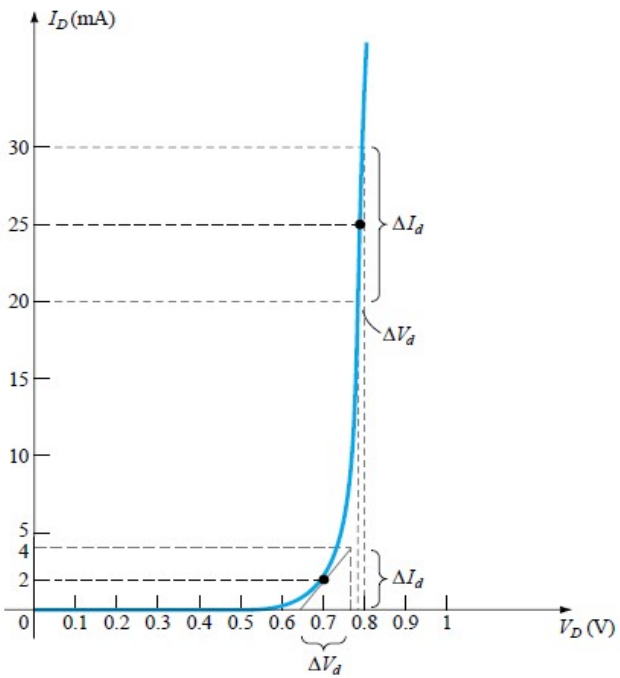
Reference :ELECTRONIC DEVICES AND CIRCUIT THEORY ROBERT BOYLESTAD LOUIS NASHELSKY

1) For the characteristics of Fig:

(a) Determine the ac resistance at I_D *2 mA.*

(b) Determine the ac resistance at I_D *25 mA.*

(c) Compare the results of parts (a) and (b) to the dc resistances at each current level.



a)

$$\Delta I_d = 4\text{ mA} - 0\text{ mA} = 4\text{ mA}$$

$$\Delta V_d = 0.76\text{ V} - 0.65\text{ V} = 0.11\text{ V}$$

$$r_d = \frac{\Delta V_d}{\Delta I_d} = \frac{0.11\text{ V}}{4\text{ mA}} = \mathbf{27.5\ \Omega}$$

b)

$$\Delta I_d = 30\text{ mA} - 20\text{ mA} = 10\text{ mA}$$

$$\Delta V_d = 0.8\text{ V} - 0.78\text{ V} = 0.02\text{ V}$$

$$r_d = \frac{\Delta V_d}{\Delta I_d} = \frac{0.02\text{ V}}{10\text{ mA}} = \mathbf{2\ \Omega}$$

c)

$$R_D = \frac{V_D}{I_D} = \frac{0.7\text{ V}}{2\text{ mA}} = \mathbf{350\ \Omega}$$

$$R_D = \frac{V_D}{I_D} = \frac{0.79\text{ V}}{25\text{ mA}} = \mathbf{31.62\ \Omega}$$

Diode Resistance: Numerical

2. AC or Dynamic Resistance: *The derivative of a function at a point is equal to the slope of the tangent line drawn at that point.*

$$k = \frac{11{,}600}{\eta} = \frac{11{,}600}{1} = 11{,}600$$

$$\frac{d}{dV_D}(I_D) = \frac{d}{dV}[I_s(e^{kV_D/T_K} - 1)]$$

$$\frac{dI_D}{dV_D} = \frac{k}{T_K}(I_D + I_s)$$

$$T_K = T_C + 273° = 25° + 273° = 298°$$

$$\frac{k}{T_K} = \frac{11{,}600}{298} \cong 38.93$$

$$\frac{dI_D}{dV_D} = 38.93 I_D$$

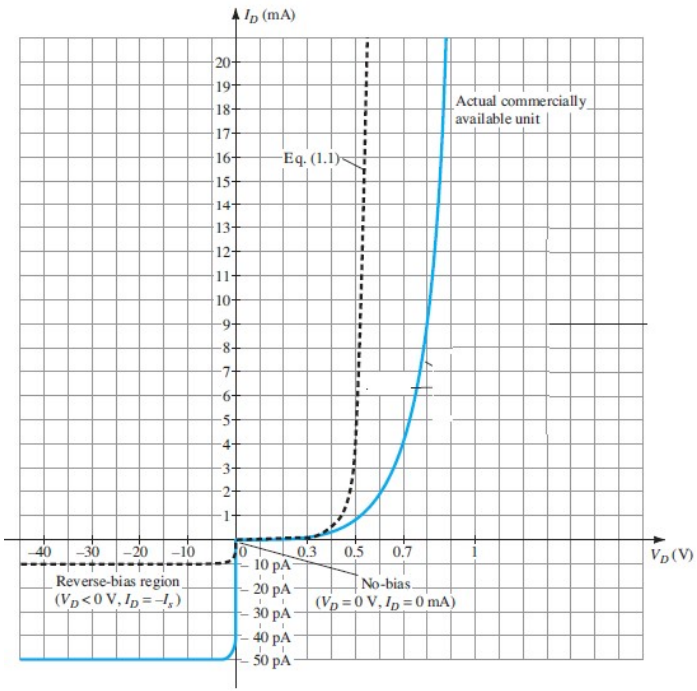
$$\frac{dI_D}{dV_D} \cong \frac{k}{T_K} I_D$$

$$\frac{dV_D}{dI_D} \cong \frac{0.026}{I_D}$$

$$\boxed{r_d = \frac{26\ \text{mV}}{I_D}}$$ Ge,Si

Diode Resistance: Numerical

3. Calculate the dc and ac resistance for the diode of Fig shown at a forward current of 10 mA and compare their magnitudes.



$$I_D = 10 \text{ mA}, V_D = 0.76 \text{ V}$$

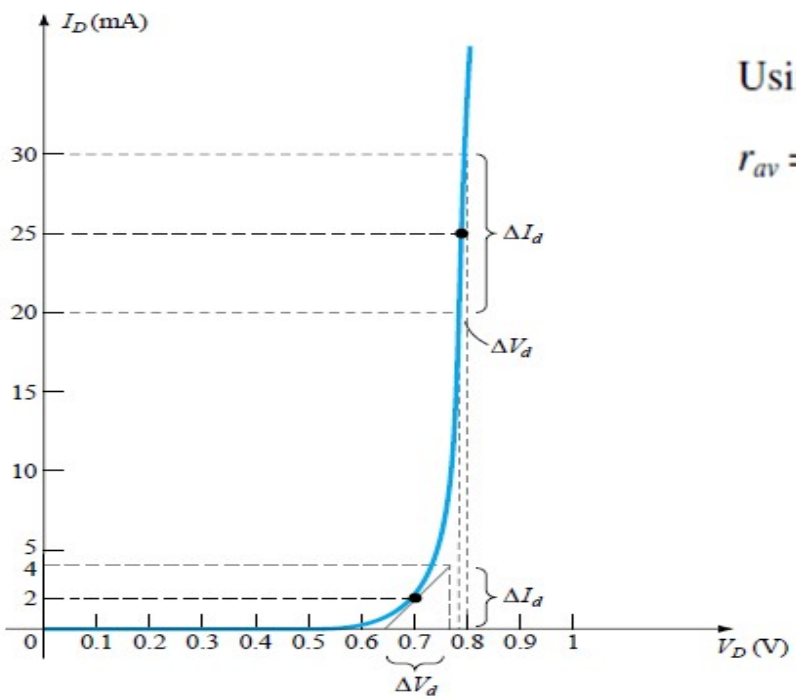
$$R_{DC} = \frac{V_D}{I_D} = \frac{0.76 \text{ V}}{10 \text{ mA}} = \mathbf{76\ \Omega}$$

$$r_d = \frac{\Delta V_d}{\Delta I_d} \cong \frac{0.85\text{V} - 0.72 \text{ V}}{15 \text{ mA} - 5 \text{ mA}} = \frac{\mathbf{0.13}\text{V}}{10 \text{ mA}} = \mathbf{13\ \Omega}$$

$$R_{DC} >> r_d$$

Diode Resistance: Numerical

4. Find the piecewise-linear equivalent circuit for the diode of Fig. Use a straight line segment that intersects the horizontal axis at 0.7 V and Best approximates the curve for the region greater than 0.7 V.

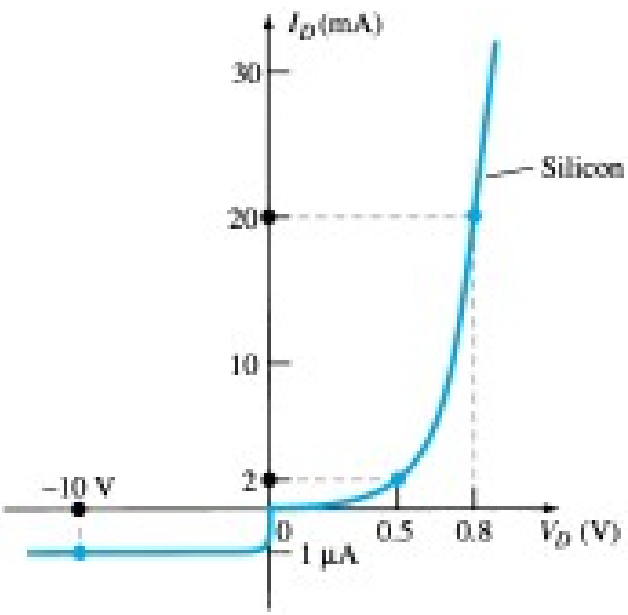


Using the best approximation to the curve beyond $V_D = 0.7$ V:

$$r_{av} = \frac{\Delta V_d}{\Delta I_d} \cong \frac{0.8\text{ V} - 0.7\text{ V}}{25\text{ mA} - 0\text{ mA}} = \frac{0.1\text{ V}}{25\text{ mA}} = 4\ \Omega$$

Diode Resistance: Numerical

5. Determine the dc resistance levels for the diode of Fig.at
(a) I_D =2 mA (b) I_D =20 mA (c) V_D = -10 V



(a) At $I_D = 2$ mA, $V_D = 0.5$ V (from the curve) and

$$R_D = \frac{V_D}{I_D} = \frac{0.5\text{ V}}{2\text{ mA}} = \mathbf{250\ \Omega}$$

(b) At $I_D = 20$ mA, $V_D = 0.8$ V (from the curve) and

$$R_D = \frac{V_D}{I_D} = \frac{0.8\text{ V}}{20\text{ mA}} = \mathbf{40\ \Omega}$$

(c) At $V_D = -10$ V, $I_D = -I_s = -1\ \mu$A (from the curve) and

$$R_D = \frac{V_D}{I_D} = \frac{10\text{ V}}{1\ \mu\text{A}} = \mathbf{10\ M\Omega}$$

Diode Equivalent Diagrams/Diode Approximations

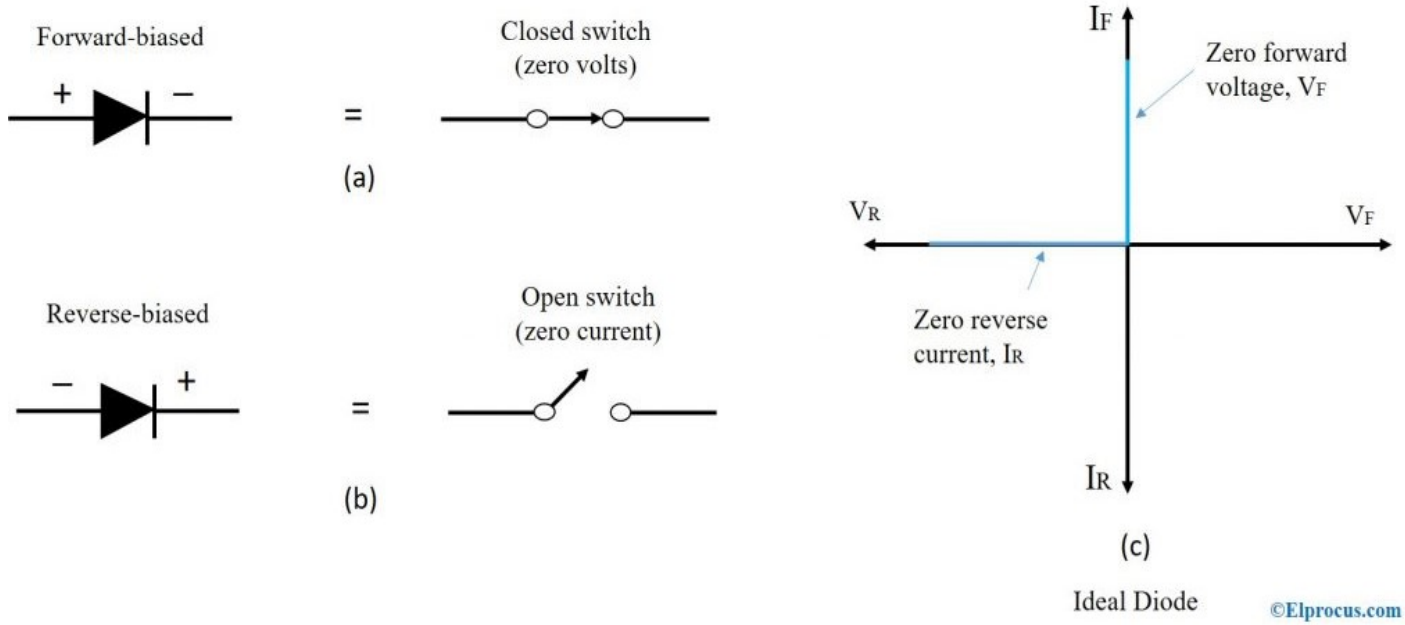
Diode approximation is a mathematical method used to approximate the nonlinear behavior of real diodes to enable calculations and circuit analysis.

There are three different approximations used to analyze the diode circuits, namely

I. First Approximation (Ideal Diode Characteristics)
II. Second Approximation (Simplified Diode Characteristics)
III. Third approximation (Piecewise-linear equivalent Circuit)

First Approximation: Ideal diode Characteristics

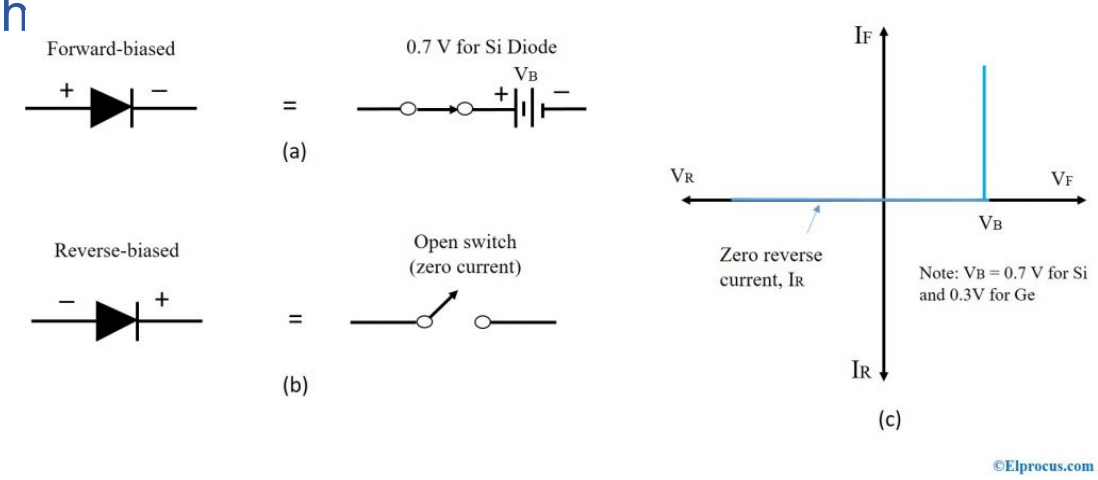
First approximation: The diode is considered as a closed switch with zero voltage drop when forward-biased and as an open switch when reverse biased



Second Approximation: Simplified Diode Characteristics

Second approximation: Under forward-bias, the diode turns ON when a voltage of V_K or V_B is applied across it. It turns off if the voltage is less than V_K. Thus, the diode is represented by a voltage of V_K in series with a closed switch.

Under reverse bias, it is an open switch



Third Approximation: Piecewise-linear equivalent

Third approximation: Considers the increase in the voltage across the diode when the current through it increases. Here the diode is represented as a closed switch in series with V_K and resistance R_B when forward biased.

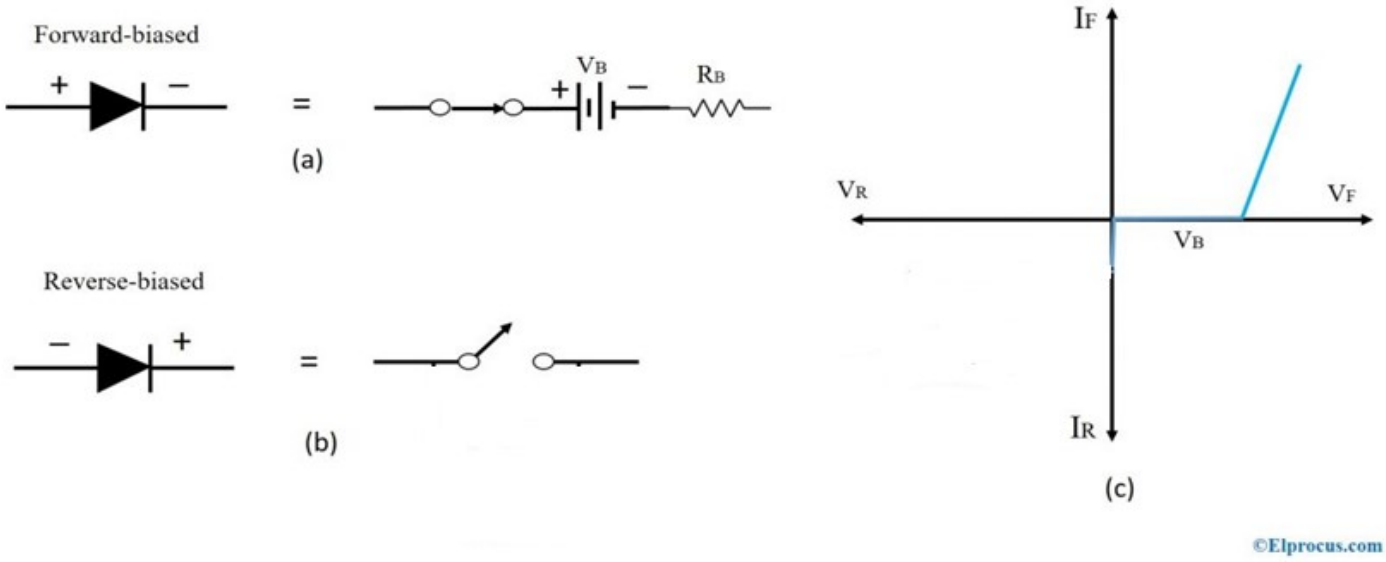
Characteristics resemble closely to that of practical diode.

The voltage drop across the diode is calculated using the formula

$V_d = V_K + I_d * R_B$

Third Approximation: Linear Piece-Wise Diode Characteristics

Under reverse – bias, the diode is an open switch and no current flows through it



Series Diode Configuration with a resistor

- It's assumed that the forward resistance of the diode is usually so small compared to the other series elements of the network that it can be ignored.
- In general, a diode is in the "on" state if the current established by the applied sources is such that its direction matches that of the arrow in the diode symbol.

Forward Bias

Constants

- **Silicon Diode: $V_D = 0.7$ V**
- **Germanium Diode: $V_D = 0.3$ V**

ELECTRONIC PRINCIPLES AND DEVICES

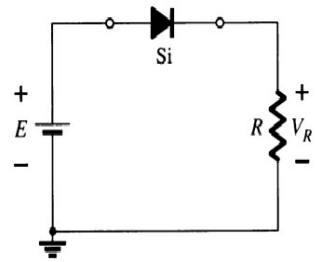
Series Diode Configuration with a resistor

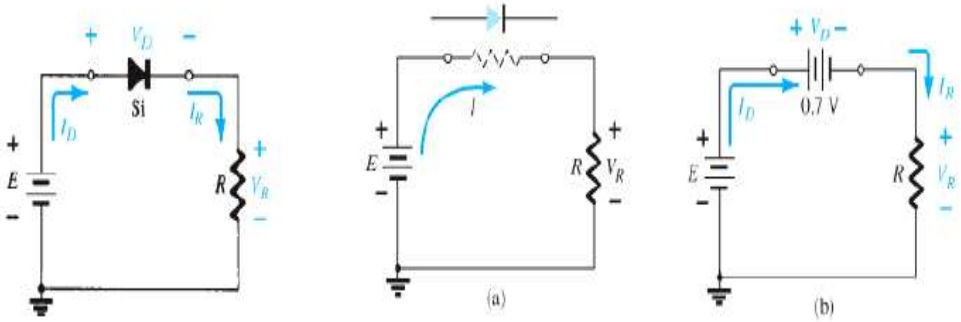
Reverse Bias

Diodes ideally behave as open circuits

Analysis

$V_D = E$; $V_R = 0$ V & $I_D = 0$ A

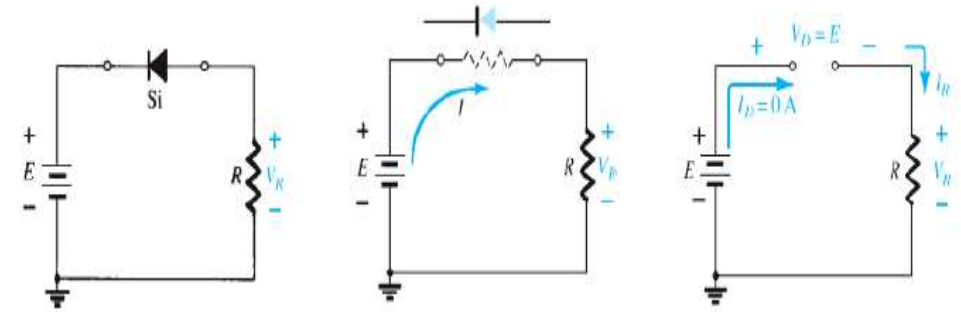




$V_D = V_K$

$V_R = E - V_K$

$I_D = I_R = \frac{V_R}{R}$



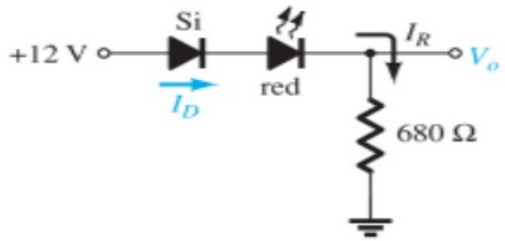
$V_R = I_R R = I_D R = (0\text{ A})R = \mathbf{0\ V}$

Analysis (for silicon)

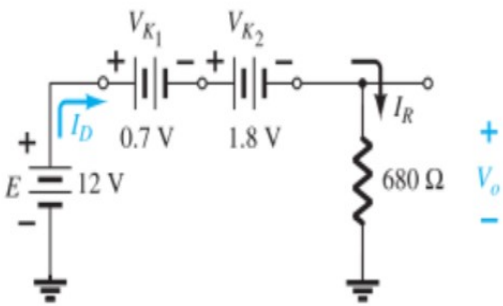
- $V_D = 0.7$ V (or $V_D = E$ if $E < 0.7$ V)
- $V_R = E - V_D$
- $I_D = I_R = I_T = V_R / R$

Series Diode Configuration – A Solved Problem

1. Determine Vout and Id for the given series diode Circuit. Assume the LED Voltage as 1.8 V.



Solution: Re-draw the given circuit based on simplified diode's configuration, we get

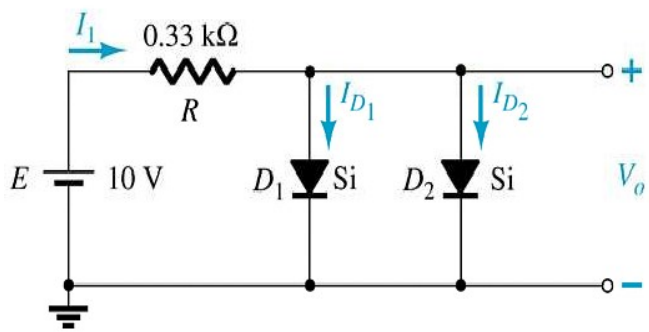


$$V_o = E - V_{K_1} - V_{K_2} = 12\text{ V} - 2.5\text{ V} = \mathbf{9.5\text{ V}}$$

$$I_D = I_R = \frac{V_R}{R} = \frac{V_o}{R} = \frac{9.5\text{ V}}{680\ \Omega} = \mathbf{13.97\text{ mA}}$$

Parallel Diode Configuration - A Solved Problem

2. Determine Vo , I_1 , I_{D1}, and I_{D2} for the parallel diode configuration of Figure below

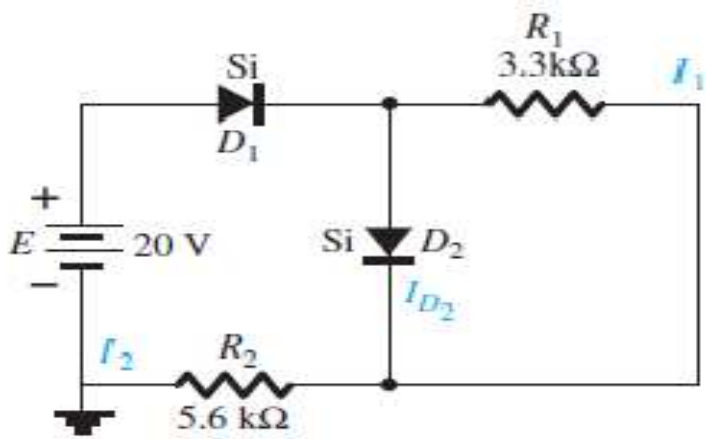


Solution: $V_o = 0.7\text{ V}$

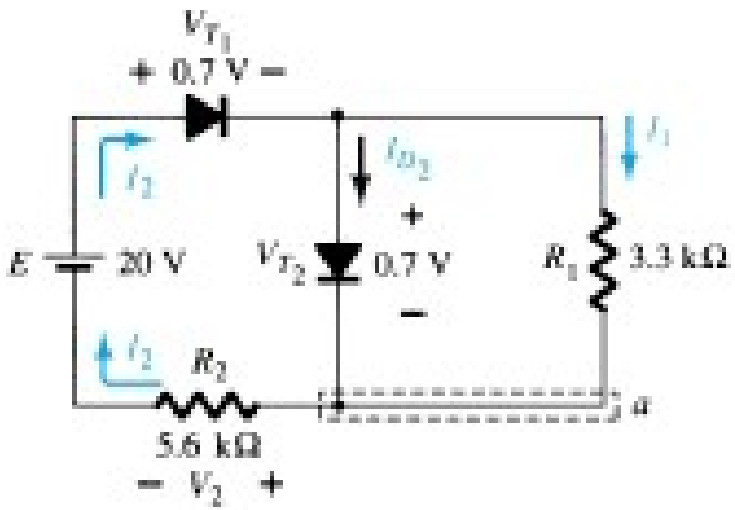
$$I_1 = \frac{V_R}{R} = \frac{E - V_D}{R} = \frac{10\text{ V} - 0.7\text{ V}}{0.33\text{ k}\Omega} = 28.18\text{ mA}$$

$$I_{D_1} = I_{D_2} = \frac{I_1}{2} = \frac{28.18\text{ mA}}{2} = 14.09\text{ mA}$$

3. Determine I_1, I_2, and I_{D2} for the series- parallel diode configuration of Figure below



Series-Parallel Diode Configuration – An Excise Problem



$$-V_2 + E - V_{T_1} - V_{T_2} = 0$$

$$V_2 = E - V_{T_1} - V_{T_2} = 20\text{ V} - 0.7\text{ V} - 0.7\text{ V} = 18.6\text{ V}$$

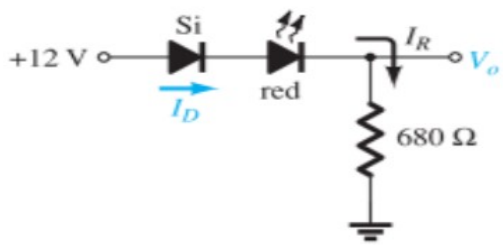
$$I_2 = \frac{V_2}{R_2} = \frac{18.6\text{ V}}{5.6\text{ k}\Omega} = \mathbf{3.32\text{ mA}}$$

$$I_{D_2} + I_1 = I_2$$

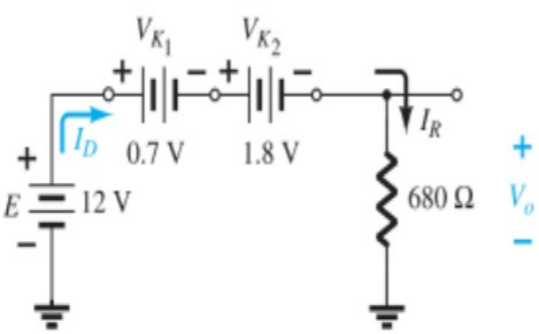
$$I_1 = \frac{V_{T_2}}{R_1} = \frac{0.7\text{ V}}{3.3\text{ k}\Omega} = \mathbf{0.212\text{ mA}}$$

$$I_{D_2} = I_2 - I_1 = 3.32\text{ mA} - 0.212\text{ mA} = \mathbf{3.108\text{ mA}}$$

4. Determine V_{out} and I_d for the given series diode Circuit. Assume the LED Voltage as 1.8 V.



Solution: Re-draw the given circuit based on simplified diode's configuration, we get



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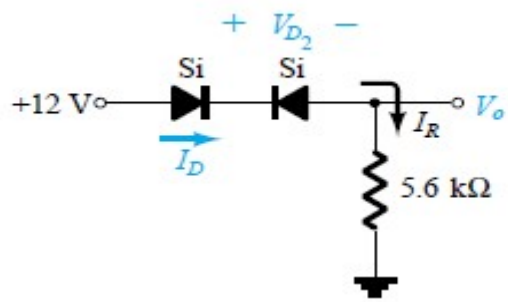
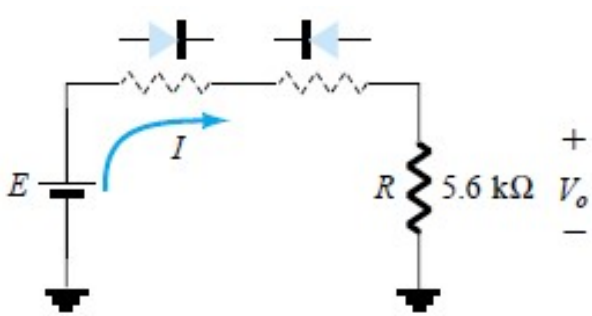
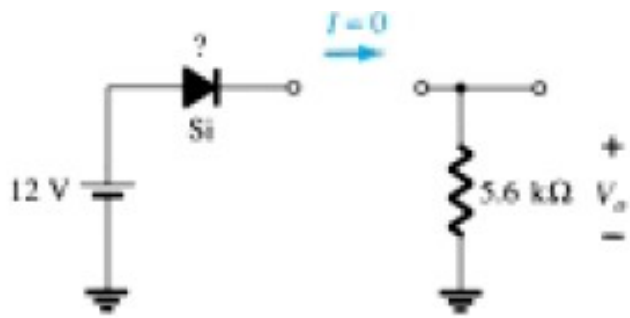
$$I_D = I_R = \frac{V_R}{R} = \frac{V_o}{R} = \frac{9.5\text{ V}}{680\ \Omega} = \mathbf{13.97\text{ mA}}$$

5. Determine I_D, V_{D2} and V_o



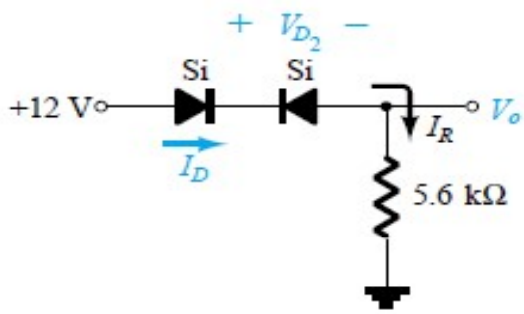
Solution: Re-draw the given circuit based on simplified diode's configuration, we get





Series Diode Configuration

$$V_o = I_R R = I_D R = (0\text{ A})R = 0\text{ V}$$



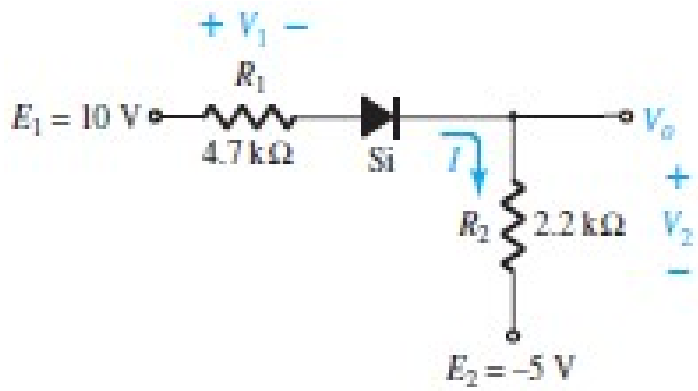
$$E - V_{D_1} - V_{D_2} - V_o = 0$$

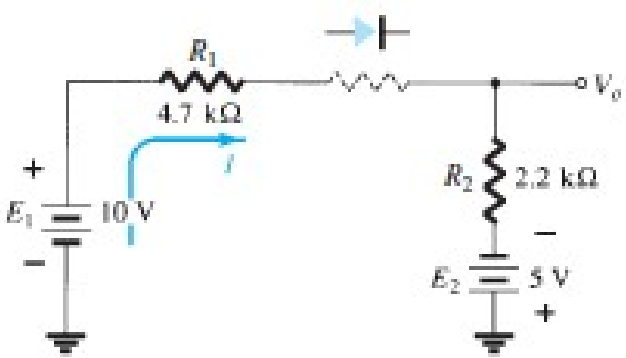
$$V_{D_2} = E - V_{D_1} - V_o = 12\text{ V} - 0 - 0$$

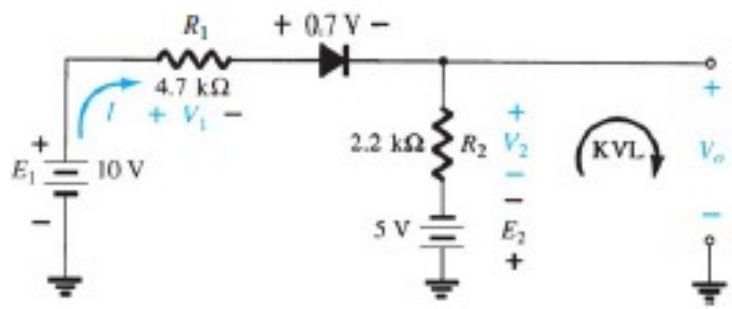
$$= \mathbf{12\ V}$$

$$V_o = \mathbf{0\ V}$$

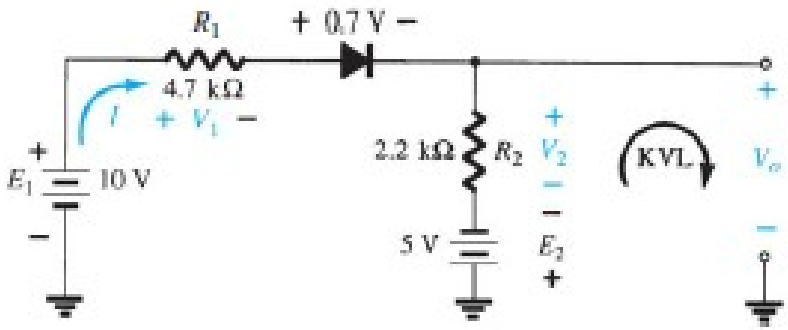
6. Determine I, V_1, V_2 and V_0







Series Diode Configuration

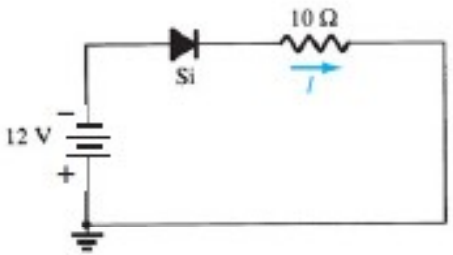


$$I = \frac{E_1 + E_2 - V_D}{R_1 + R_2} = \frac{10\text{ V} + 5\text{ V} - 0.7\text{ V}}{4.7\text{ k}\Omega + 2.2\text{ k}\Omega} = \frac{14.3\text{ V}}{6.9\text{ k}\Omega}$$
$$\cong \mathbf{2.07\text{ mA}}$$

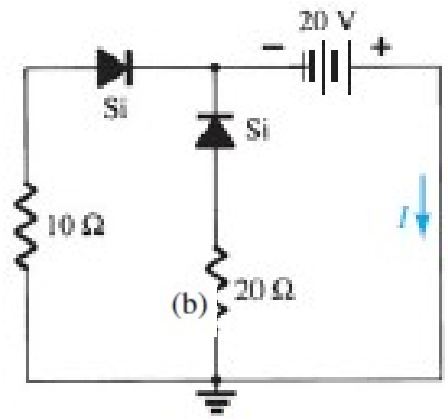
$$V_1 = IR_1 = (2.07\text{ mA})(4.7\text{ k}\Omega) = \mathbf{9.73\text{ V}}$$
$$V_2 = IR_2 = (2.07\text{ mA})(2.2\text{ k}\Omega) = \mathbf{4.55\text{ V}}$$

$$-E_2 + V_2 - V_o = 0$$
$$V_o = V_2 - E_2 = 4.55\text{ V} - 5\text{ V} = \mathbf{-0.45\text{ V}}$$

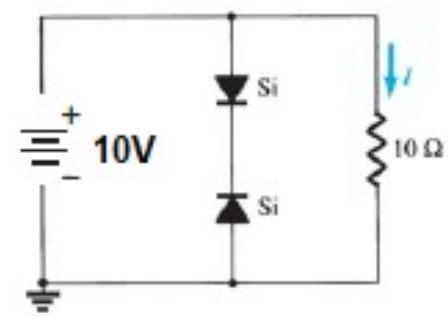
7. Determine the current I for each of the configurations



(a)



(b)



(c)

(a) $I = \mathbf{0\ mA}$; diode reverse-biased.

(b) $V_{20\Omega} = 20\ \text{V} - 0.7\ \text{V} = 19.3\ \text{V}$ (Kirchhoff's voltage law)

$$I(20\ \Omega) = \frac{19.3\ \text{V}}{20\ \Omega} = 0.965\ \text{A}$$

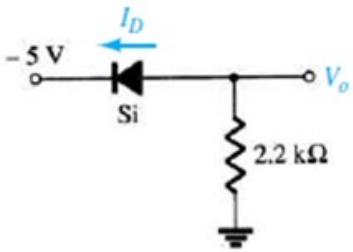
$$V(10\ \Omega) = 20\ \text{V} - 0.7\ \text{V} = 19.3\ \text{V}$$

$$I(10\ \Omega) = \frac{19.3\ \text{V}}{10\ \Omega} = 1.93\ \text{A}$$

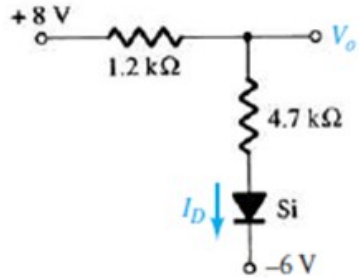
$$I = I(10\ \Omega) + I(20\ \Omega)$$
$$= \mathbf{2.895\ A}$$

(c) $I = \dfrac{10\ \text{V}}{10\ \Omega} = \mathbf{1\ A}$; center branch open

8. Determine V_0 and I_D for the networks



(a)



(b)

(a) Diode forward-biased,

Kirchhoff's voltage law (CW): $-5\text{ V} + 0.7\text{ V} - V_o = 0$

$$V_o = \mathbf{-4.3\ V}$$

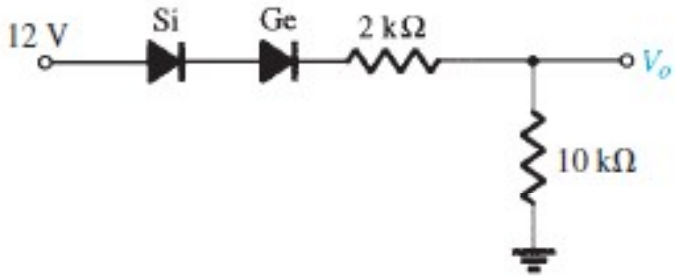
$$I_R = I_D = \frac{|V_o|}{R} = \frac{4.3\text{ V}}{2.2\text{ k}\Omega} = \mathbf{1.955\ mA}$$

(b) Diode forward-biased,

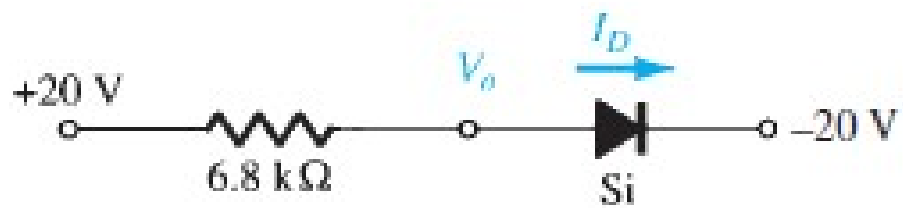
$$I_D = \frac{8\text{ V} + 6\text{ V} - 0.7\text{ V}}{1.2\text{ k}\Omega + 4.7\text{ k}\Omega} = \mathbf{2.25\ mA}$$

$$V_o = 8\text{ V} - (2.25\text{ mA})(1.2\text{ k}\Omega) = \mathbf{5.3\ V}$$

9. Determine the level of V_0 for each network



(a) $V_o = \dfrac{10\ \text{k}\Omega(12\ \text{V} - 0.7\ \text{V} - 0.3\ \text{V})}{2\ \text{k}\Omega + 10\ \text{k}\Omega} = \mathbf{9.17\ V}$



(b) Diode forward-biased

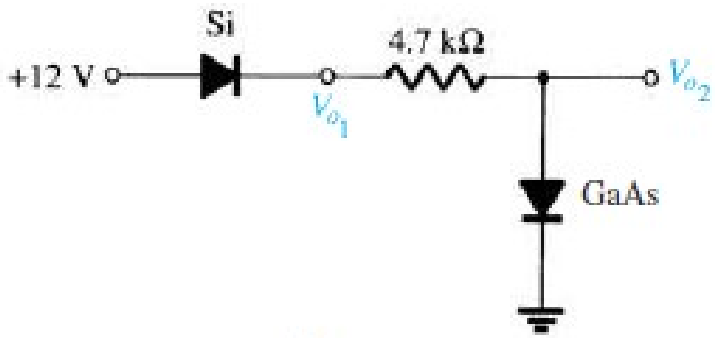
$$I_D = \frac{20\ \text{V} + 20\ \text{V} - 0.7\ \text{V}}{6.8\ \text{k}\Omega} = \mathbf{5.78\ mA}$$

Kirchhoff's voltage law (CW):

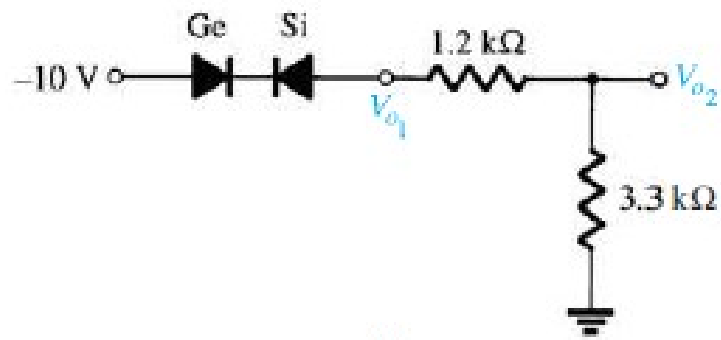
$+V_o - 0.7\ \text{V} + 20\ \text{V} = 0$

$V_o = \mathbf{-19.3\ V}$

10. Determine V_{01} and V_{02} for the circuits



(a)



(b)

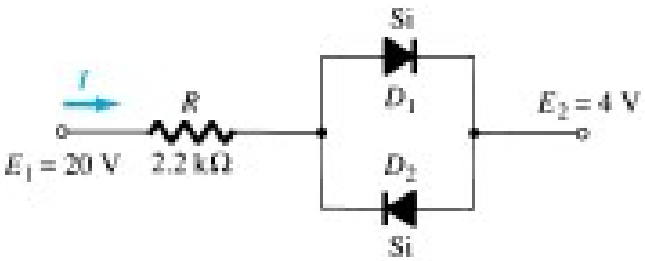
(a) $V_{o_1} = 12\text{ V} - 0.7\text{ V} = \mathbf{11.3\text{ V}}$

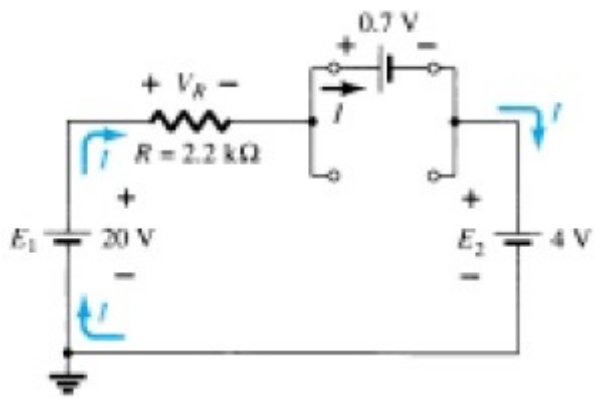
$V_{o_2} = \mathbf{1.2\text{ V}}$

(b) $V_{o_1} = \mathbf{0\text{ V}}$

$V_{o_2} = \mathbf{0\text{ V}}$

11. Determine I for the parallel diode configuration of Figure below

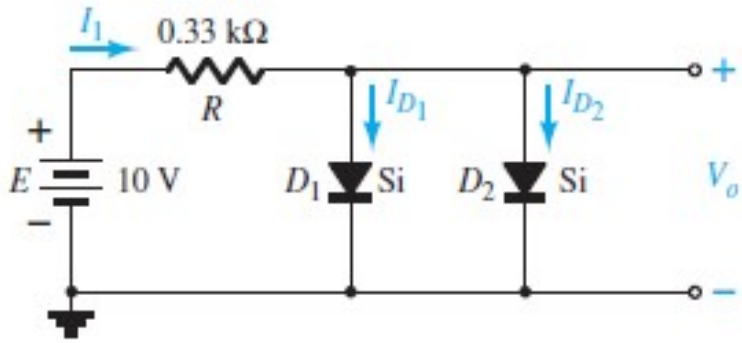


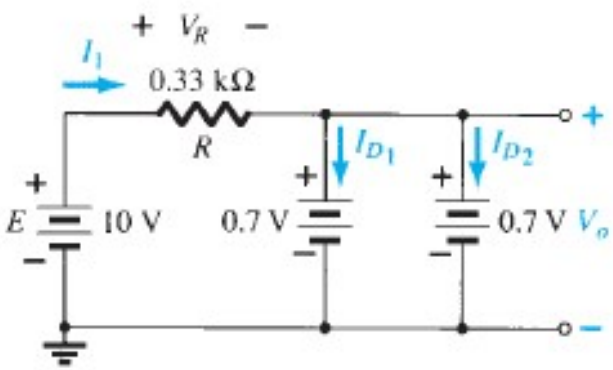


Solution:

$$I = \frac{E_1 - E_2 - V_D}{R} = \frac{20\text{ V} - 4\text{ V} - 0.7\text{ V}}{2.2\text{ k}\Omega} \cong \mathbf{6.95\ mA}$$

12. Determine V_0, I_1, I_2 in the diode circuit





$$V_o = 0.7\text{ V}$$

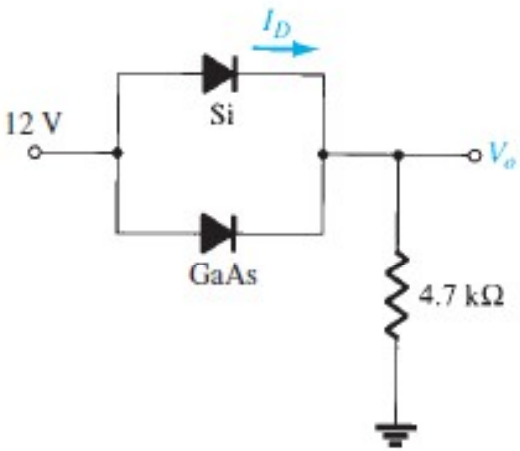
The current is

$$I_1 = \frac{V_R}{R} = \frac{E - V_D}{R} = \frac{10\text{ V} - 0.7\text{ V}}{0.33\text{ k}\Omega} = \mathbf{28.18\text{ mA}}$$

Assuming diodes of similar characteristics, we have

$$I_{D_1} = I_{D_2} = \frac{I_1}{2} = \frac{28.18\text{ mA}}{2} = \mathbf{14.09\text{ mA}}$$

13. Determine I_D and V_0 for the circuits shown

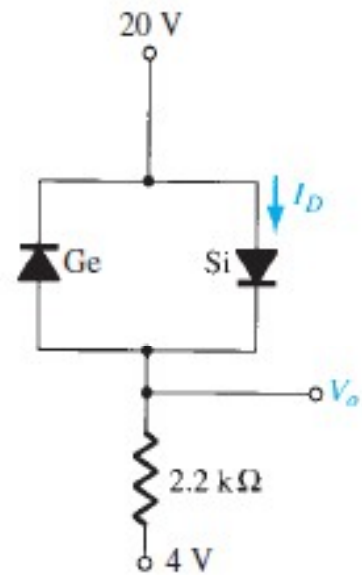


(a) Both diodes forward-biased
Si diode turns on first and locks in 0.7 V drop.

$$I_R = \frac{12\text{ V} - 0.7\text{ V}}{4.7\text{ k}\Omega} = 2.4\text{ mA}$$

$$I_D = I_R = \mathbf{2.4\text{ mA}}$$

$$V_o = 12\text{ V} - 0.7\text{ V} = \mathbf{11.3\text{ V}}$$

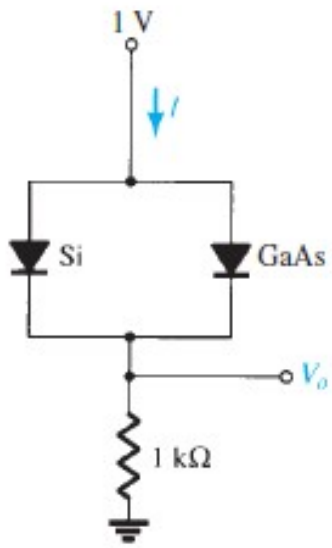


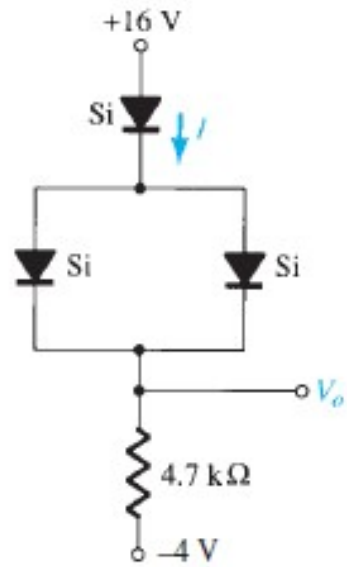
(b) Right diode forward-biased:

$$I_D = \frac{20\text{ V} + 4\text{ V} - 0.7\text{ V}}{2.2\text{ k}\Omega} = \mathbf{10.59\text{ mA}}$$

$$V_o = 20\text{ V} - 0.7\text{ V} = \mathbf{19.3\text{ V}}$$

14. Determine I and V_0 for the circuits shown





Si diode "on" preventing GaAs diode from turning "on":

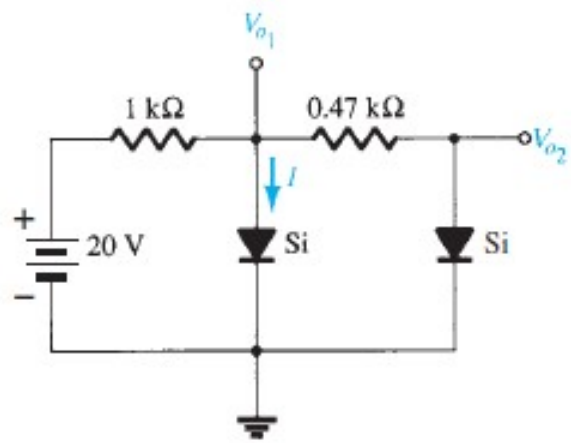
$$I = \frac{1\text{ V} - 0.7\text{ V}}{1\text{ k}\Omega} = \frac{0.3\text{ V}}{1\text{ k}\Omega} = \mathbf{0.3\text{ mA}}$$

$$V_o = 1\text{ V} - 0.7\text{ V} = \mathbf{0.3\text{ V}}$$

$$I = \frac{16\text{ V} - 0.7\text{ V} - 0.7\text{ V} + 4\text{ V}}{4.7\text{ k}\Omega} = \frac{18.6\text{ V}}{4.7\text{ k}\Omega} = \mathbf{3.96\text{ mA}}$$

$$V_o = 16\text{ V} - 0.7\text{ V} - 0.7\text{ V} = \mathbf{14.6\text{ V}}$$

15. Determine I, V_{01} and V_{02}



Both diodes forward-biased:

$V_{o_1} = \mathbf{0.7\ V}$, $V_{o_2} = \mathbf{0.7\ V}$

$$I_{1\ k\Omega} = \frac{20\ V - 0.7\ V}{1\ k\Omega} = \frac{19.3\ V}{1\ k\Omega} = 19.3\ mA$$

$I_{0.47\ k\Omega} = 0\ mA$

$I = I_{1\ k\Omega} - I_{0.47\ k\Omega} = 19.3\ mA - 0\ mA$

$= \mathbf{19.3\ mA}$

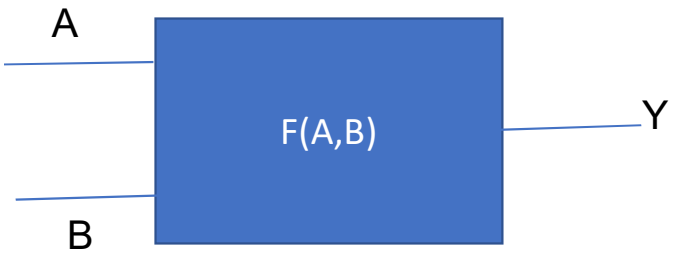
Logical operation:

It is an Operation that acts on binary numbers to produce a result according to the Laws of Boolean Logic.

A Logic Gate is a basic building block of Digital circuits.

Logic gate is considered as a device that has the ability to produce one output level with the combinations of input levels.

Example : AND,OR and NOT functions



Logical operations:

Logic gates are implemented by using diodes, transistors, and by other several devices.

Hence logic gates can also be considered as electronic circuits.

The logic gates obtained by Diode is called Diode Resistor Logic.

Inputs and outputs of logic gates are in two levels which are termed as HIGH and LOW, or TRUE and FALSE, or ON and OFF, or simply 1 and 0.

Logical Operations

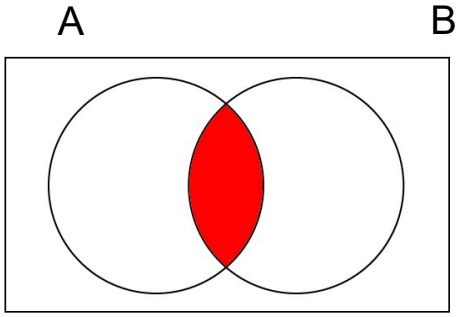
For all logic gates a Table with all combinations is listed out.

The combination of the input variables and the corresponding output is termed as “TRUTH TABLE”.

It explains how the logic circuit output responds to various combinations of logic levels at the inputs.

AND Operation is explained by the following Truth Table

A	B	Y=A.B
0	0	0
0	1	0
1	0	0
1	1	1



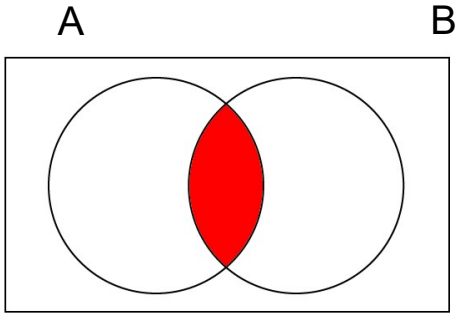
Logical Operations

An AND / OR gate may also have two or more inputs but produces only one output.

AND gate produces an output of logic 1 state when all of its inputs is in logic 1 state and produces an output of logic 0 state if any of its inputs are in logic 0 state.

AND Operation is explained by the following Truth Table

A	B	Y=A.B
0	0	0
0	1	0
1	0	0
1	1	1



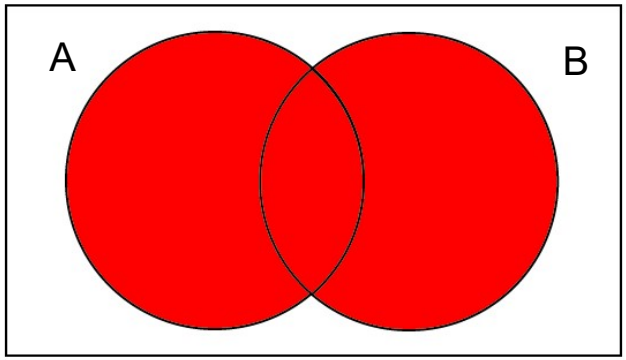
Logical Operations

An AND / OR gate may also have two or more inputs but produces only one output.

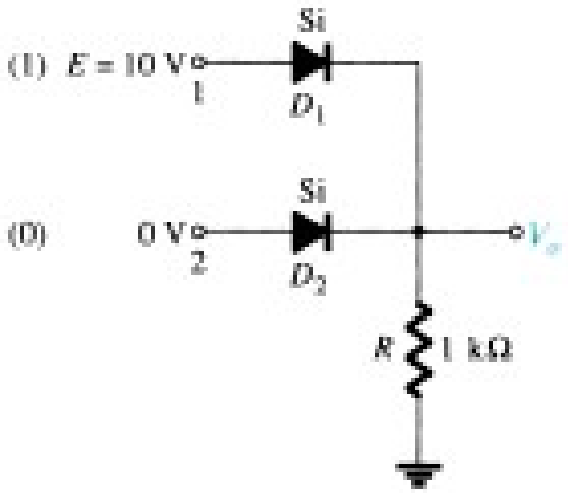
OR gate produces an output of logic 1 state even if any of its inputs is in logic 1 state and produces an output of logic 0 state if all of its inputs are in logic 0 state.

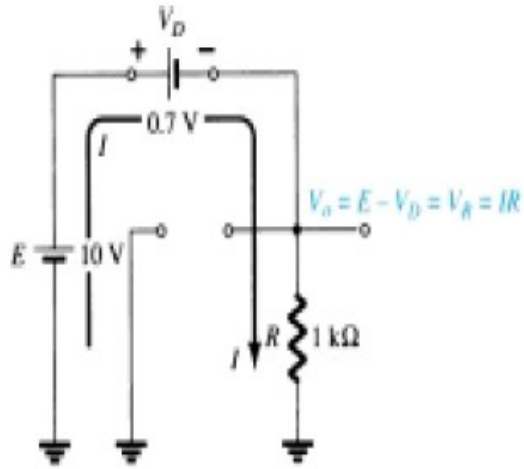
OR Operation is explained by the following Truth Table

A	B	Y=A+B
0	0	0
0	1	1
1	0	1
1	1	1



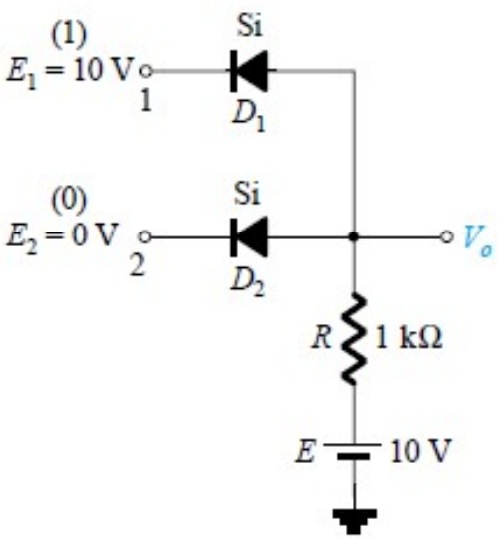
OR Operation Illustrated using Diode

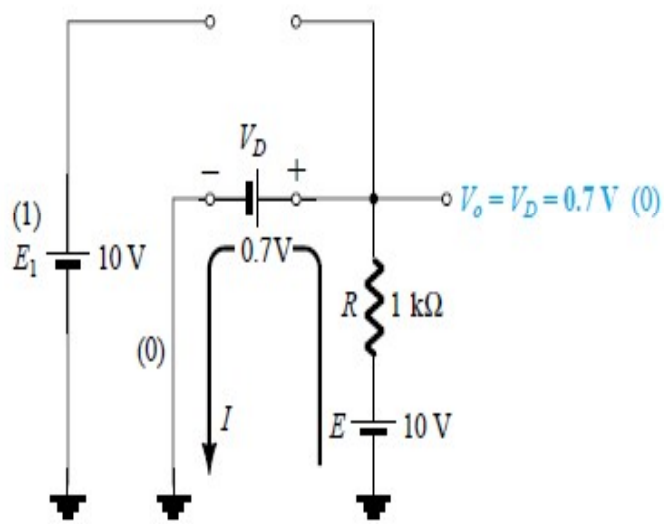




A (V1)	B(V2)	Y (Vo)
0	0	0
0	10 V	9.3 V
10 V	0	9.3 V
10 V	10 V	9.3V

AND Operation Illustrated using Diode





A (V1)	B(V2)	Y(Vo)
0	0	0.7 V
0	10 V	0.7V
10 V	0	0.7V
10 V	10 V	10V

THANK YOU

Department of Electronics and Communication

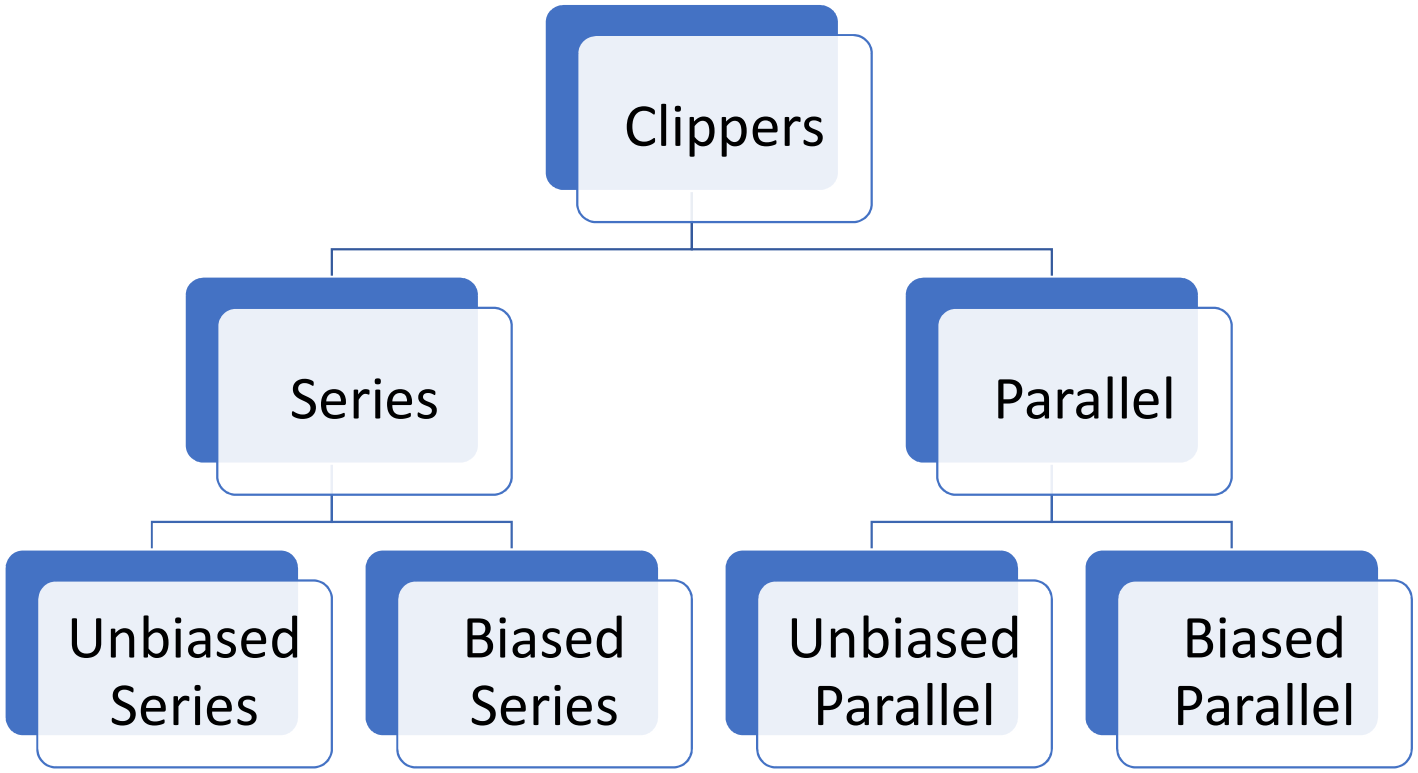
ELECTRONIC PRINCIPLES AND DEVICES

Department of Electronics and Communication Engineering

Clippers

- **Clippers** are networks that employ diodes to “clip” away a portion of an input signal without distorting the remaining part of the applied waveform.
- The half-wave rectifier is an example of the simplest form of diode clipper having one resistor and a diode.
- Depending on the orientation of the diode, the positive or negative region of the applied signal is “clipped” off.
- Two general categories:
  - **Series Clipper** (Diode is in series with the load)
  - **Parallel Clipper** (Diode in a branch parallel to the load)

Clippers - Classification



Series Clippers

- The **series configuration** is defined as one where the **diode is in series with the load.**
- Fig.1(a) shows the circuit of a series clipper.
- The response of the series configuration of Fig. 1(a) to a variety of alternating waveforms is shown in Fig. 1(b).
- There are **no boundaries on the type of signals** that can be applied to a clipper.

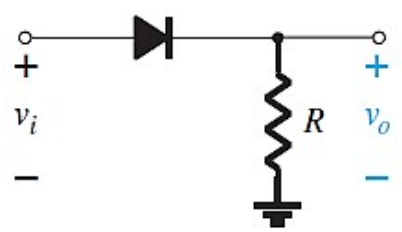


Fig. 1(a): Series Unbiased Clipper

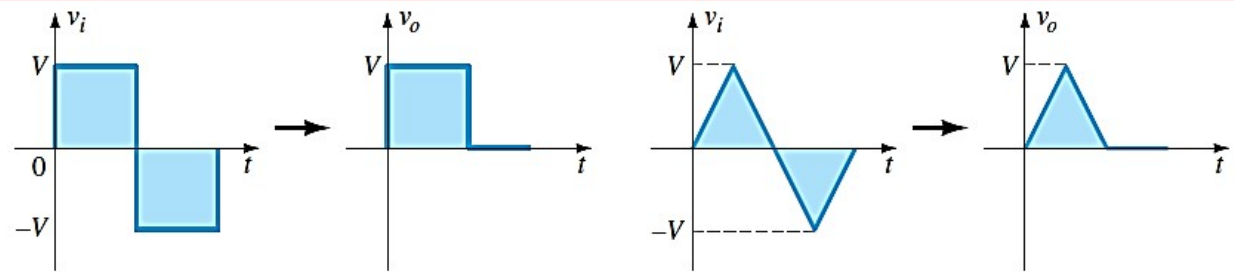


Fig. 1(b): Input-output Waveforms

Series Clippers

- Fig.2 shows the **series clipper with DC supply**. This configuration is called as **biased series clipper**.
- The **addition of a dc supply** to the network as shown in Fig. 2 can have a pronounced effect on the analysis of the series clipper configuration.
- The dc supply can be in the **leg between the supply and output** or in the **branch parallel to the output**.
- The output response is not as obvious because the **dc supply can aid or work against the source voltage.**

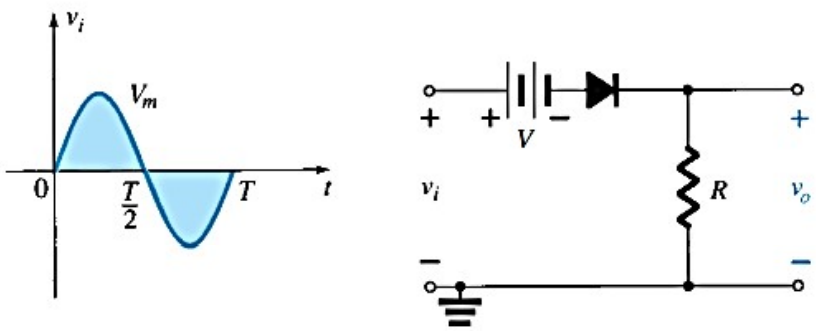


Fig. 2: Series clipper with DC supply

General instructions for analysis:

1. **Take careful note of where the output voltage is defined**.

In Fig. 2 it is directly across the resistor R . In some cases it may be across a combination of series elements.

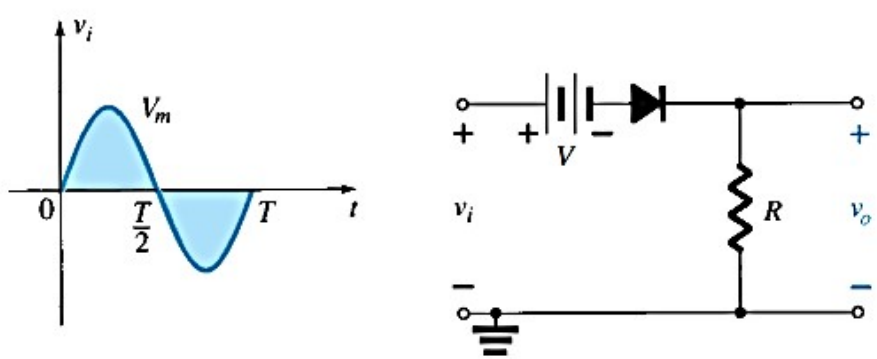


Fig. 2: Series clipper with DC supply

General instructions for analysis: (cont….)

2. **Try to develop an overall sense of the response by simply noting the that how the input supply affects the conventional current direction through the diode.**

- In Fig. 2 , for instance, any positive voltage of the supply will try to turn the diode "ON" by establishing a forward bias current through the diode.
- However, the added dc supply V will oppose that applied voltage and try to keep the diode in the "OFF" state.
- The result is that any supply voltage greater than V volts will turn the diode "ON" and conduction can be established through the load resistor. (Note here that we are dealing with an ideal diode, so the turn-on diode voltage is simply 0 V)
- Therefore, the diode will be "ON" for any voltage vi that is greater than V volts and "OFF" for any lesser voltage.

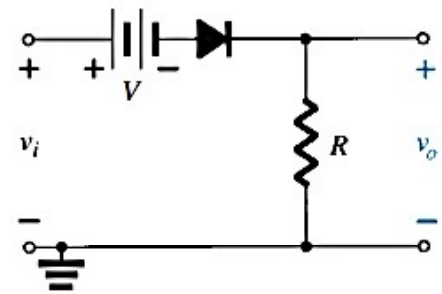


Fig.2: Series clipper with DC supply

General instructions for analysis: (cont….)

3. **Determine the "transition voltage" that will result in a change of state for the diode from the "OFF" to the "ON" state.**

- This step will help to define a region of the applied voltage when the diode is "ON" and when it is "OFF".
- For an ideal diode this will occur when $V_D = 0$ V and $I_D = 0$ mA.
- For the approximate equivalent (non-ideal diode) this is determined by finding the applied voltage when the diode has a drop of 0.7 V across it (for silicon) and I_D 0 mA.
- Note the substitution of the short-circuit equivalent for the ideal diode in **Fig 3**, and the fact that the voltage across the resistor is 0 V because the diode current is 0 mA. The result is v_i **-V = 0 or** v_i **= V** is the applied (transition) voltage.
- This permits drawing a line on the sinusoidal supply voltage as shown in **Fig. 4** to define the regions where the diode is on and off.

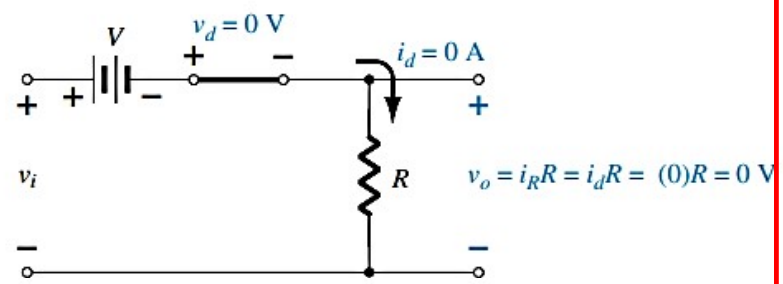


Fig. 3: Determining applied voltage for the circuit

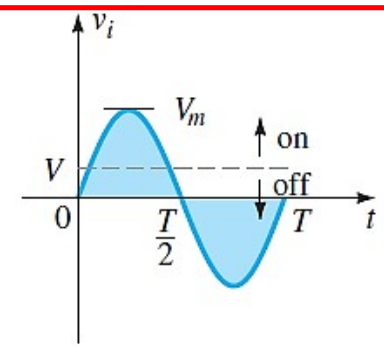


Fig.4: Define the "ON" and "OFF" regions.

General instructions for analysis: (cont….)

- For the "ON" region, as shown in **Fig. 5**, the output voltage is defined by-
  - $v_o = v_i - V$ ……. **(1)**
- For the "OFF" region, the diode is an open circuit, $I_D = 0$ mA, and the output voltage is
  - $v_o = 0\ V$ ……...**(2)**

4. It is often helpful to draw the output waveform directly below the applied voltage using the same scales for the horizontal axis and the vertical axis.

- For the "ON" condition, **Eq. (1)** can be used to find the output voltage when the applied voltage has its peak value:
  - $v_{o_peak} = V_m - V$ ……..*(3)*
  - Output voltage, v_o is plotted in the **Fig. 6**.

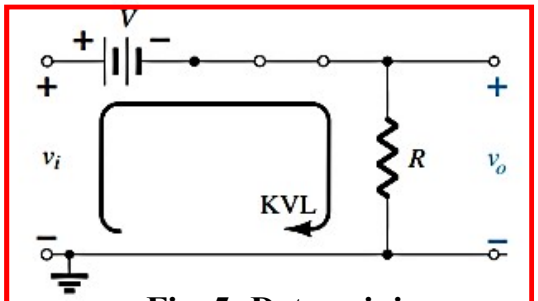


Fig. 5: Determining v_o for the diode in the "ON" state.

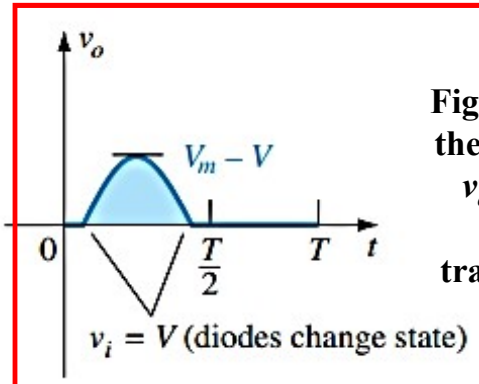


Fig. 6: Sketching the waveform of v_o above and below the transition level.

EXAMPLE 1: Determine the output waveform for the sinusoidal input of Fig. 7.

Step 1: The output is directly across the resistor R.

Step 2: The positive region of v_i and the dc supply are both working in same direction to turn the diode "ON". The result is that we can safely assume the diode is in the "on" state for the entire range of positive voltages for v_i .

Once the supply goes negative, it would have to exceed the dc supply voltage of 5 V before it could turn the diode "OFF".

Step 3: The transition model is substituted in **Fig. 8**, and we find that the transition from one state to the other will occur when,

$$v_i + 5V = 0V$$

Or $$v_i = -5V \text{ .....(1)}$$

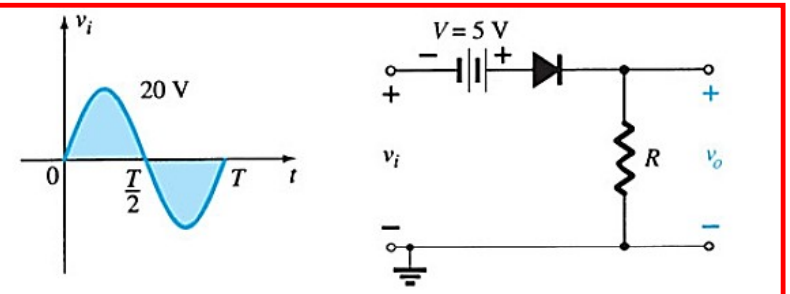


Fig. 7

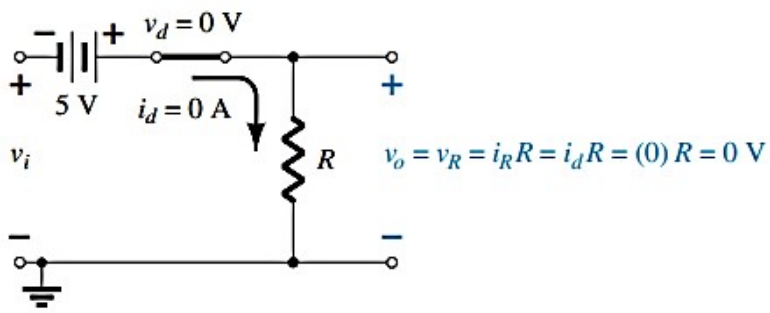


Fig. 8

EXAMPLE 1 (cont…..)

Step 4: In **Fig. 9** horizontal line is drawn through the applied voltage at the transition level.

For voltages less than 5V the diode is in the open-circuit state and the output is 0 V, as shown in the sketch of v_o .

Using **Fig. 9** , we find that for conditions when the diode is on and the diode current is established the output voltage will be the following, as determined using Kirchhoff's voltage law:

$$v_o = v_i + 5V \text{ ……..(2)}$$

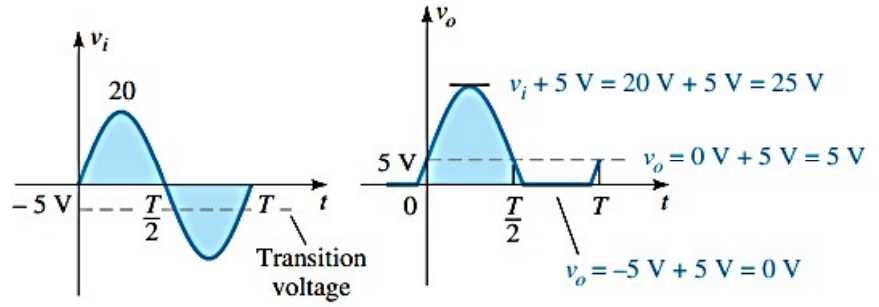


Fig. 9

Note: The analysis of clipper networks with square-wave inputs is actually easier than with sinusoidal inputs because only two levels have to be considered.

EXAMPLE 2: Find the output voltage for the network examined in previous Example, if the applied signal is the square wave of **Fig. 10**.

- For v_i = 20 V (0 → T/2) the network of **Fig. 11** results. The diode is in the short-circuit state i.e. "ON", and

  $v_o = 20\text{ V} + 5\text{ V} = 25\text{ V}$ ……(1)

- For v_i = -10 V (T/2 → T) the network of **Fig. 12**, results, moving the diode in the "OFF" state, and

  $v_o = i_R R = (0)R = 0\text{ V}$ ……..(2)

- The resulting output voltage appears in **Fig. 13**.

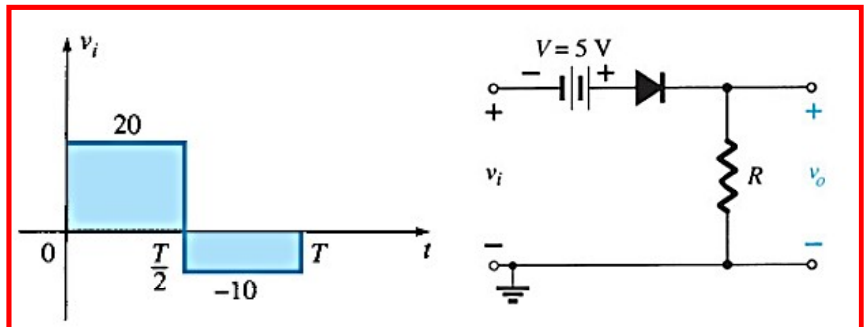


Fig. 10

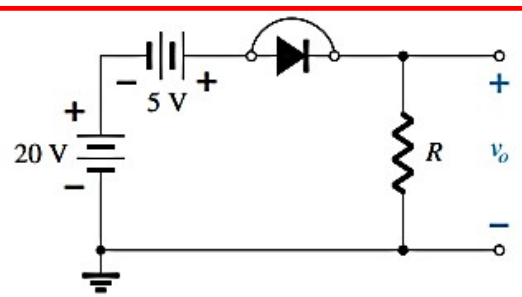


Fig. 11

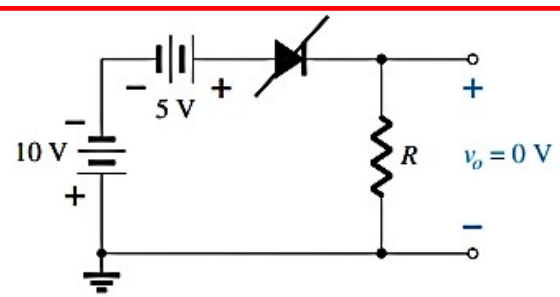


Fig. 12

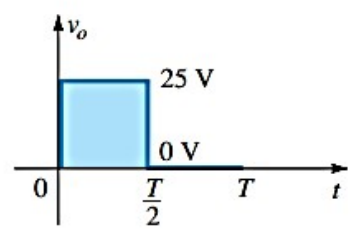


Fig. 13

Parallel Clippers without bias

- In parallel clippers, diode is connected in parallel with the load.
- The analysis of parallel configurations is very similar to that of series configurations.
- The simplest parallel clipper is shown in **Fig 14.**

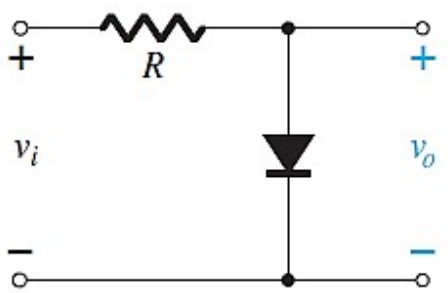


Fig. 14: Parallel Clipper

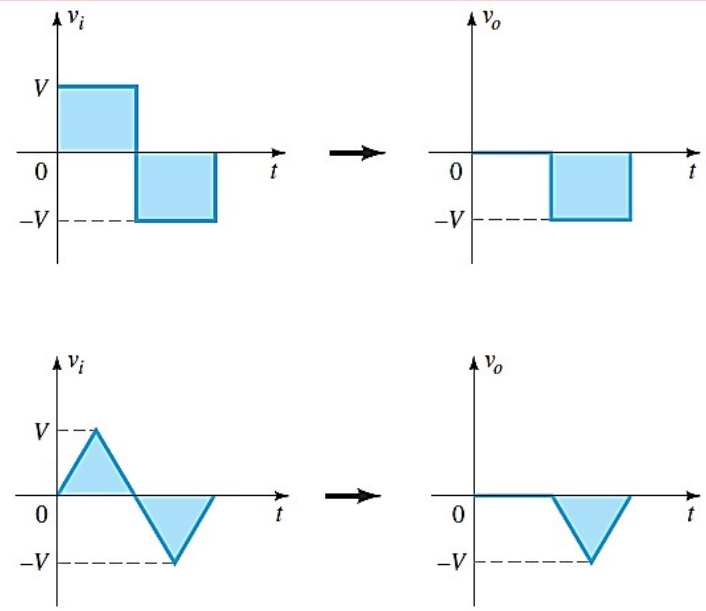


Fig. 15: Response to a parallel clipper.

EXAMPLE 3: Determine v_o for the network of Fig. 16.

Step 1: In this example the output is defined across the series combination of the 4-V supply and the diode, not across the resistor R.

Step 2: The polarity of the dc supply and the direction of the diode strongly suggest that the diode will be in the "ON" state for a good portion of the negative region of the input signal.

When the diode is in its short-circuit i.e. "ON" state the output voltage will be directly across the 4-V dc supply, requiring that the output be fixed at 4 V. In other words, when the diode is "ON" the output will be 4 V.

When the diode is an open circuit i.e. "OFF" state, the current through the series network will be 0 mA and the voltage drop across the resistor will be 0 V. That will result in $v_o = v_i$.

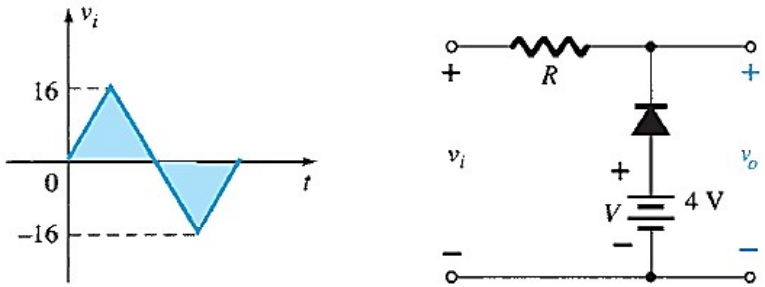


Fig. 16

Example 3 (cont….)

Step 3: The transition level of the input voltage can be found from **Fig. 17** by substituting the short-circuit equivalent and remembering the diode current is 0 mA at the instant of transition.
The result is a change in state when v_i = 4 V

Step 4: In **Fig. 18** the transition level is drawn along with v_o = 4 V when the diode is "ON".

Therefore, for v_i >= 4 V, v_o = v_i ……(1)

And, for v_i <= 4 V, v_o = 4 V, ……..……(2)

As shown in **Fig. 18**.

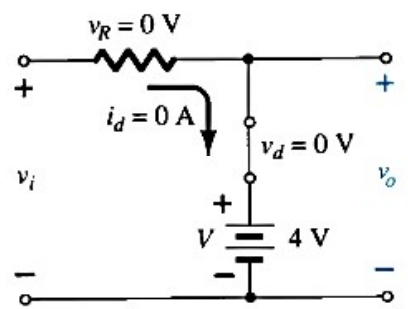


Fig. 17: Determining the transition level

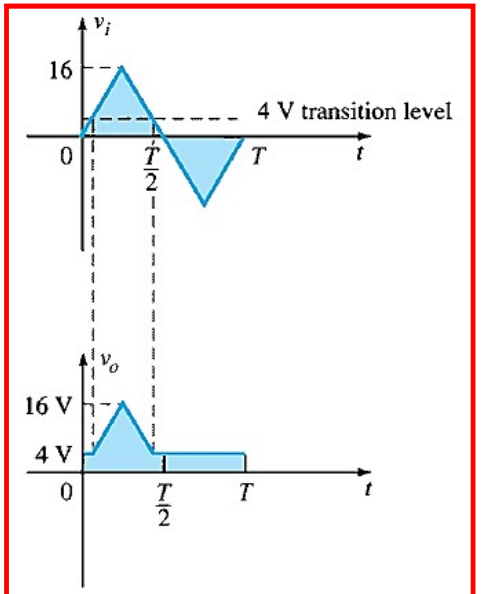


Fig. 18: Output Sketch

EXAMPLE 4: Repeat Example 3, using a **silicon diode with V_K = 0.7 V**.

- Determine Transition voltage
  - Using the condition $i_d = 0$ A at $v_d = V_D = 0.7$ V and obtaining the network of **Fig. 19** .
  - Applying KVL, $v_i + V_K - V = 0$
  - or $v_i = V - V_K = 4\text{ V} - 0.7\text{ V} = 3.3\text{ V}$ .....(1)
- Diode will be "OFF", for $v_i > 3.3$ V (in Fig. 19) and
  - $v_o = v_i$ ..... (2)
- Diode will be "ON", for $v_i < 3.3$ V (in Fig. 20) and
  - $v_o = 4\text{ V} - 0.7\text{ V} = 3.3\text{ V}$ .....(3)

- The resulting output waveform appears in **Fig. 21** .
- Note that the only effect of V_K was to drop the transition level to 3.3 from 4 V.

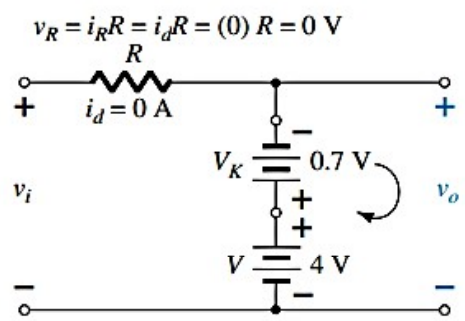


Fig. 19: Determining the output v_o

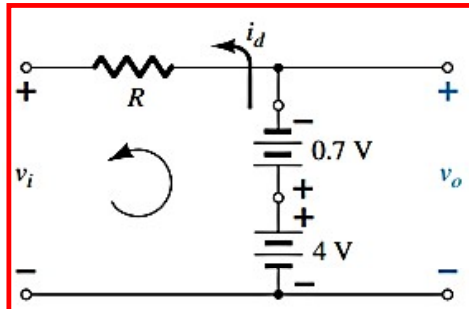


Fig. 20: Determining the output v_o

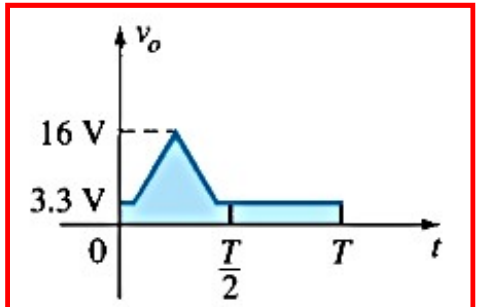
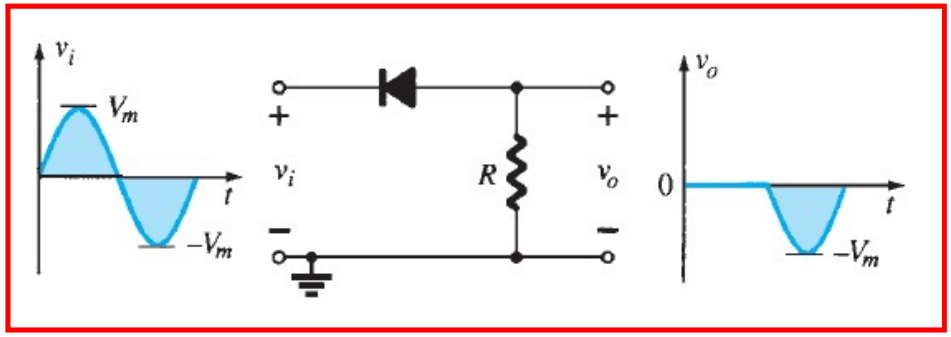


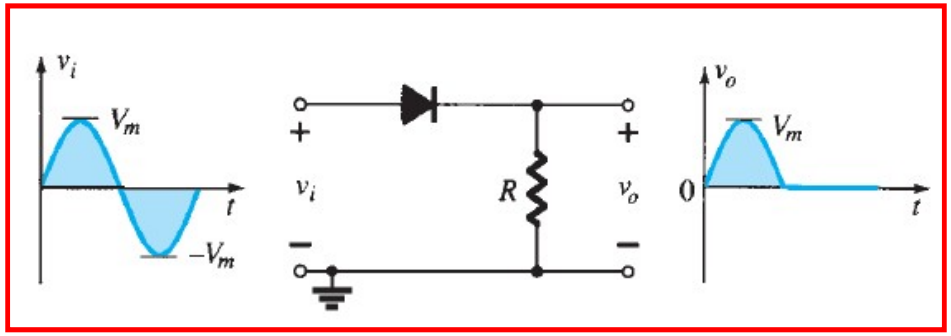
Fig. 21: Sketching v_o

Simple Series Clippers (Ideal Diodes)

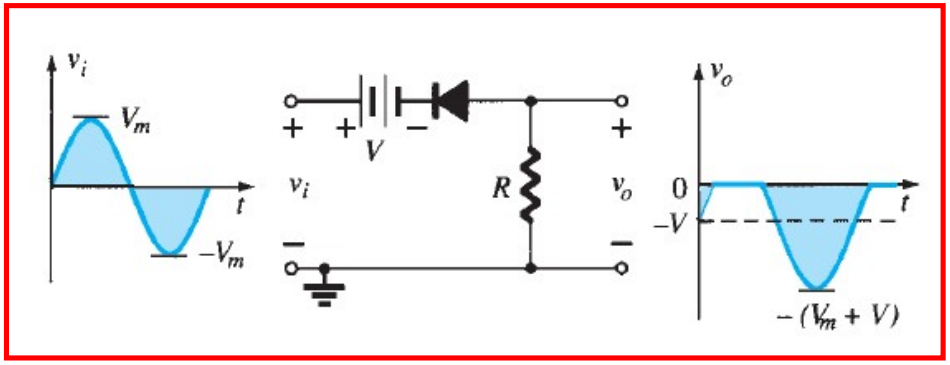


POSITIVE

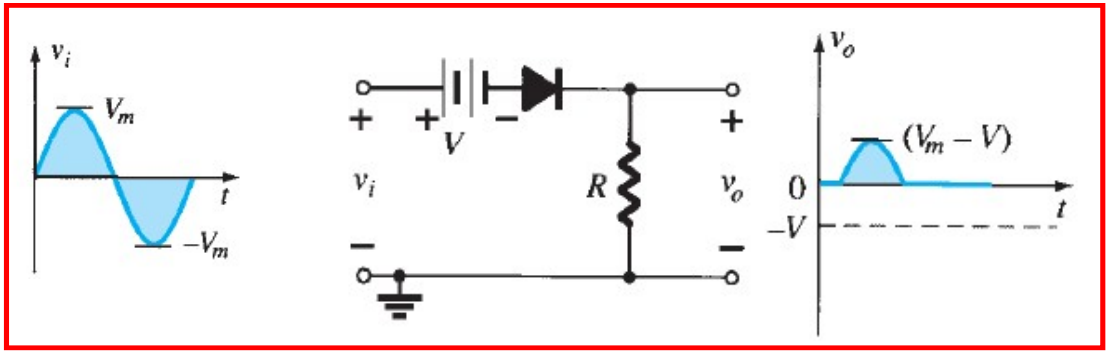
NEGATIVE



Biased Series Clippers (Ideal diodes)

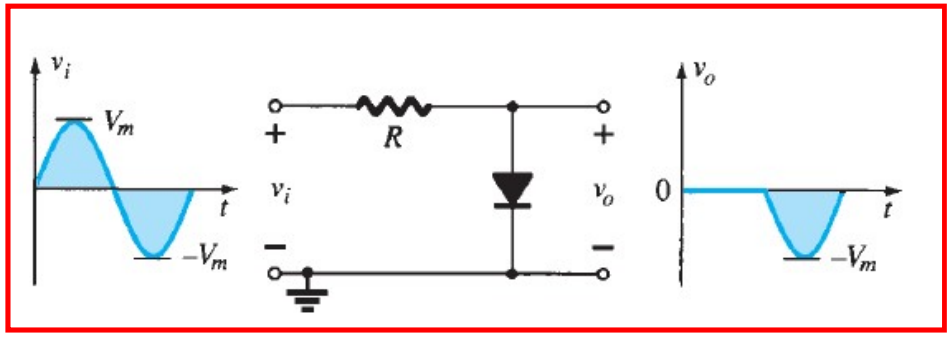


POSITIVE



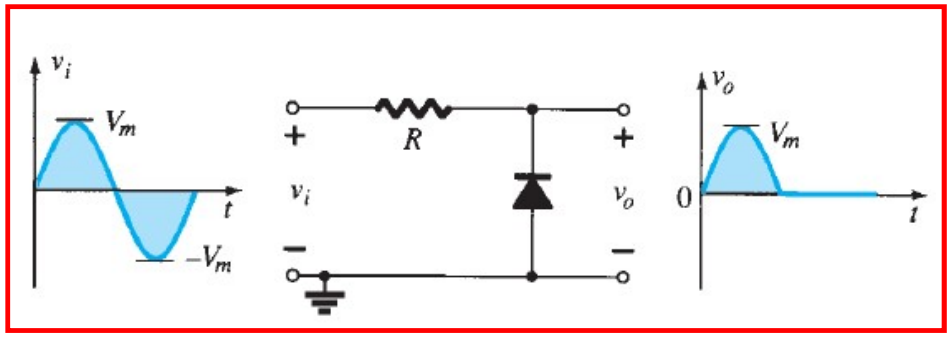
NEGATIVE

Simple Parallel Clippers (Ideal diodes)

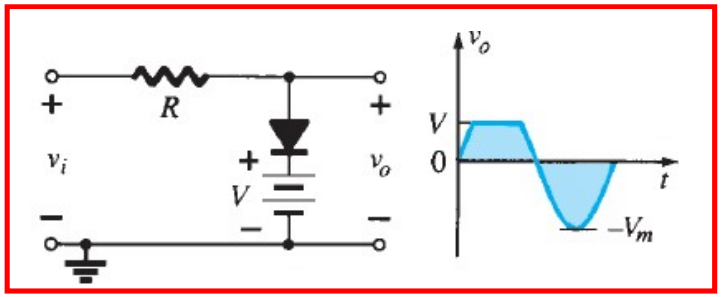


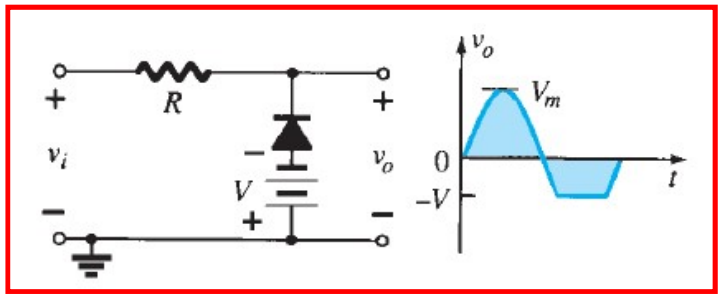
POSITIVE

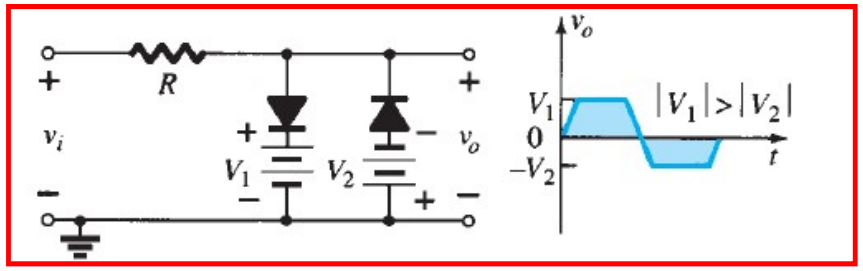
NEGATIVE



Biased Parallel Clippers (Ideal diodes)







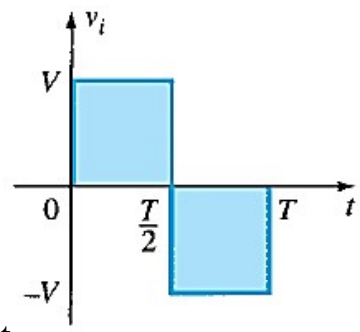
Topic:

CLAMPERS

Introduction

- A clamper is a circuit with a diode, resistor, and capacitor that shifts a waveform to a new DC level without altering its shape.

- Also known as DC restorer.



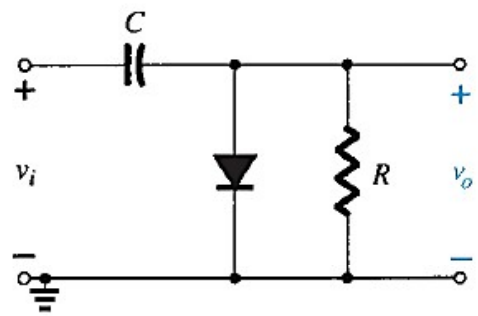


Fig.1: Clamper

- Clamping networks have a capacitor connected directly from input
- Resistive element connected in parallel with the output signal.
- The diode is also in parallel with the output signal but may or may not have a series dc supply as an added element.

Steps used for analysis:

Step 1: Examine the response of the portion of the input signal that will forward bias the diode.

- For Fig. 2, the diode is forward biased during the positive portion of the signal.
- The short-circuit equivalent for the diode results in $V_o = 0$ V for t = 0 to T/2 .

Step 2: During the on period of the diode, assume that the capacitor will charge up instantaneously to a voltage level determined by the surrounding network.

Step 3: Assume the capacitor retains its voltage while the diode is "off."

Step 4: Track the position and polarity of v_o to ensure correct levels.

- When the input turns negative, the network appears as in Fig. 3, with the diode as an open circuit and voltage stored across the capacitor.

Step 5: Check that the total swing of the output matches that of the input. (see Fig. 4)

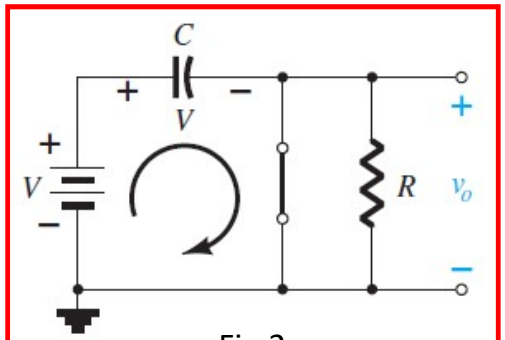


Fig.2

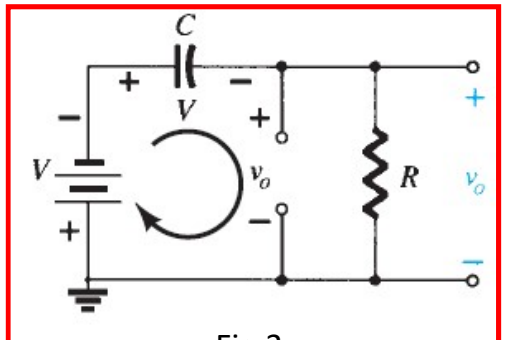


Fig.3

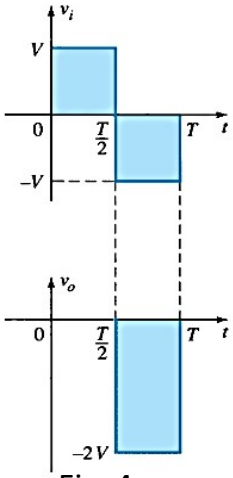


Fig. 4

Numerical

Example1: Determine v_o for the network of shown below, for the input indicated in Fig. 1.1

Solution:

Note: f = 1000 Hz => time period, T= 1 ms

<u>Step 1</u>: For *t1→ t2 of the* v_i since the diode is in its short-circuit state. The network appears as shown in Fig. 1.2 .

<u>Step 2</u>: The output is across *R (also directly across the 5-V battery)*. So, $v_o = 5$ *V.*

Applying KVL around the input loop

$-20\text{ V} + V_C - 5\text{ V} = 0$

and $V_C = 25$ *V* =>*the capacitor charges to 25 V.*

<u>*Step 3*</u>: For the period $t_2 \rightarrow t_3$ *the network will appear as shown in Fig. 1.3 .*

Applying KVL around the outside loop of the network

$+10\text{ V} + 25\text{ V} - v_o = 0$

$\boldsymbol{v_o = 35\text{ V}}$

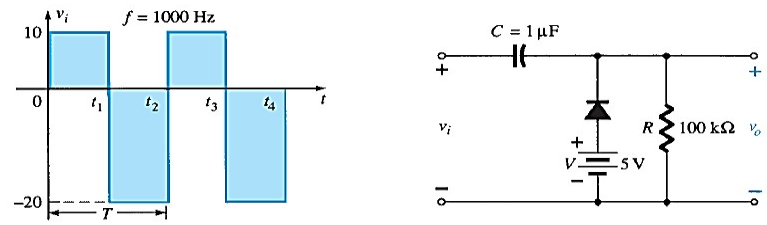


Fig. 1.1

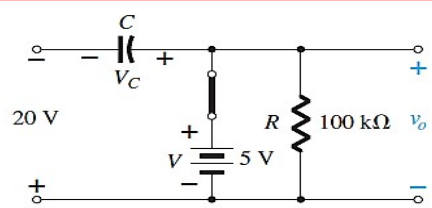


Fig. 1.2 : Determining V_o and V_C with the diode in the "on" state.

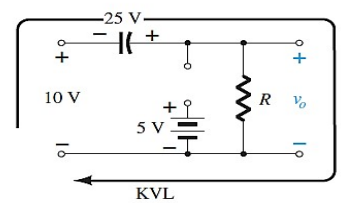


Fig. 1.3: Determining v_o with the diode in the "off" state.

Numerical

Step 4: The time constant of the network of Fig. 1.3 is determined by the product *RC and has the magnitude*
ζ = RC = (100 kΩ)(0.1 μF) = 0.01 s = 10 ms

The total discharge time is: 5 ζ = 5(10 ms) = 50 ms

Step 5: The resulting output appears in Fig. 1.4 with the input signal.
Note: The output swing of 30 V matches the input swing.

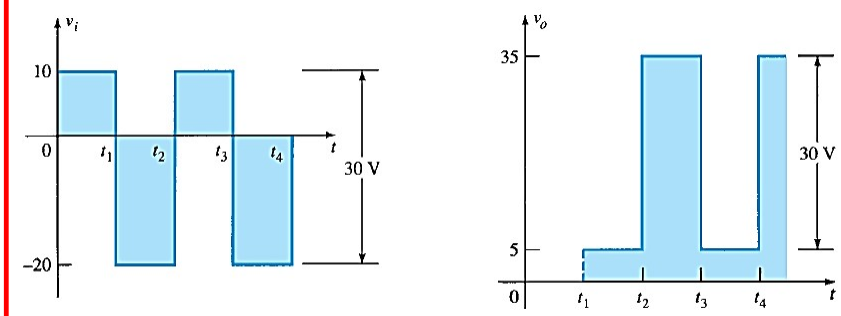


Fig. 1.4: Input and Output Waveform

Numerical

Example 2: Repeat example 1, using a silicon diode with V_k = 0.7 V.

Solution:

For the short-circuit state, the network appears as in Fig. 2.1 , and v_o *is determined by KVL in the output section as:*

+5 V - 0.7 V - $v_o = 0$

and $v_o = 4.3$ V

For the input section, KVL results in

-20 V + V_C + 0.7 V - 5 V = 0

and $V_C = 24.3$ V

For the period $t_2 \rightarrow t_3$ *the network will now appear as in Fig. 2.2 , with the only change* being the voltage across the capacitor.

Applying KVL yields

+10 V + 24.3 V - $v_o = 0$

and $\boldsymbol{v_o = 34.3}$ **V**

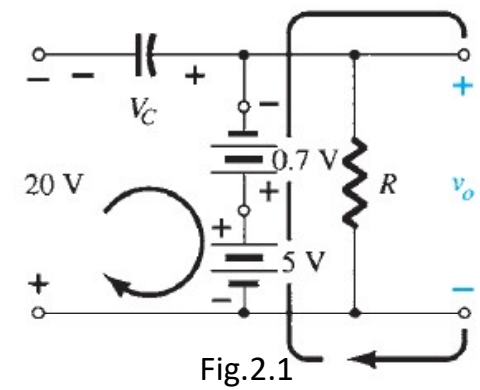


Fig.2.1

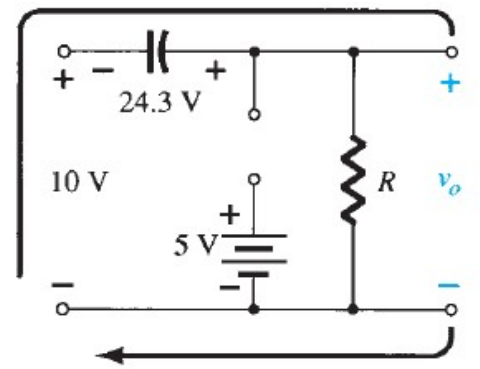


Fig.2.2

Numerical

The resulting output appears in Fig. 2.3 , verifying the statement that the input and output swings are the same.

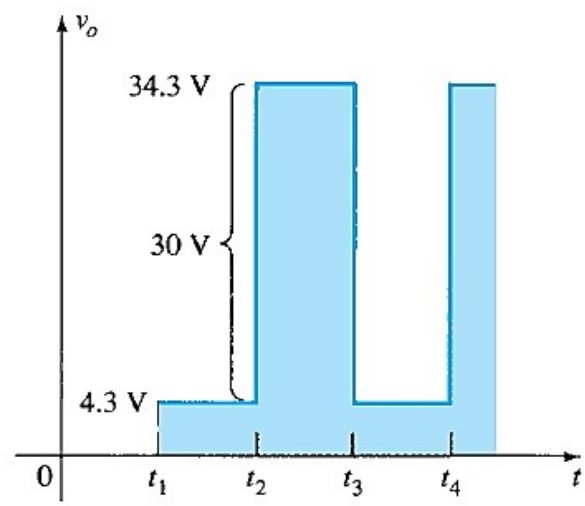
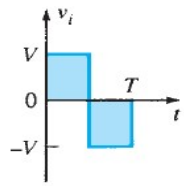
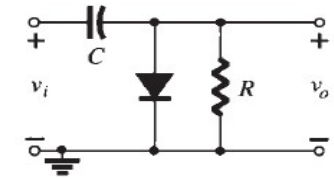
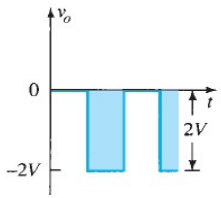
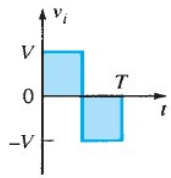
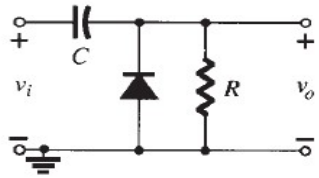
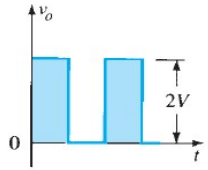
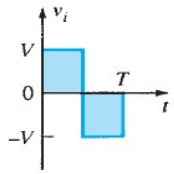
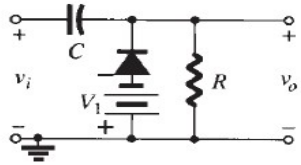
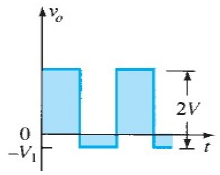


Fig. 2.3: Output Waveform

CLAMPING NETWORKS

Input Waveform	Clamping Circuit	Output Waveform
		
		
		

THANK YOU

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ELECTRONIC PRINCIPLES AND DEVICES

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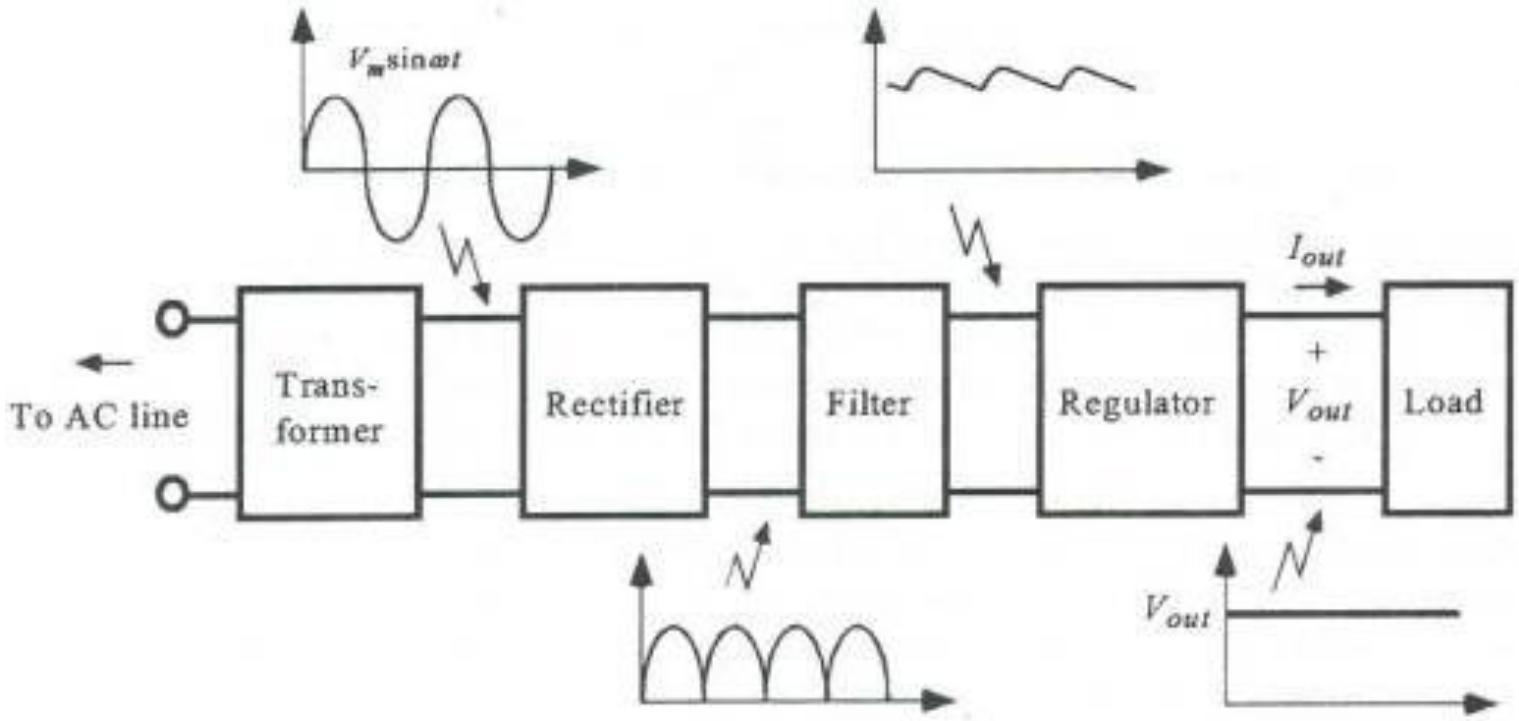
ELECTRONIC PRINCIPLES AND DEVICES

Semiconductor Diode applications

Department of Electronics and Communication.

ELECTRONIC PRINCIPLES AND DEVICES

Regulated Power Supply



Regulated Power Supply

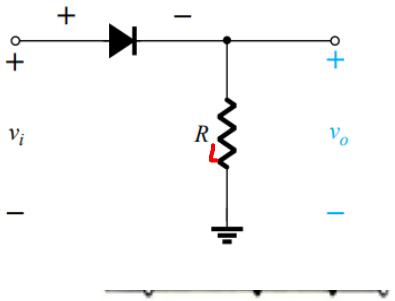
Regulated power supply converts an alternating current signal to a constant signal.

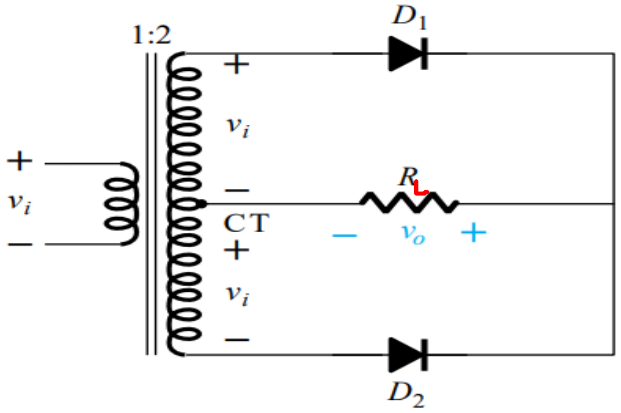
- **Transformer** : The output sinusoidal voltage is either step-up or step-down from the input sinusoidal voltage value
- **Rectifier** : Converts an alternating current into a direct one by allowing the current to flow through it in one direction only.
- **Filter** : Removes the AC ripples from the DC signal obtained from the rectifier.
- **Regulator** : Converts DC voltage into a lower constant voltage

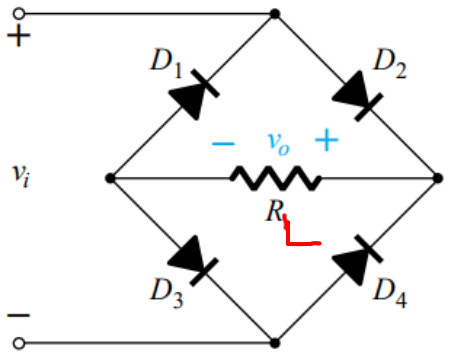
Rectifier

Rectifier

- Half wave rectifier
- Full wave rectifier
  - Centre Tapped Full Wave Rectifier
  - Bridge Rectifier



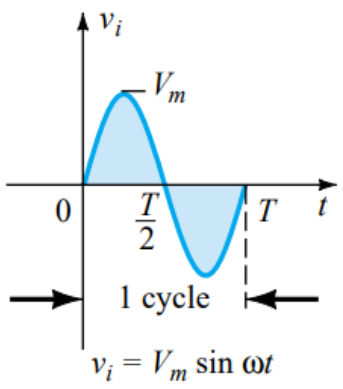




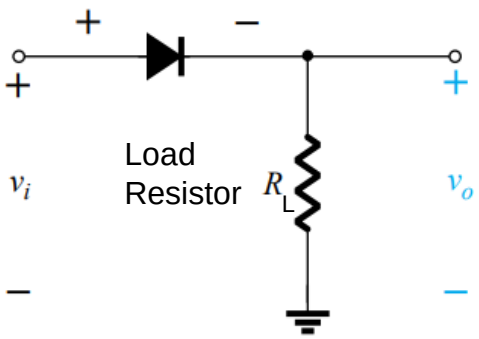
ELECTRONIC PRINCIPLES AND DEVICES

Half Wave Rectifier (HWR) - Ideal Diode

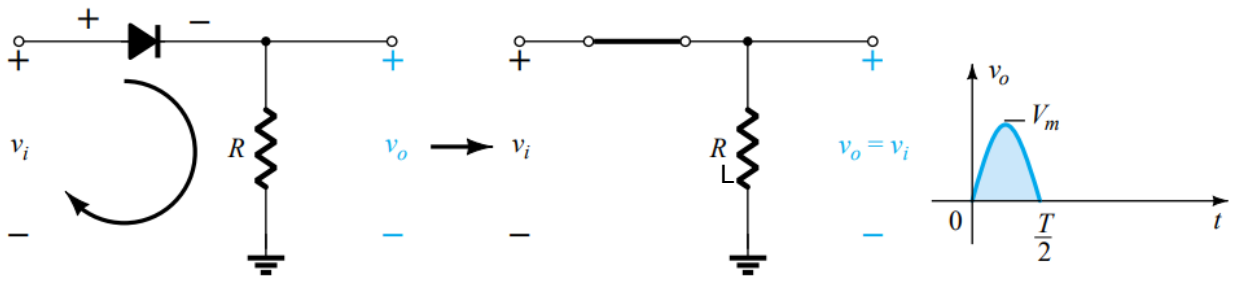
Input Waveform



HWR Circuit



Positive Half Cycle:

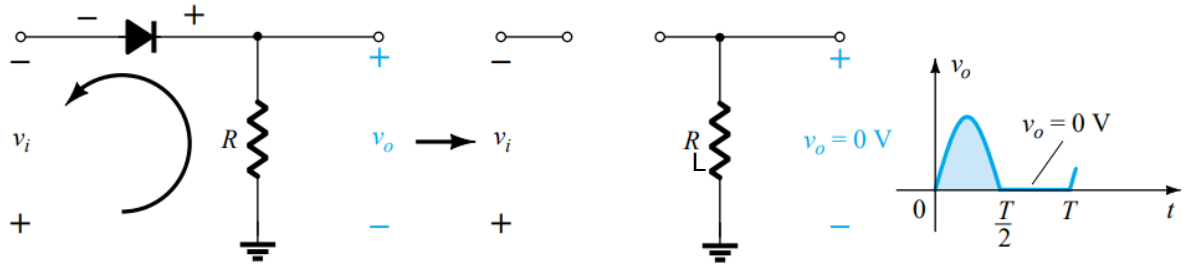


Conduction region ($0 \rightarrow T/2$).

$$I_m = \frac{V_m}{R_L}$$

$$V_o = V_m$$

Negative Half Cycle:

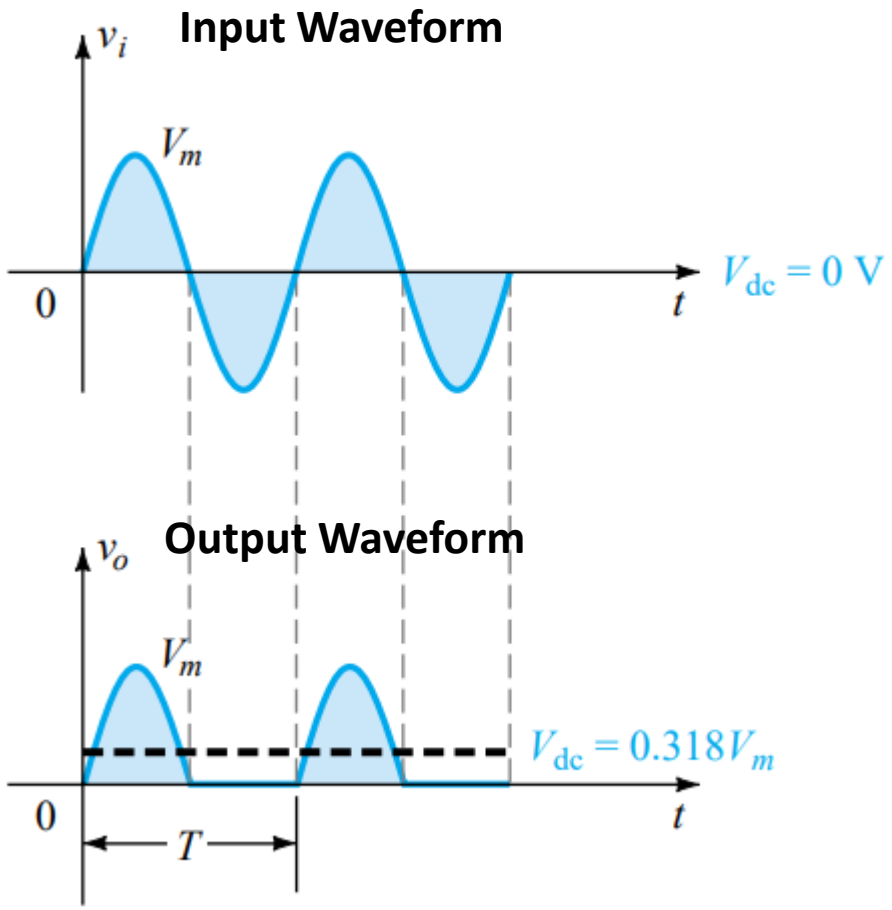


Nonconduction region ($T/2 \rightarrow T$).

I=0

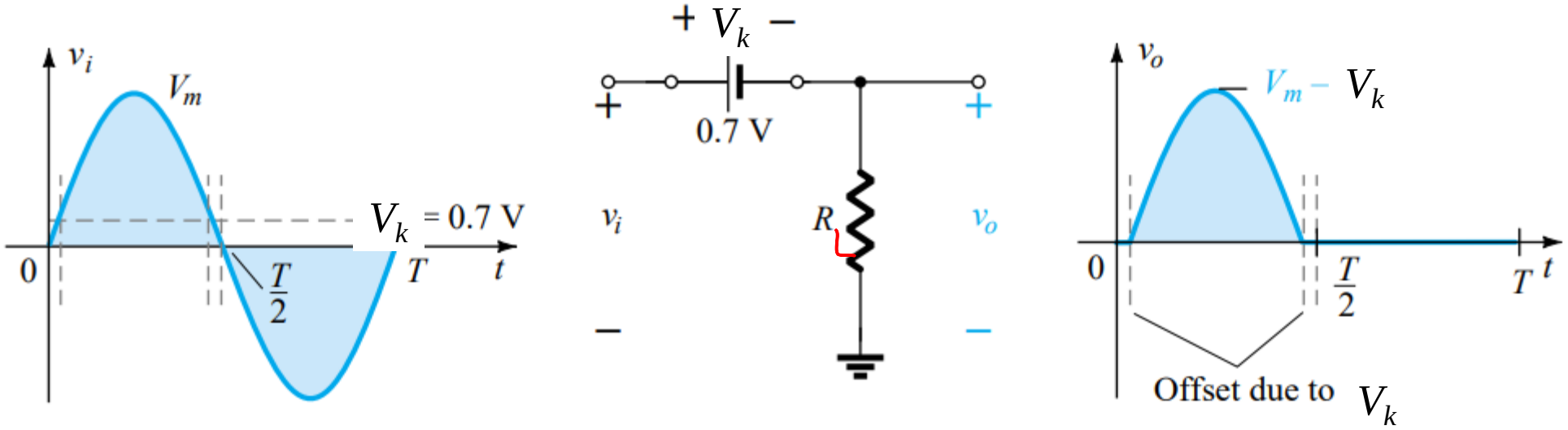
$$V_o = 0$$

Half Wave Rectifier (HWR) - Ideal Diode



Half Wave Rectifier (HWR) - Non Ideal Diode

Positive Half Cycle:

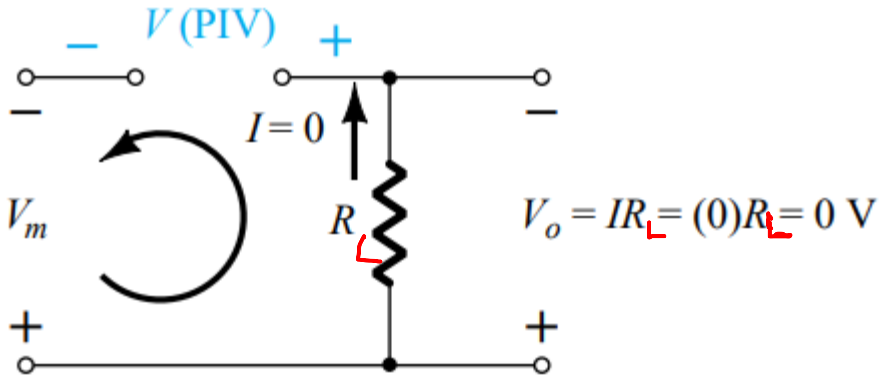


Effect of V_k on half-wave rectified signal.

$$\mathbf{V_{omax} = V_m - V_k}$$

$$I_{omax} = \frac{V_m - V_k}{R_l}$$

Half Wave Rectifier (HWR) PIV - Ideal Diode & Non Ideal Diode



PIV rating $\geqq V_m$ half-wave rectifier

Peak Inverse Voltage (PIV) or Peak Reverse voltage (PRV)- (For both Ideal & Non-Ideal) is the maximum reverse biased voltage (Vm) the diode can withstand without entering the breakdown region.

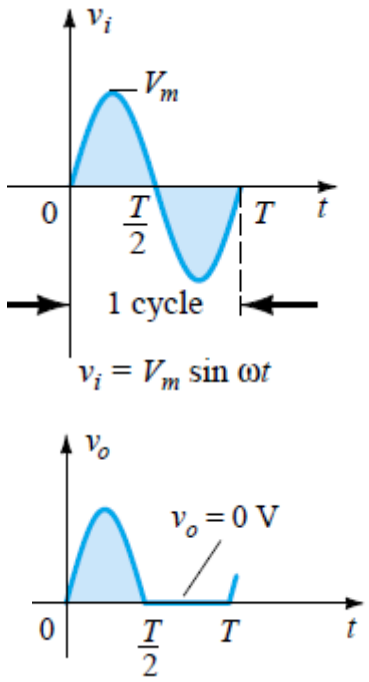
Determining Average voltage/Current for HWR - Ideal Diode

$$V_{dc} = \frac{1}{2\pi}\int_{0}^{2\pi} V_m \ sin\omega t \ d\omega t$$

$$= \frac{1}{2\pi}\int_{0}^{\pi} V_m \ sin\omega t \ d\omega t$$

$$= \frac{V_m}{2\pi}\left[-Cos\ \omega t\right]_0^{\pi} = \frac{V_m}{\pi}$$

$$\boxed{I_{dc} = \frac{V_{dc}}{R_L} = \frac{V_m}{\pi R_L} = \frac{I_m}{\pi}}$$



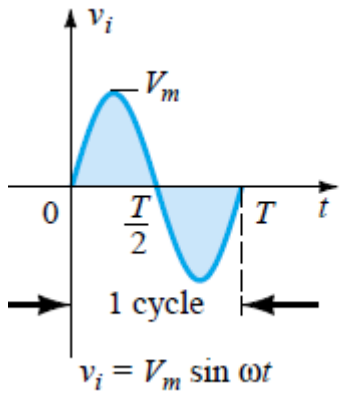
Determining RMS voltage/Current for HWR - Ideal Diode

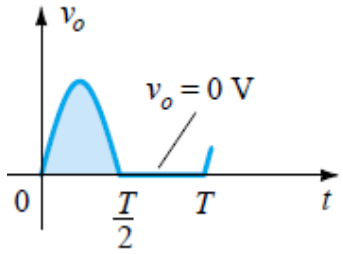
$$V_{rms} = \left[\frac{1}{2\pi}\int_0^{2\pi}(V_m sin\omega t)^2\, d\omega t\right]^{1/2}$$

$$= \left[\frac{V_m{}^2}{2\pi}\int_0^{\pi}(sin^2\,\omega t)\;\; d\omega t\right]^{1/2}$$

$$= \left[\frac{V_m{}^2}{2\pi}\int_0^{\pi}\left(\frac{1-Cos2\,\omega t}{2}\right)\;\; d\omega t\right]^{1/2}$$

$$V_{rms} = \left[\frac{V_m{}^2}{2\pi}\left(\frac{\omega t}{2}-\frac{sin2\omega t}{2}\right)_0^{\pi}\right]^{1/2} = \frac{V_m}{2}$$





$$I_{rms} = \frac{V_{rms}}{R_L} = \frac{V_m}{2R_L} = \frac{I_m}{2}$$

Determining Average & RMS voltage/Current for HWR – Non-Ideal Diode

$$V_{dc} = \frac{V_m - V_k}{\pi}$$

$$I_{dc} = \frac{V_{dc}}{R_L} = \frac{V_m - V_k}{\pi R_L} = \frac{I_m}{\pi} \qquad \left(I_m = \frac{V_m - V_k}{R_L} \right)$$

$$V_{rms} = \frac{V_m - V_k}{2}$$

$$I_{rms} = \frac{V_{rms}}{R_L} = \frac{V_m - V_K}{2R_L} = \frac{I_m}{2} \qquad \left(I_m = \frac{V_m - V_k}{R_L} \right)$$

Ripple factor of HWR

Ripple Factor is a measure of purity of the dc output of a rectifier and can be defined as

$$r = \frac{rms\ value\ of\ the\ ac\ component\ of\ the\ output}{average\ or\ dc\ value\ of\ the\ output}$$

$$V'_{rms} = \left[V_{rms}^2 - V_{dc}^2\right]^{1/2}$$

$$= \left[\left(\frac{V_m}{2}\right)^2 - \left(\frac{V_m}{\pi}\right)^2\right]^{1/2} = 0.385V_m$$

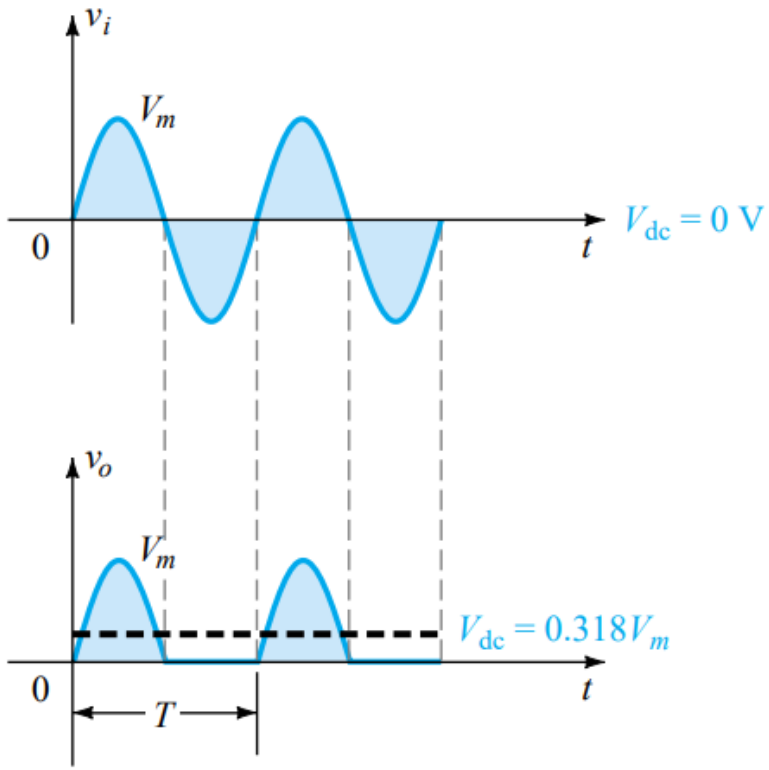
$$\text{Ripple Factor } (\gamma_{HWR}) = \frac{V'_{rms}}{V_{dc}} = \frac{\sqrt{V_{rms}^2 - V_{dc}^2}}{V_{dc}}$$

$$= \sqrt{\left(\frac{V_{rms}}{V_{dc}}\right)^2 - 1} = \sqrt{\left(\frac{V_m/2}{V_m/\pi}\right)^2 - 1}$$

$\therefore$ Ripple factor =1.21

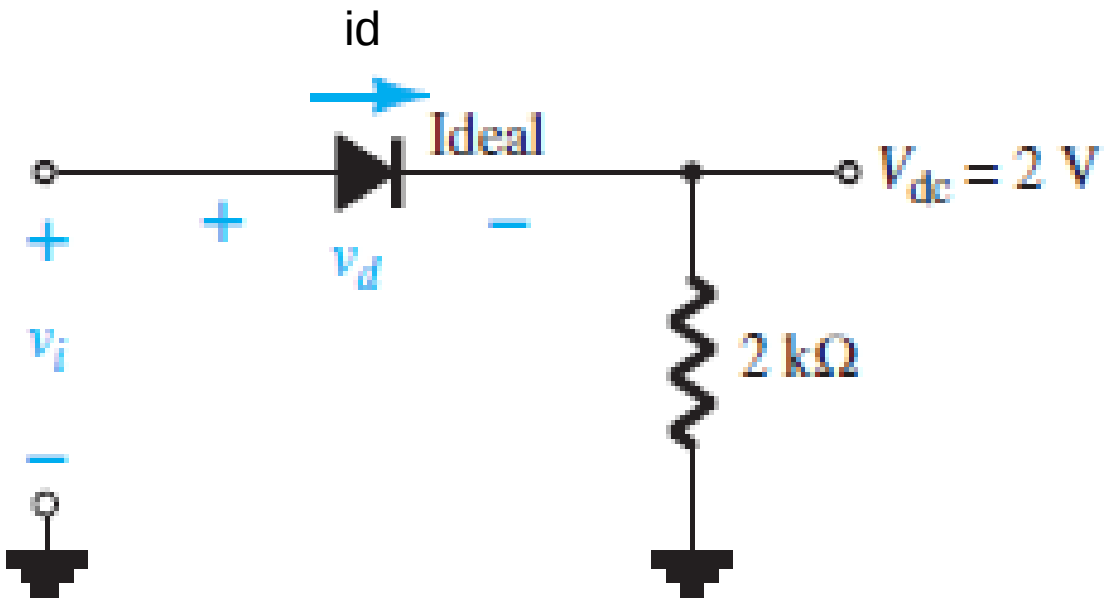
Frequency of HWR

The time duration of 1 cycle of input waveform is T and the time duration of 1 cycle of output wave form is also T , hence $fo = fi$



Numerical on HWR

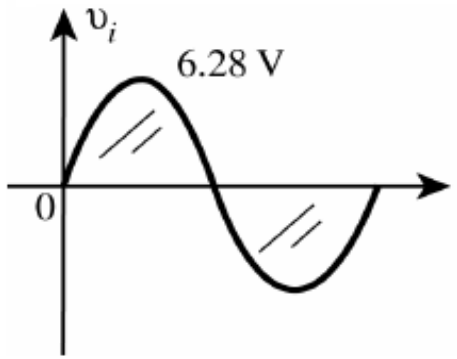
1. a) Assuming an ideal diode, sketch Vi, Vd, and id for the half-wave rectifier. The input is a sinusoidal waveform with a frequency of 60 Hz



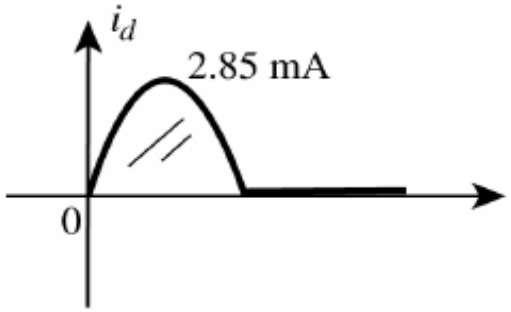
Numerical on HWR

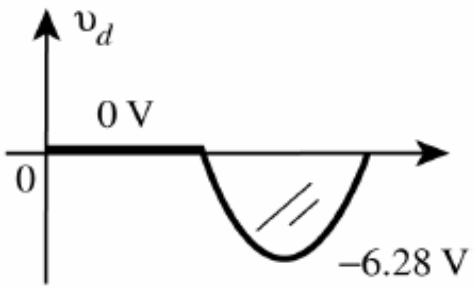
Solution:

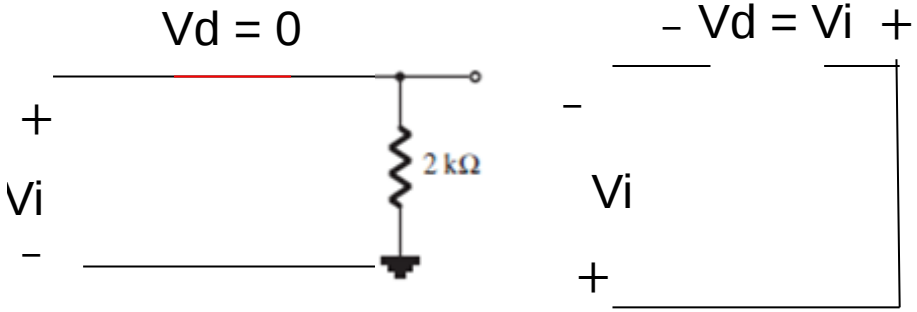
$$V_{dc} = 0.318\ V_m \Rightarrow V_m = \frac{V_{dc}}{0.318} = \frac{2\ \text{V}}{0.318} = \mathbf{6.28\ V}$$



$$I_m = \frac{V_m}{R} = \frac{6.28\ \text{V}}{2.2\ \text{k}\Omega} = \mathbf{2.85\ mA}$$

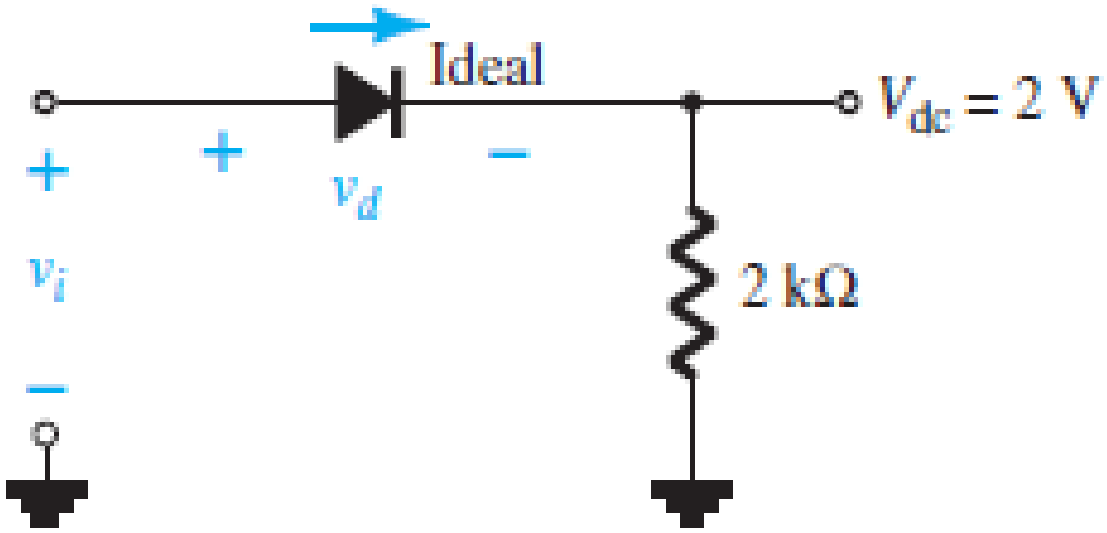






Numerical on HWR

1. b) Assuming a silicon diode (V_k=0.7 V), sketch *vi*, *vd*, and *id* for the half-wave rectifier . The input is a sinusoidal waveform with a frequency of 60 Hz



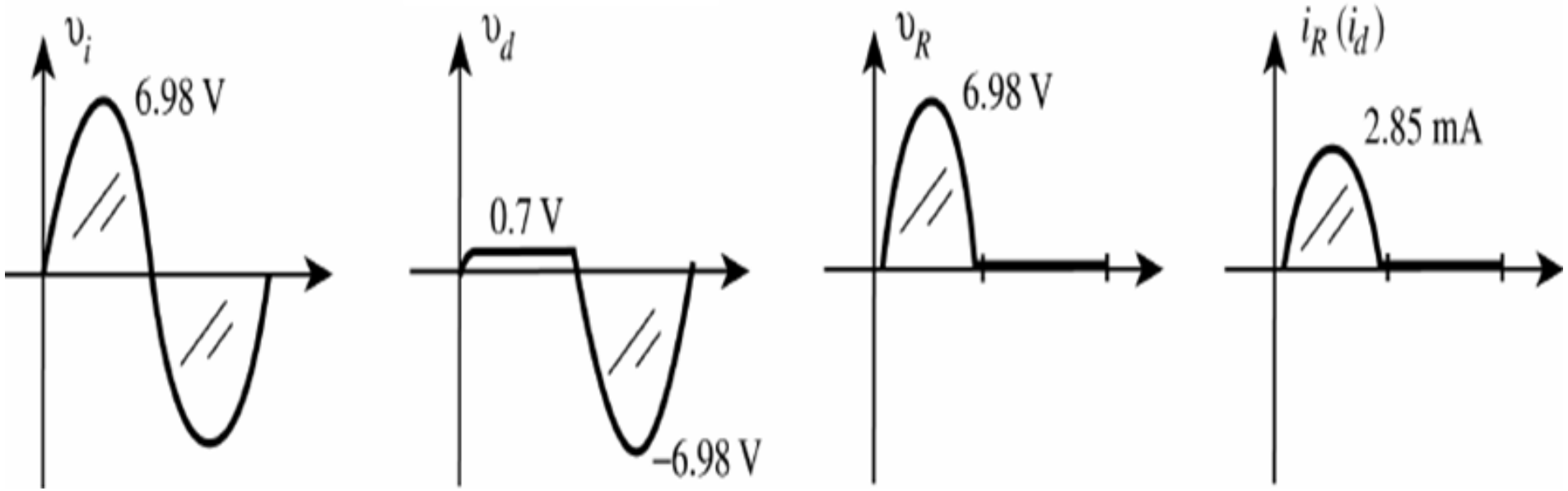
Numerical on HWR

Solution:

Using $V_{dc} \cong 0.318(V_m - V_\gamma)$

$$2\text{ V} = 0.318(V_m - 0.7\text{ V})$$

Solving: $V_m = \mathbf{6.98\ V}$



ELECTRONIC PRINCIPLES AND DEVICES

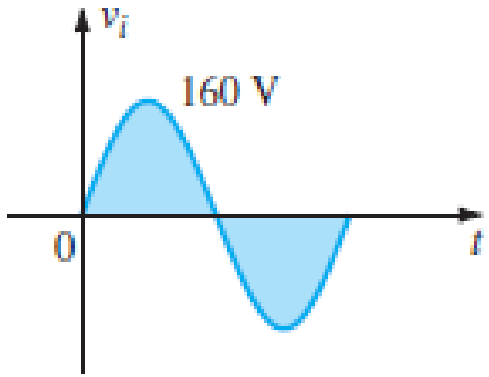
Numerical on HWR

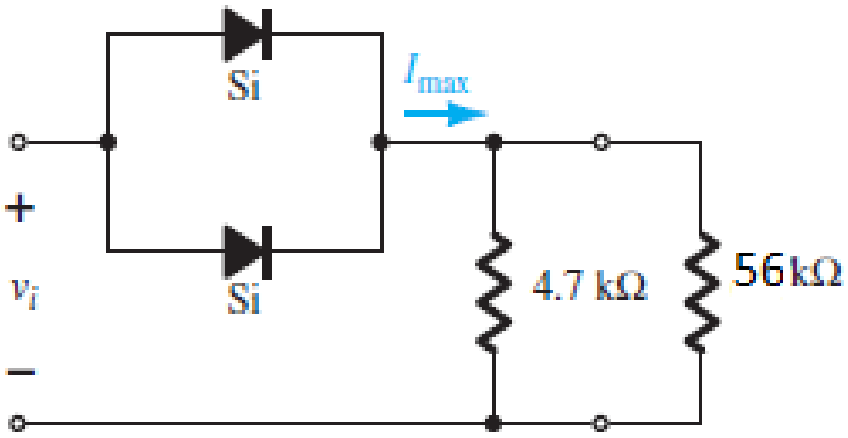
2. (a) Given Pmax= 14 mW for each diode shown, determine the maximum current rating of each diode (using the approximate equivalent model).

(b) Determine Imax for Vimax =160 V.

(c) Determine the current through each diode at Vimax using the results of part (b).

(d) If only one diode were present, determine the diode current and compare it to the maximum rating.





Numerical on HWR

Solution:

(a) $P_{max} = 14\text{ mW} = (0.7\text{ V})I_D$

$$I_D = \frac{14\text{ mW}}{0.7\text{ V}} = \mathbf{20\ mA}$$

(b) $4.7\text{ k}\Omega \parallel 56\text{ k}\Omega = 4.34\text{ k}\Omega$

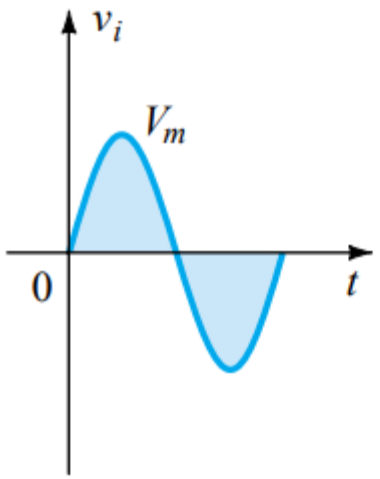
$V_R = 160\text{ V} - 0.7\text{ V} = 159.3\text{ V}$

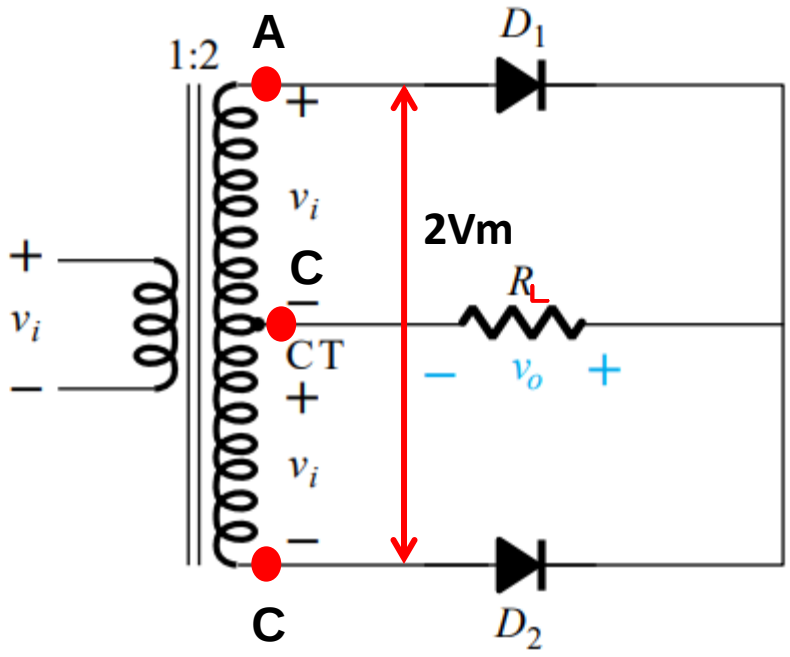
$$I_{max} = \frac{159.3\text{ V}}{4.34\text{ k}\Omega} = \mathbf{36.71\ mA}$$

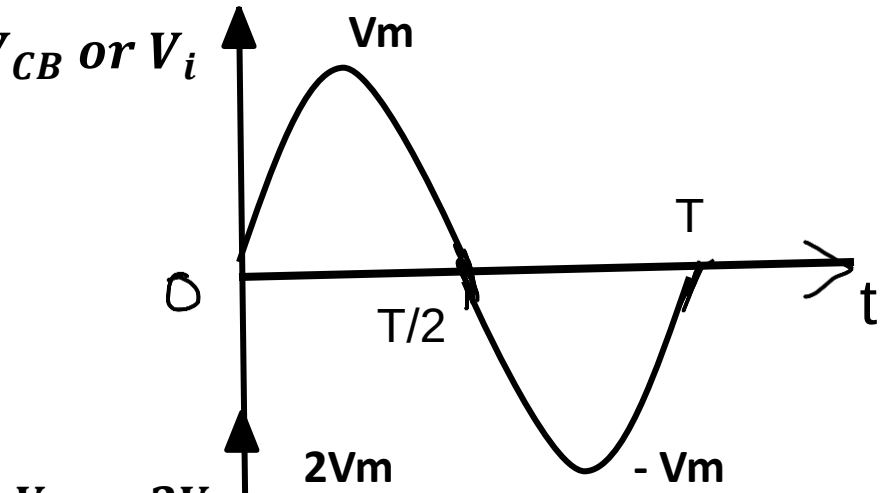
(c) $I_{diode} = \dfrac{I_{max}}{2} = \dfrac{36.71\text{ mA}}{2} = \mathbf{18.36\ mA}$ $\qquad I_D = 20\text{ mA} > 18.36\text{ mA}$

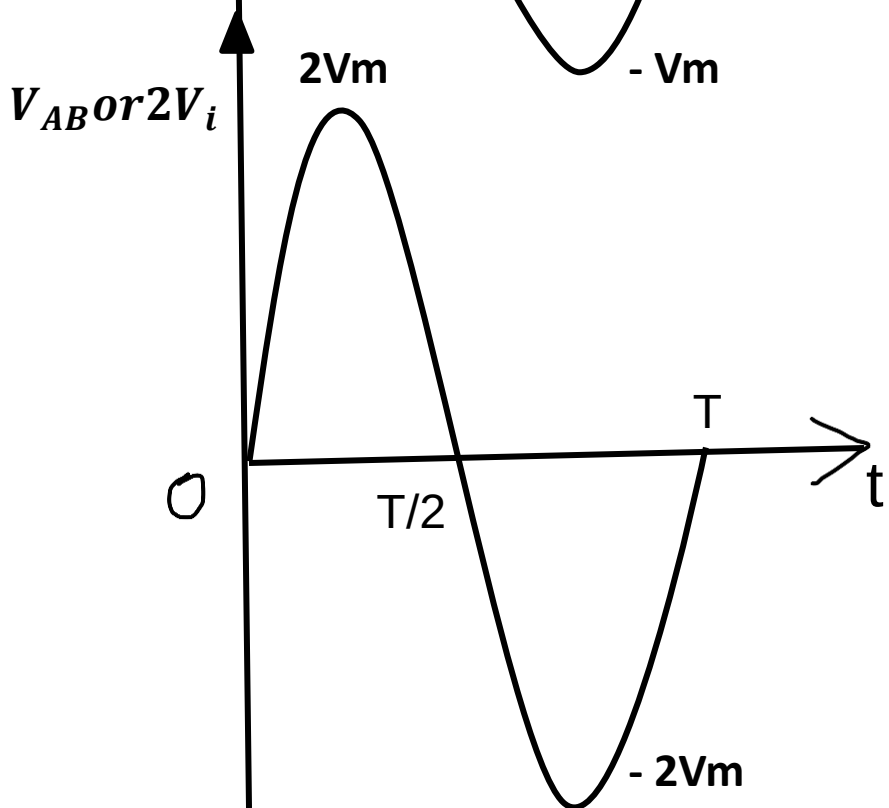
(d) $I_{diode} = 36.71\text{ mA} \gg I_{max} = 20\text{ mA}$ Total damage

Full Wave Rectifier : Centre Tap (Ideal Diode)



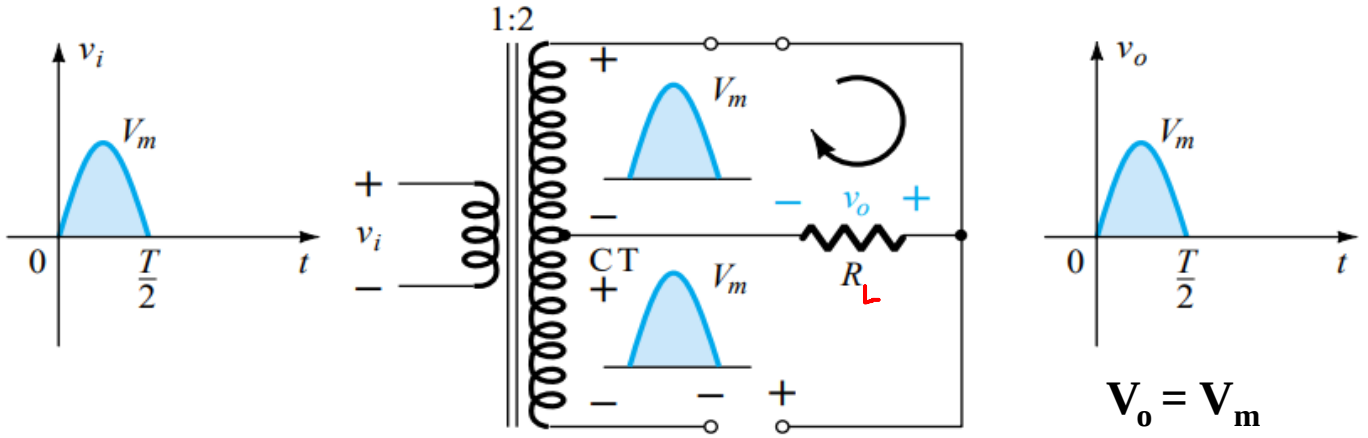






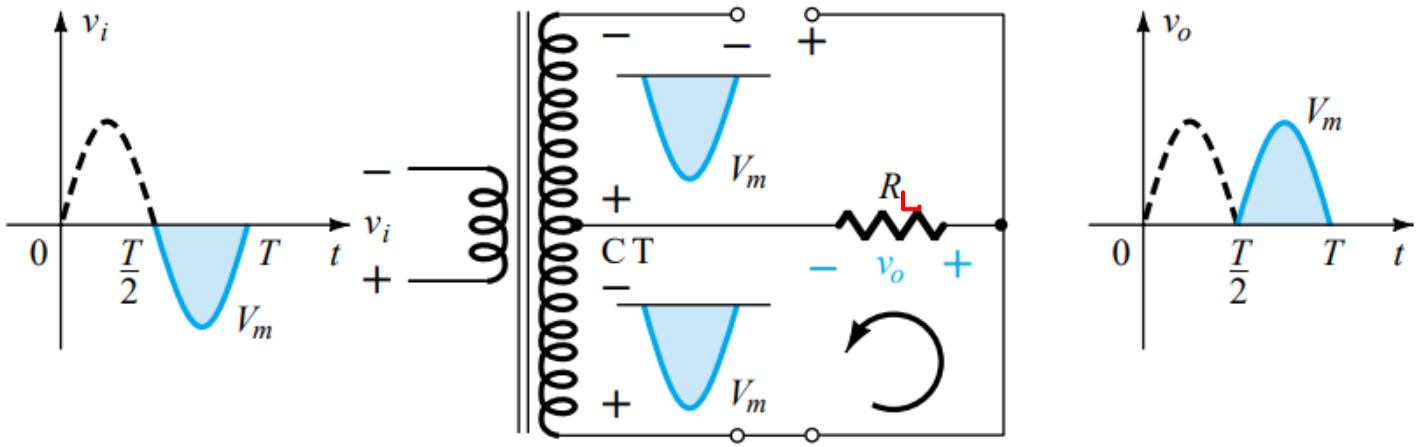
Full Wave Rectifier : Centre Tap (Ideal Diode)

Positive Half Cycle:



$V_o = V_m$ $\qquad$ $I_o = \frac{V_m}{R_L}$

Negative Half Cycle:

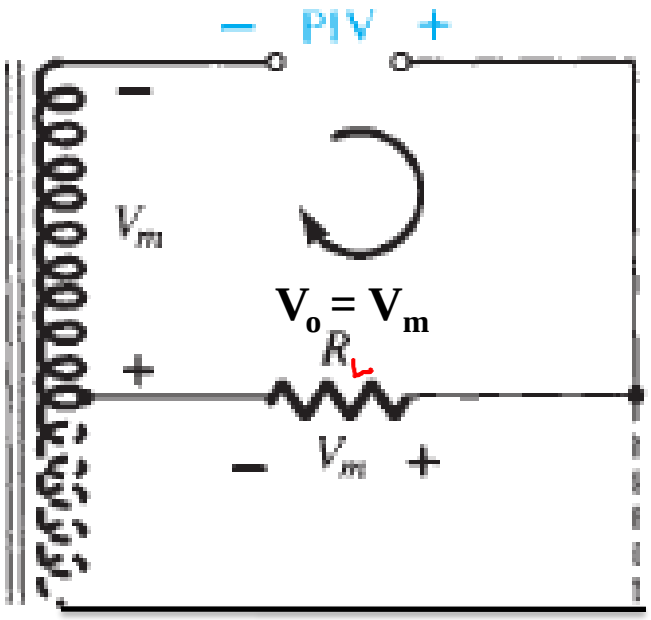


$V_o = V_m$

$I_m = \frac{V_m}{R_L}$

Full Wave Rectifier PIV - Centre Tap (Ideal Diode)

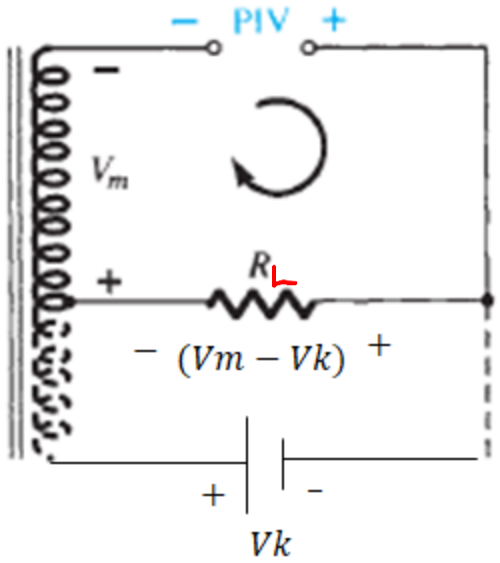
$$\text{PIV} = V_{\text{secondary}} + V_R$$
$$= V_m + V_m$$



$\boxed{\text{PIV} \geqq 2V_m}$ CT transformer, full-wave rectifier

Full Wave Rectifier : Centre Tap (Non Ideal Diode)

Negative Half Cycle:



$$V_{o\,max} = V_m - V_k$$

$$I_{o\,max} = \frac{V_m - V_k}{R_L}$$

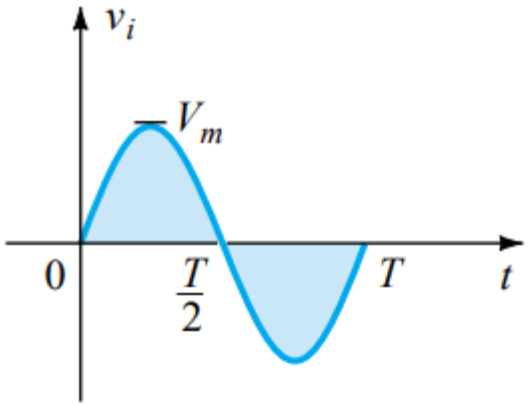
$$\text{PIV} - Vm + Vk - Vm = 0$$

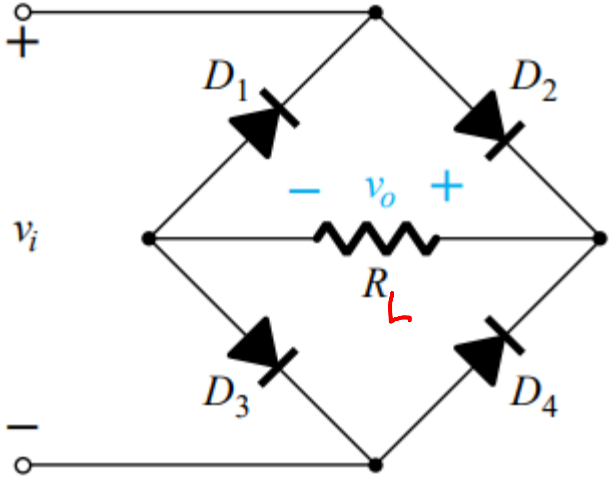
$$\text{PIV} - 2Vm + Vk = 0$$

$$\text{PIV} = 2Vm - Vk$$

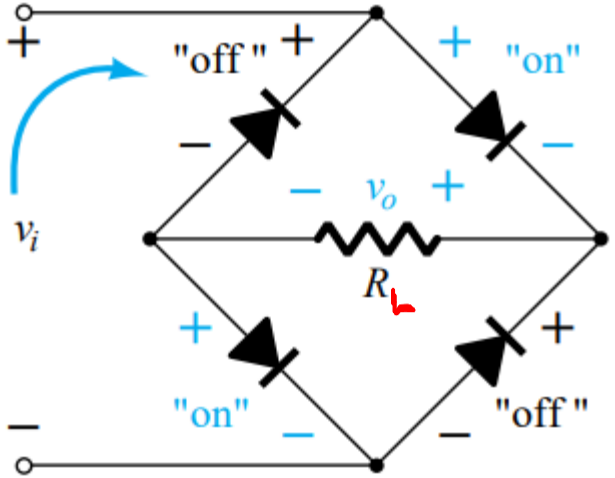
$$Non-\ Ideal\ diode:\ \text{PIV} \geq 2Vm - Vk$$

Full Wave Rectifier: Bridge Rectifier (Ideal Diode)



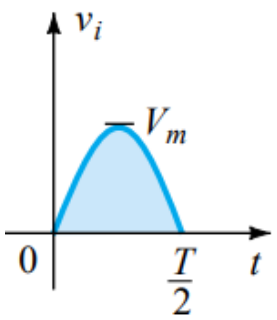


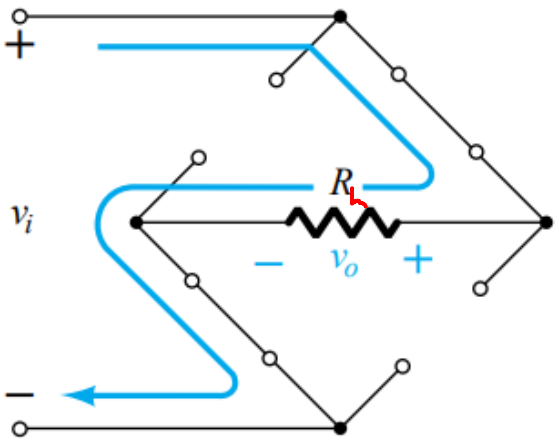
Positive Half Cycle:

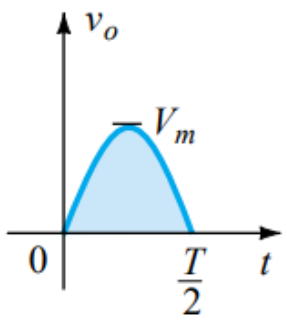


Full Wave Rectifier: Bridge Rectifier (Ideal Diode)

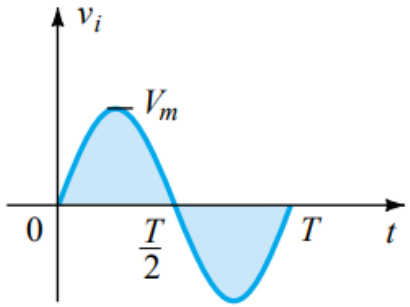
Positive Half Cycle:







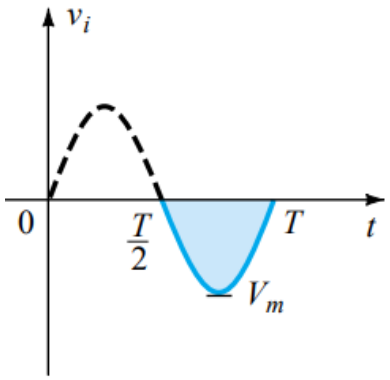
Input Waveform

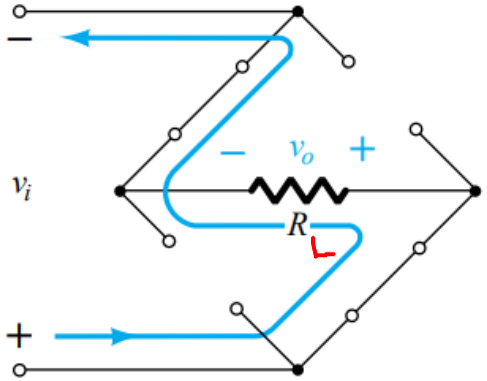


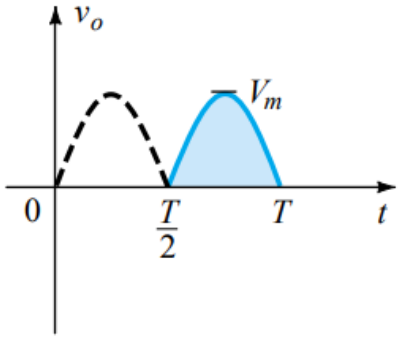
$$V_o = V_m$$

$$I_o = \frac{V_m}{R_L}$$

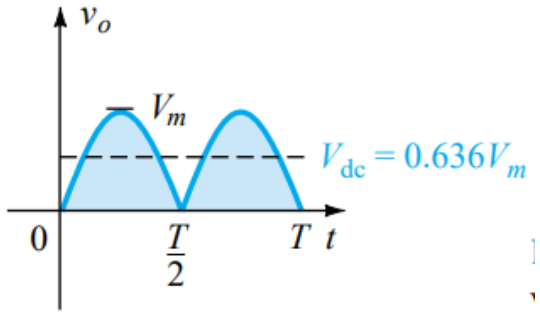
Negative Half Cycle:





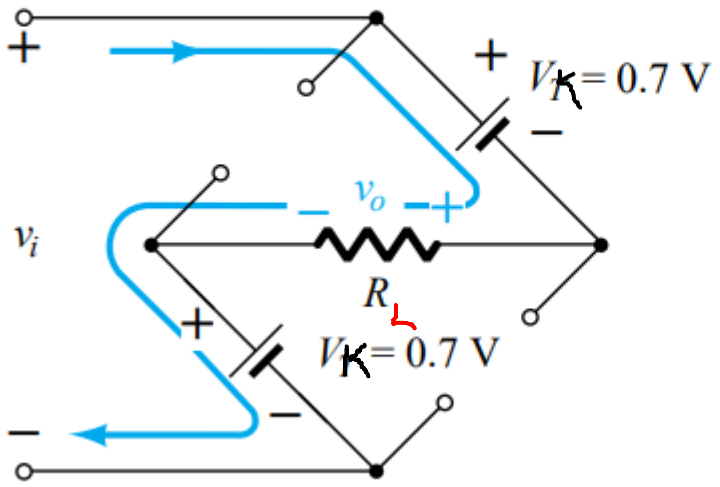


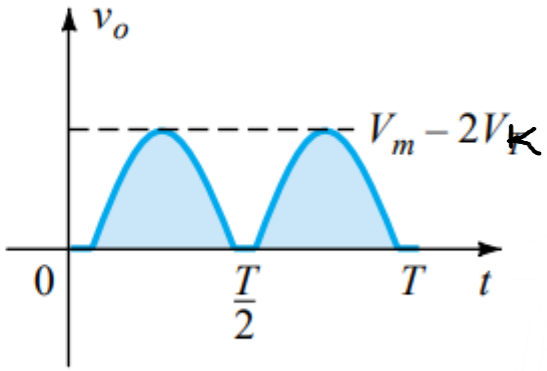
Output Waveform



Full Wave Rectifier: Bridge Rectifier (Non Ideal Diode)

$$V_{dc} \cong 0.636(V_m - 2V_K)$$





$$v_i - V_K - v_o - V_K = 0$$

$$v_o = v_i - 2V_K$$

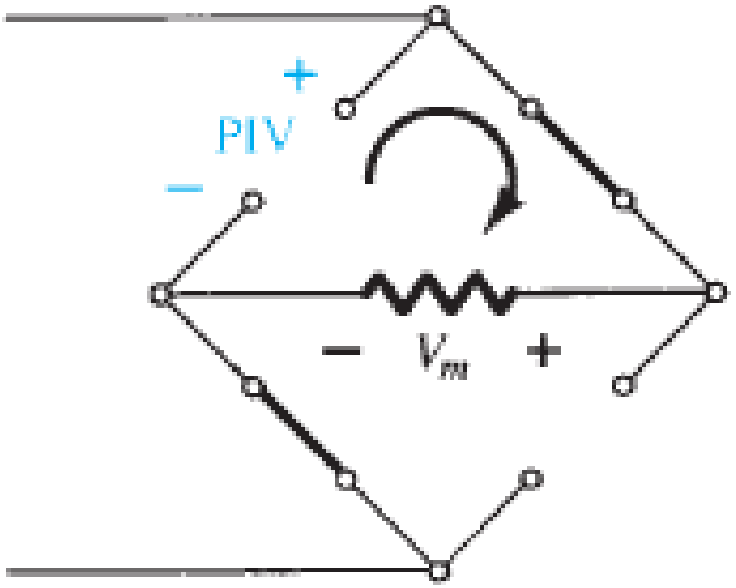
$$V_{o_{max}} = V_m - 2V_K$$

Full Wave Rectifier PIV : Bridge Rectifier (Ideal & Non-Ideal Diode)

Ideal diode: $\boxed{\text{PIV} \geqq V_m}$ full-wave bridge rectifier

$$\text{PIV} - Vm = 0$$

$$\text{PIV} = Vm$$



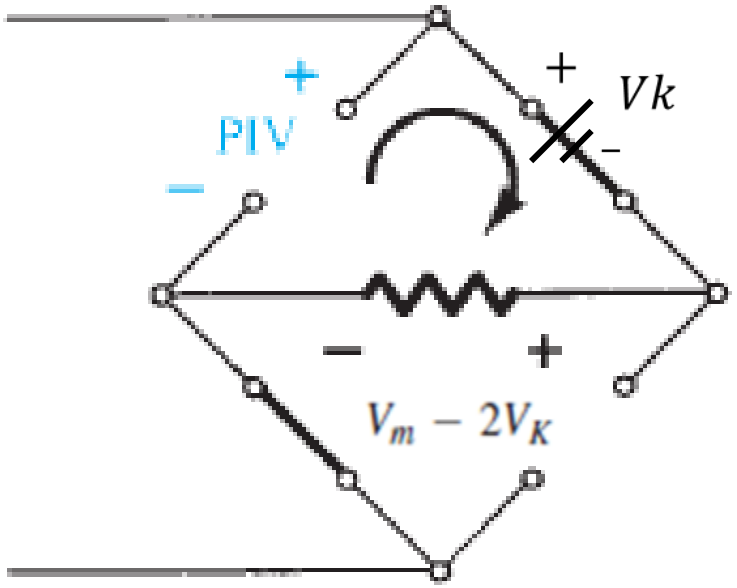
Non − Ideal diode: $\text{PIV} \geq Vm - Vk$

$$\text{PIV} - Vk - Vo = 0$$

$$\text{PIV} - Vk - Vm + 2Vk = 0$$

$$\text{PIV} + Vk - Vm = 0$$

$$\text{PIV} = Vm - Vk$$



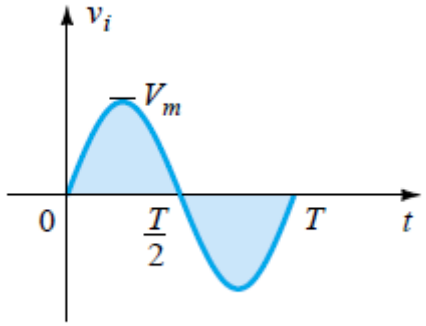
Determining Average voltage/ current for FWR (Ideal Diode)

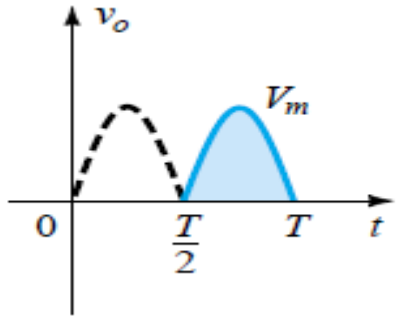
$$V_{dc} = \frac{1}{\pi}\int_0^{\pi} V_m \ sin\omega t \ d\omega t$$

$$= \frac{V_m}{\pi}\left[-Cos\ \omega t\right]_0^{\pi}$$

$$= \frac{2V_m}{\pi}$$

$$\boxed{I_{dc} = \frac{V_{dc}}{R} = \frac{2V_m}{\pi R} = \frac{2I_m}{\pi}}$$



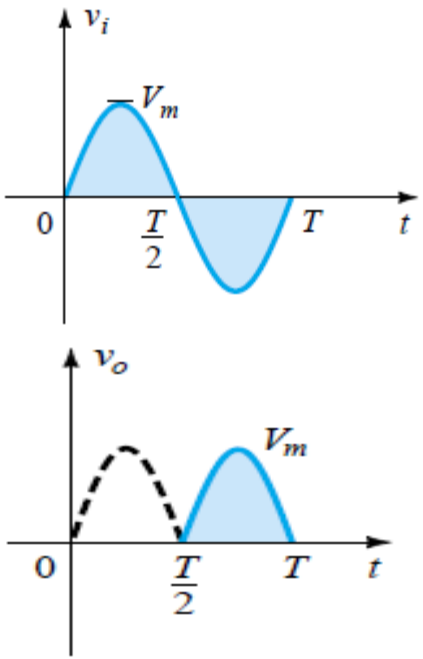


Determining RMS voltage/ current for FWR (Ideal Diode)

$$V_{rms} = \left[\frac{1}{\pi}\int_0^{\pi}(V_m sin\omega t)^2\ d\omega t\right]^{1/2}$$

$$= \left[\frac{V_m{}^2}{\pi}\int_0^{\pi}\left(\frac{1-Cos2\ \omega t}{2}\right)\ d\omega t\right]^{1/2}$$

$$= \left[\frac{V_m{}^2}{2\pi}\int_0^{\pi}(1-Cos2\ \omega t)\ d\omega t\right]^{1/2}$$



$$= \left[\frac{V_m{}^2}{2\pi}\left(\omega t_0^{\pi} - \frac{Sin2\ \omega t_0^{\pi}}{2}\right)\right]^{1/2} = \left[\frac{V_m{}^2}{2\pi}(\pi - 0)\right]^{1/2} = \frac{V_m}{\sqrt{2}}$$

$$I_{rms} = \frac{V_{rms}}{R} = \frac{V_m}{\sqrt{2}R} = \frac{I_m}{\sqrt{2}}$$

Average & RMS voltage/Current for Centre Tap Rectifier - Non Ideal Diode

$$V_{dc} = \frac{2(V_m - V_k)}{\pi}$$

$$I_{dc} = \frac{V_{dc}}{R_L} = \frac{2(V_m - V_k)}{\pi R_L} = 2\frac{I_m}{\pi} \qquad \left(I_m = \frac{V_m - V_k}{R_L}\right)$$

$$V_{rms} = \frac{V_m - V_k}{\sqrt{2}}$$

$$I_{rms} = \frac{V_{rms}}{R_L} = \frac{V_m - V_k}{\sqrt{2}R_L} = \frac{I_m}{\sqrt{2}} \qquad \left(I_m = \frac{V_m - V_k}{R_L}\right)$$

Average & RMS voltage/Current for Bridge Rectifier- Non ideal Diode

$$V_{dc} = \frac{2(V_m - 2V_k)}{\pi}$$

$$I_{dc} = \frac{V_{dc}}{R_L} = \frac{2(V_m - 2V_k)}{\pi R_L} = 2\frac{I_m}{\pi} \qquad \left(I_m = \frac{V_m - 2V_k}{R_L}\right)$$

$$V_{rms} = \frac{V_m - 2V_k}{\sqrt{2}}$$

$$I_{rms} = \frac{V_{rms}}{R_L} = \frac{V_m - 2V_k}{\sqrt{2}R_L} = \frac{I_m}{\sqrt{2}} \qquad \left(I_m = \frac{V_m - 2V_k}{R_L}\right)$$

Ripple factor of FWR

Ripple Factor is a measure of purity of the dc output of a rectifier and can be defined as

$$r = \frac{\text{rms value of the ac component of the output}}{\text{average or dc value of the output}}$$

$$V_{rms}^{I} = \sqrt{V_{rms}^{2} - V_{dc}^{2}}$$

$$= \sqrt{\left(\frac{V_m}{\sqrt{2}}\right)^2 - \left(\frac{2V_m}{\pi}\right)^2} = 0.307\, V_m$$

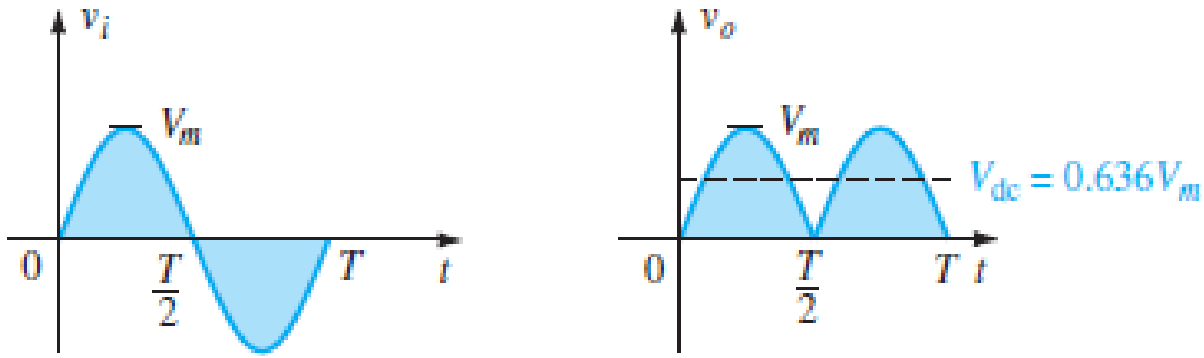
$$\text{Ripple Factor } (\gamma_{FWR}) = \frac{V'_{rms}}{V_{dc}} =$$

$$= \sqrt{\left(\frac{V_{rms}}{V_{dc}}\right)^2 - 1} = \sqrt{\left(\frac{V_m/\sqrt{2}}{2V_m/\pi}\right)^2 - 1}$$

$\therefore$ Ripple factor =0.48

FWR: Frequency

The time duration of 1 cycle of input waveform is T and the time duration of 1 cycle of output wave form is $T/2$, hence $fo=2\ fi$



Comparison Table for HWR & FWR

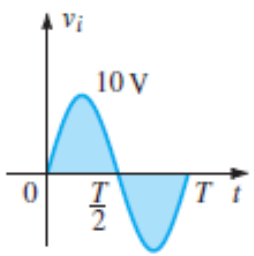
Measure	HWR Ideal	HWR Practical	CT-Ideal	CT-Practical	Bridge- Ideal	Bridge-Practical
I_{dc}	$\frac{I_m}{\pi}$	$\frac{I_m}{\pi}$	$\frac{2I_m}{\pi}$	$\frac{2I_m}{\pi}$	$\frac{2I_m}{\pi}$	$\frac{2I_m}{\pi}$
V_{dc}	$\frac{V_m}{\pi}$	$\frac{V_m - V_k}{\pi}$	$\frac{2V_m}{\pi}$	$\frac{2(V_m - V_k)}{\pi}$	$\frac{2V_m}{\pi}$	$\frac{2(V_m - 2V_k)}{\pi}$
I_{rms}	$\frac{I_m}{2}$	$\frac{I_m}{2}$	$\frac{I_m}{\sqrt{2}}$	$\frac{I_m}{\sqrt{2}}$	$\frac{I_m}{\sqrt{2}}$	$\frac{I_m}{\sqrt{2}}$
V_{rms}	$\frac{V_m}{2}$	$\frac{V_m - V_k}{2}$	$\frac{V_m}{\sqrt{2}}$	$\frac{V_m - V_k}{\sqrt{2}}$	$\frac{V_m}{\sqrt{2}}$	$\frac{V_m - 2V_k}{\sqrt{2}}$
PIV	V_m	V_m	$2V_m$	$2V_m - V_k$	V_m	$V_m - V_k$

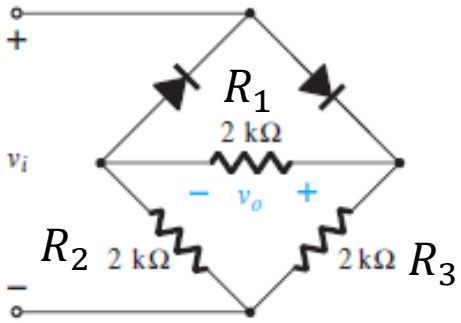
Differences between Centre Tap & Bridge FWR

Sl No.	Bridge-FWR	CT- FWR
1	Lesser PIV	Comparatively higher PIV
2	Centre tap transformer not required	Centre tap transformer required
3	Uniform input for both half cycles	Difficult to balance both the half cycles due to CT
4	4 diodes are required	2 diodes are required
5	More voltage drop due to two diodes in the path	Comparatively less voltage drop due to only one diode in the path

Numerical on Full Wave Rectifier: Bridge Rectifier

1.Determine the output waveform for the network and calculate the output dc level and the required PIV of each diode.



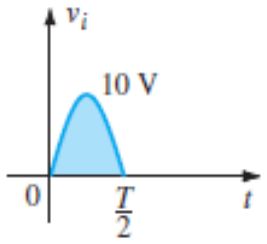


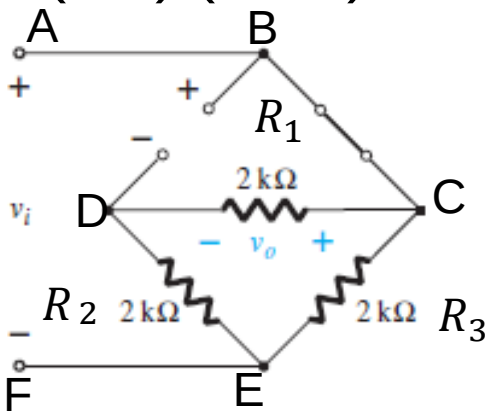
Solution:

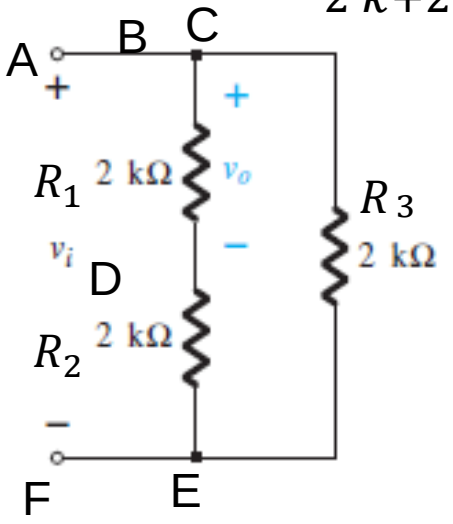
$$Voltage\ Divider\ Rule: \frac{V_i R_1}{R_1 + R_2} = V_0$$

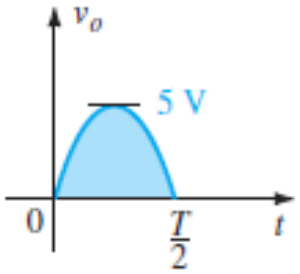
$$V_0 = \frac{10(2\,k)}{2\,k+2\,k} = 5\ V$$

$V_o$max = (2/4) Vimax = (2/4) (10 V) = 5 V

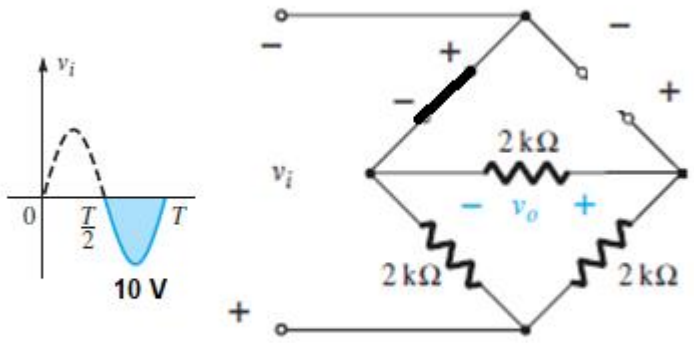


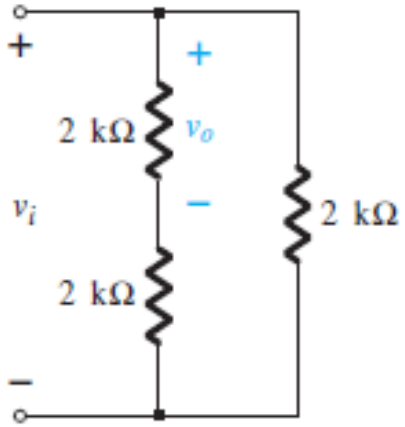


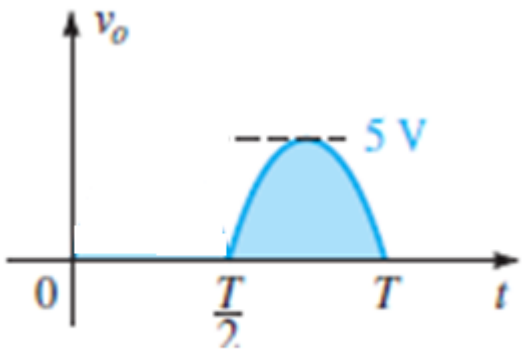


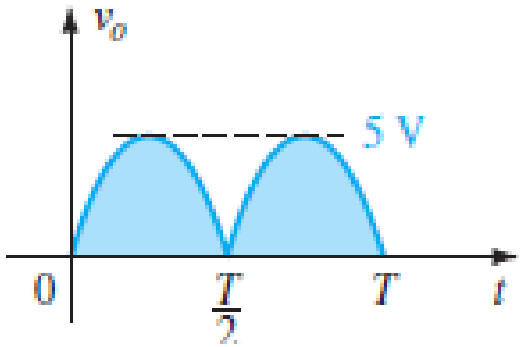


Numerical on Full Wave Rectifier: Bridge Rectifier





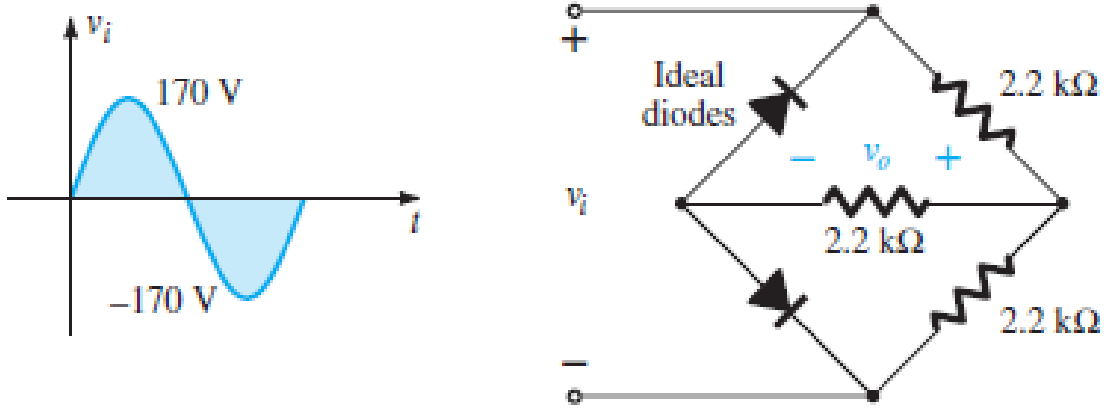




$$V_{dc} = 0.636(5\text{ V}) = 3.18\text{ V}$$

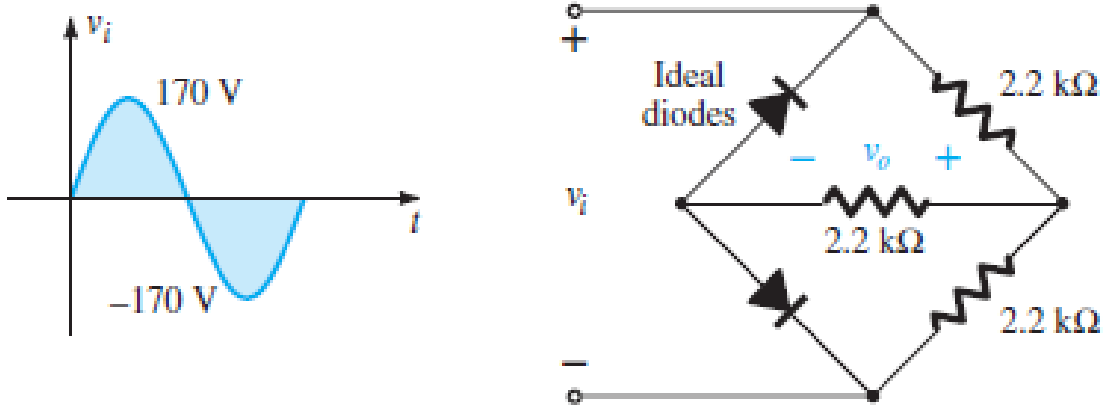
Numerical on Full Wave Rectifier: Bridge Rectifier

Sketch v_o for the network



Numerical on Full Wave Rectifier: Bridge Rectifier

Sketch v_o for the network



Positive pulse of v_i:

Top left diode "off", bottom left diode "on"

$2.2\ \text{k}\Omega \parallel 2.2\ \text{k}\Omega = 1.1\ \text{k}\Omega$

$$V_{o_{peak}} = \frac{1.1\ \text{k}\Omega(170\ \text{V})}{1.1\ \text{k}\Omega + 2.2\ \text{k}\Omega} = 56.67\ \text{V}$$

Negative pulse of v_i:

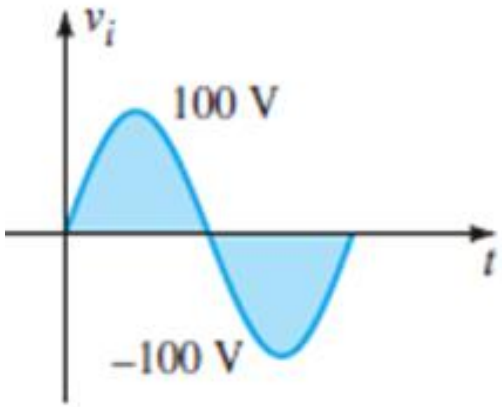
Top left diode "on", bottom left diode "off"

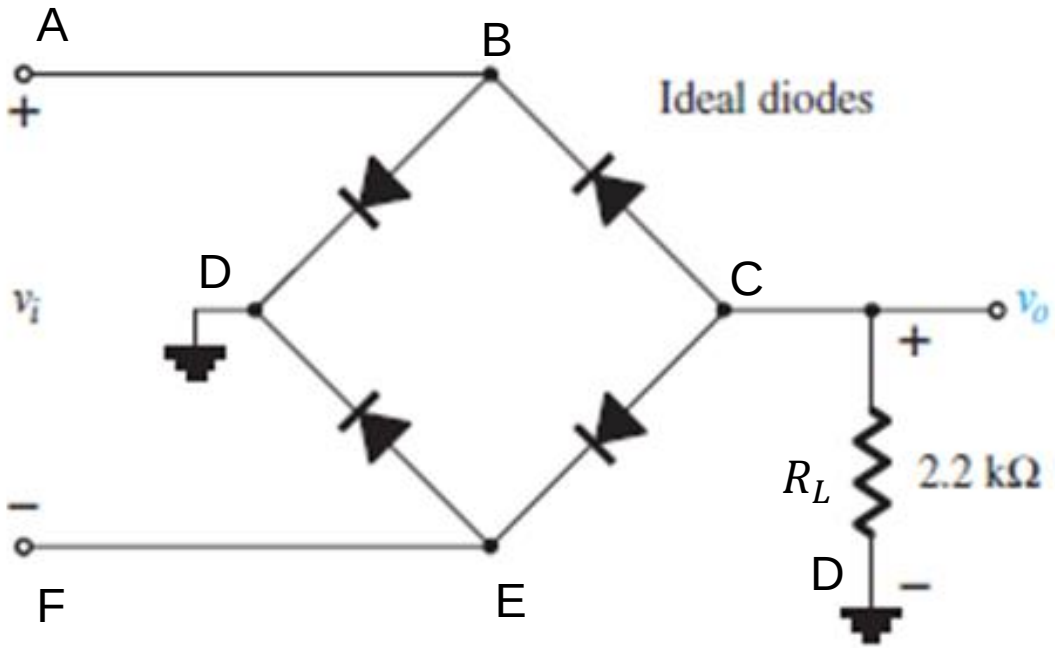
$$V_{o_{peak}} = \frac{1.1\ \text{k}\Omega(170\ \text{V})}{1.1\ \text{k}\Omega + 2.2\ \text{k}\Omega} = 56.67\ \text{V}$$

$V_{dc} = 0.636(56.67\ \text{V}) = \mathbf{36.04\ V}$

Full Wave Rectifier

3.Determine Vo and the required PIV rating of each diode for the configuration of Fig. In addition, determine the maximum current through each diode.





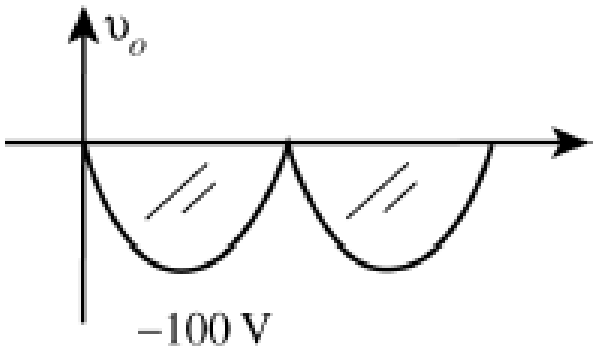
For positive cycle
Path : ABDCEF

Applying KVL

$$V_i + V_0 = 0\,;\, V_0 = -V_i$$

For Negative cycle:
Path : FEDCBA

Numerical on Full Wave Rectifier: Bridge Rectifier

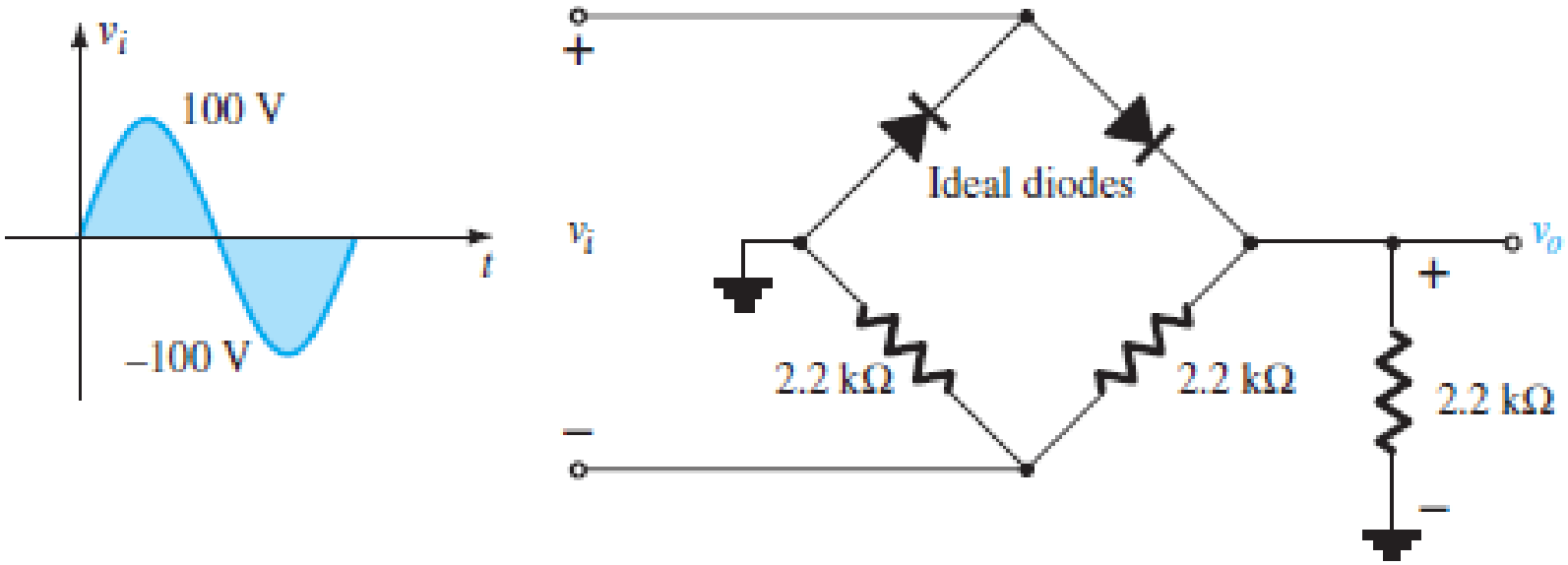


PIV = **100 V**

$$I_{max} = \frac{100\ \text{V}}{2.2\ \text{k}\Omega} = \mathbf{45.45\ mA}$$

Numerical on Full Wave Rectifier: Bridge Rectifier

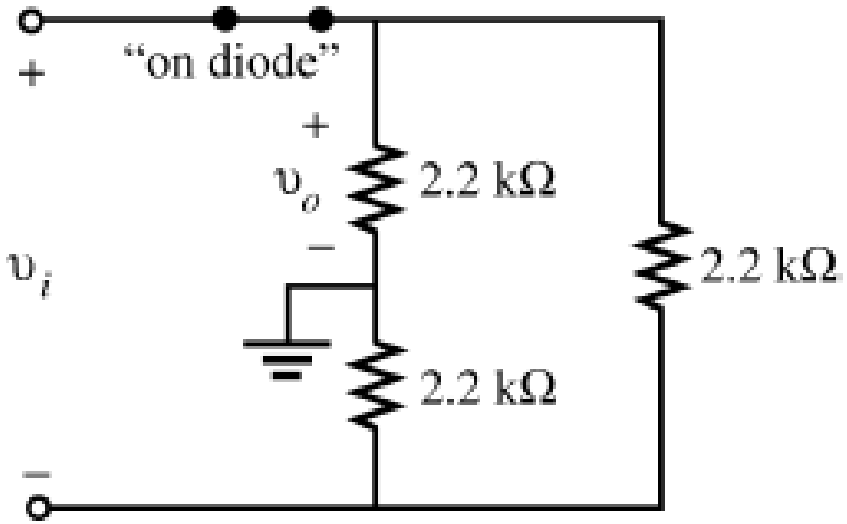
4.Sketch Vo for the network of Fig. and determine the dc voltage available.



Numerical on Full Wave Rectifier: Bridge Rectifier

Positive half-cycle of v_i:

Network redrawn:



Voltage-divider rule:

$$V_{o_{max}} = \frac{2.2\ \text{k}\Omega(V_{i_{max}})}{2.2\ \text{k}\Omega + 2.2\ \text{k}\Omega}$$

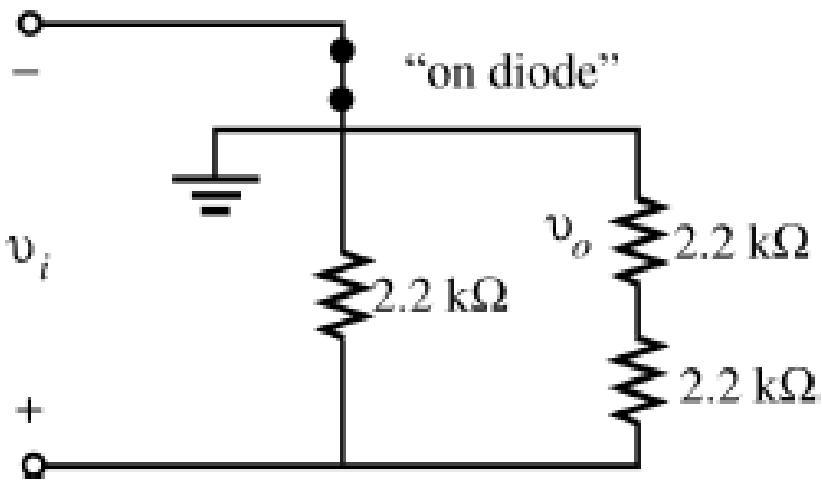
$$= \frac{1}{2}(V_{i_{max}})$$

$$= \frac{1}{2}(100\ \text{V})$$

$$= \mathbf{50\ V}$$

Numerical on Full Wave Rectifier: Bridge Rectifier

Negative half-cycle of v_i :



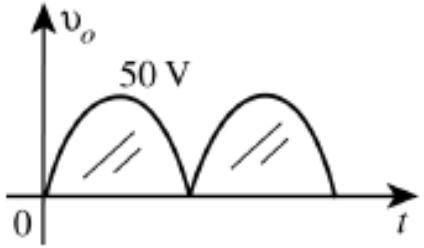
Voltage-divider rule:

$$V_{o_{max}} = \frac{2.2\ \text{k}\Omega(V_{i_{max}})}{2.2\ \text{k}\Omega + 2.2\ \text{k}\Omega}$$

$$= \frac{1}{2}(V_{i_{max}})$$

$$= \frac{1}{2}(100\ \text{V})$$

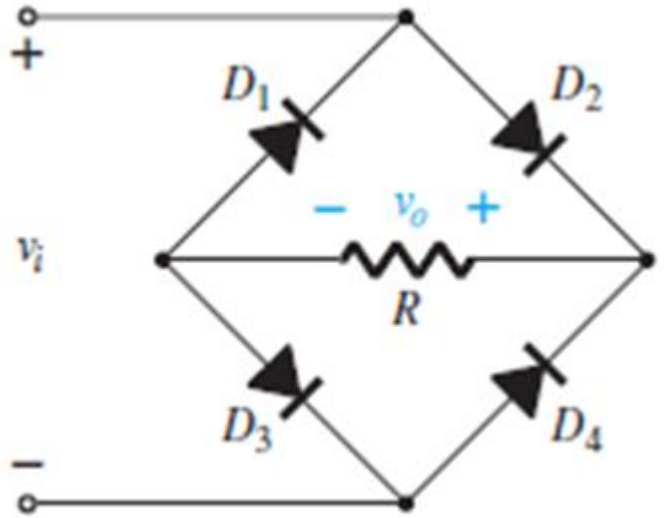
$$= \mathbf{50\ V}$$



$$V_{dc} = 0.636V_m = 0.636\ (50\ \text{V})$$
$$= \mathbf{31.8\ V}$$

Numerical on Full Wave Rectifier: Bridge Rectifier

5. A full-wave bridge rectifier with a 120-V rms sinusoidal input has a load resistor of 1 kΩ.
   (a) If silicon diodes are employed, what is the dc voltage available at the load?
   (b) Determine the required PIV rating of each diode.
   (c) Find the maximum current through each diode during conduction.
   (d) What is the required power rating of each diode?



Numerical on Full Wave Rectifier: Bridge Rectifier

5. A full-wave bridge rectifier with a 120-V rms sinusoidal input has a load resistor of 1 kΩ.
   (a) If silicon diodes are employed, what is the dc voltage available at the load?
   (b) Determine the required PIV rating of each diode.
   (c) Find the maximum current through each diode during conduction.
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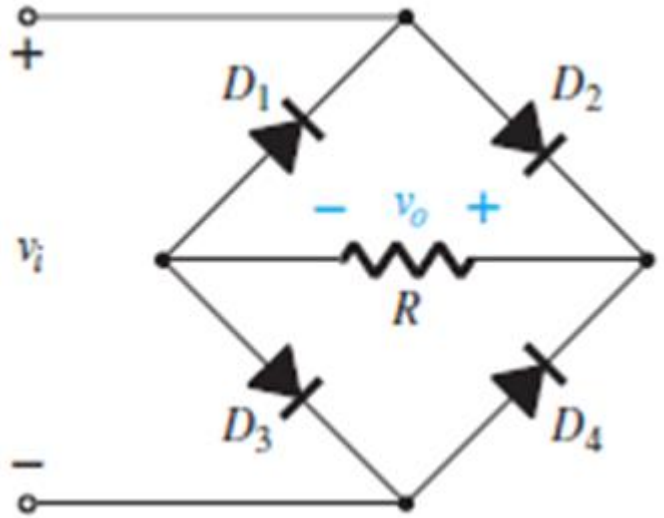


Numerical on Full Wave Rectifier: Bridge Rectifier

(a) $V_m = \sqrt{2}\,(120\text{ V}) = 169.7\text{ V}$

$$V_{L_m} = V_{i_m} - 2V_D$$

$$= 169.7\text{ V} - 2(0.7\text{ V}) = 169.7\text{ V} - 1.4\text{ V}$$

$$= 168.3\text{ V}$$

$$V_{dc} = 0.636(168.3\text{ V}) = \mathbf{107.04\text{ V}}$$

(b) PIV : $V_m - V_k = 169.7 - 0.7$ $= \mathbf{169\text{ V}}$

Numerical on Full Wave Rectifier: Bridge Rectifier

(c) $$I_D(\max) = \frac{V_{L_m}}{R_L} = \frac{168.3\ \text{V}}{1\ \text{k}\Omega} = \mathbf{168.3\ mA}$$

(d) $$\begin{aligned} P_{\max} = V_D I_D &= (0.7\ \text{V}) I_{\max} \\ &= (0.7\ \text{V})(168.3\ \text{mA}) \\ &= \mathbf{117.81\ mW} \end{aligned}$$

Numerical on Full Wave Rectifier: Bridge Rectifier

6. The input to a bridge rectifier is given through a 10 : 1 transformer from a supply of 230 Sin 314 t. If $R_L = 500\ \Omega$. Determine

DC load voltage

RMS load voltage

PIV across diodes

DC power delivered to the load

Frequency of output waveform

Numerical on Full Wave Rectifier: Bridge Rectifier

$$The\ primary\ voltage\ of\ transformer, V_1 = 230\ Sin\ 314\ t$$

$$Transformer\ turns\ ration, \frac{N_1}{N_2} = \frac{10}{1}$$

$$The\ secondary\ voltage\ of\ transformer, V_2 = \frac{N_2}{N_1}\ V_1 = \frac{1}{10}\ 230\ Sin\ 314\ t$$

$$V_2 = 23\ Sin\ 314\ t$$

$$V_2 = Vm\ Sin\ \omega t = 23\ Sin\ 314\ t$$

$$Therefore, Vm = 23\ V$$

Numerical on Full Wave Rectifier: Bridge Rectifier

$$DC\ load\ voltage, Vdc = \frac{2\,Vm}{\pi} = \frac{2 \times 23}{\pi}$$ **= 14.64 V**

$$RMS\ load\ voltage, Vrms = \frac{Vm}{\sqrt{2}} = \frac{23}{\sqrt{2}}$$ **= 16.26**

$$PIV\ across\ diodes, PIV \geq Vm \geq 23\ V$$

$$DC\ power\ delivered\ to\ the\ load, Pdc = Idc^2 \times R_L = \frac{Vdc^2}{R_L}$$ **= 0.428 W**

$$Frequency\ of\ output\ waveform, f_o = 2f_i = 100\ Hz$$

Numerical on Full Wave Rectifier: Center Tap & Bridge Rectifier

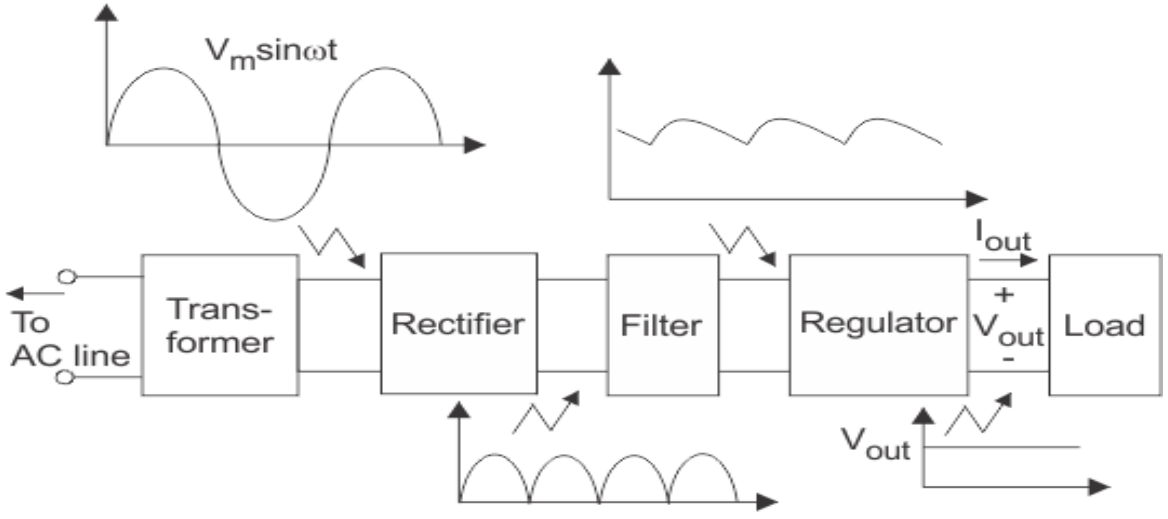
7. In a two diode FWR using Si diodes, the RMS voltage across each half of the transformer secondary is 100V. The load resistance is 975 Ω Find (i) Average current (ii) Average output voltage (iii) PIV of diode.

   Ans: V_{dc} = 89.57V, I_{dc} = 91.8mA and PIV= 282.1V.

8. A Bridge rectifier with ideal diodes has an ac source of RMS value 220 V, 50Hz connected to the primary of transformer. If the load resistance is 200Ω and turns ratio of transformer is 4:1, find the dc output volatge, dc output current and output frequency.

   Ans: V_{dc} = 49.6V, I_{dc} = 248mA and f_o = 100Hz.

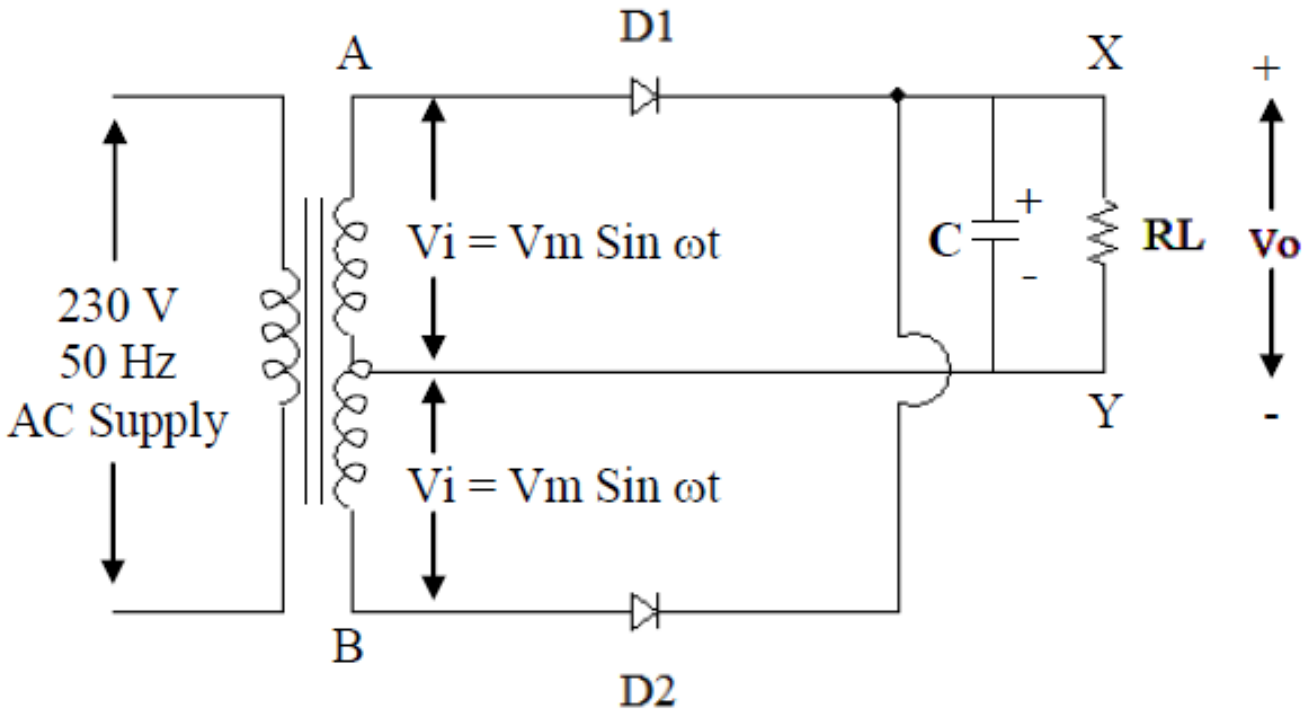
Shunt Capacitor Filter



Components of typical linear power supply

Filter is a circuit which converts pulsating DC to smooth DC. Since the reactance of capacitor and inductor depends on frequency, by connecting a capacitor in parallel with the load or by connecting an inductor in series with the load, the ac ripple present at the output of a rectifier can be reduced.

FWR with Shunt Capacitor Filter

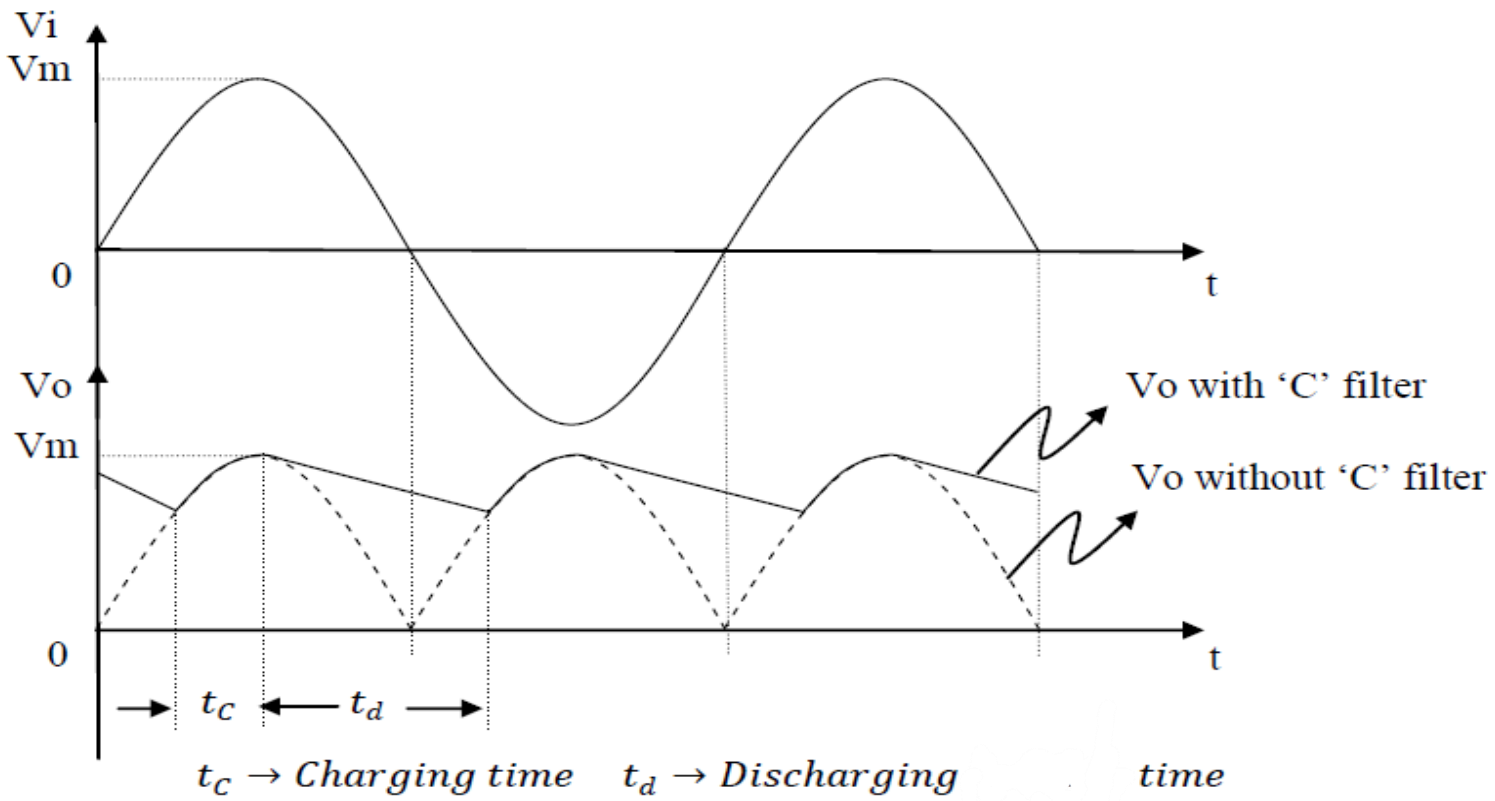


FWR with Shunt Capacitor Filter

Working

During positive half cycle the diode D1 is forward biased in centre tap full wave rectifier and diode D1 and D2 are forward biased in bridge rectifier. Hence the capacitor C will charge from 0 V towards the peak value of input Vm. When input voltage Vi reaches Vm the charge on capacitor will also be equal to Vm, hence the diodes will turn off (since both anode and cathode of diodes will be at same potential). Now the capacitor starts discharging through the load RL, if the load is very light (load resistance is very high and load current is low) the capacitor will discharge by a small amount, by that time next half cycle charges the capacitor back to Vm. Thus the output voltage remains almost constant.

Shunt Capacitor Filter



Shunt Capacitor Filter

Expression for ripple factor

$$\gamma = \frac{1}{4\sqrt{3}\, f\, C\, R_L}$$

$f \rightarrow$ *Frequency of input AC signal*

$C \rightarrow$ *Filter capacitor used*

$R_L \rightarrow$ *Load resistance*

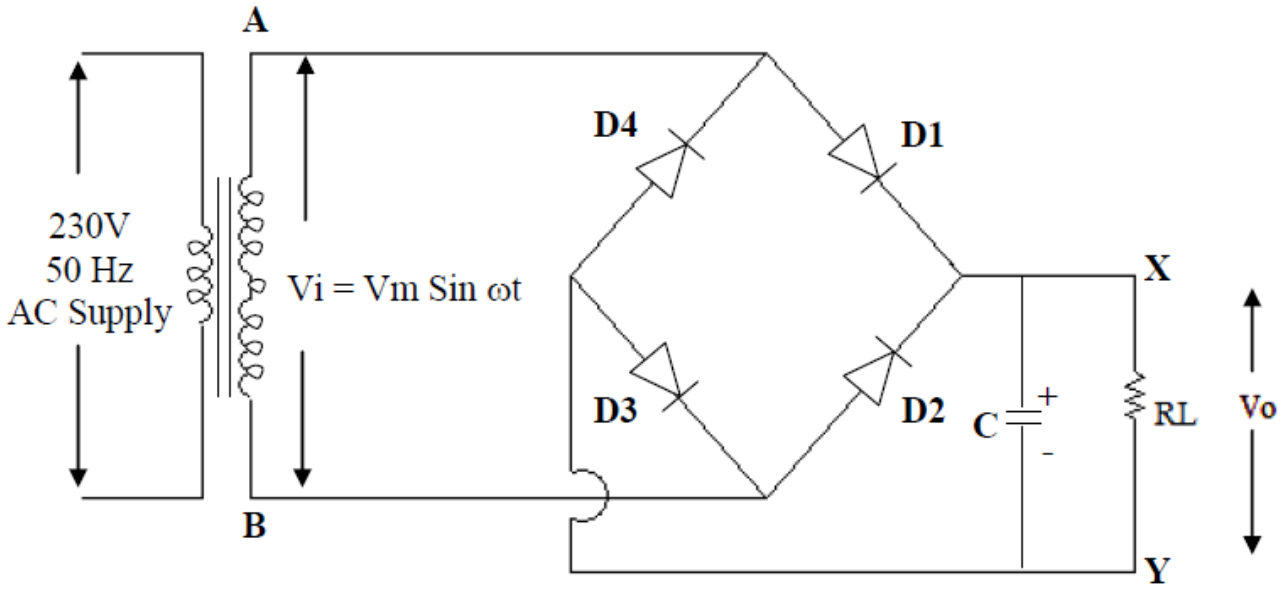
$$\gamma \propto \frac{1}{f} \quad \frac{1}{C} \quad \frac{1}{R_L}$$

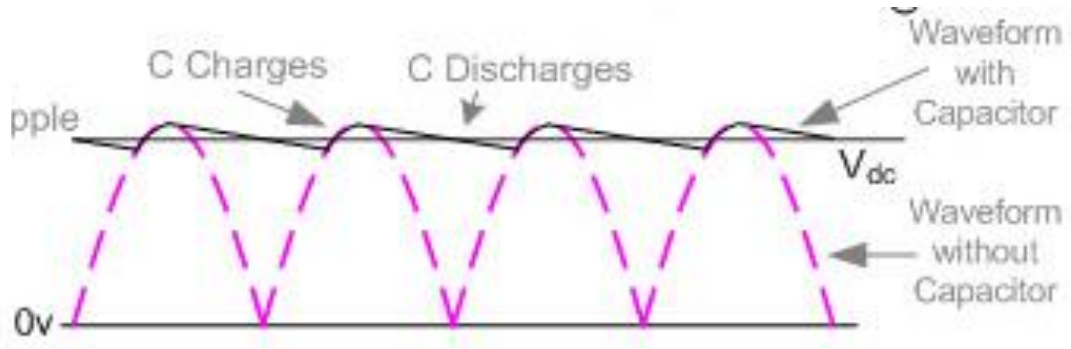
Since ripple is inversely proportional to frequency, capacitor and load resistance, the ripple can be minimized by using high value of C. (R_L and f are not in designer's hand)

$$\gamma = \frac{V_{r(rms)}}{V_{dc}}, V_{r(rms)} = \frac{I_{DC}}{4\sqrt{3}\, fc},$$

$$V_{dc} = V_m - \frac{I_{DC}}{4\, fc}$$

Shunt Capacitor Filter for Bridge Rectifier

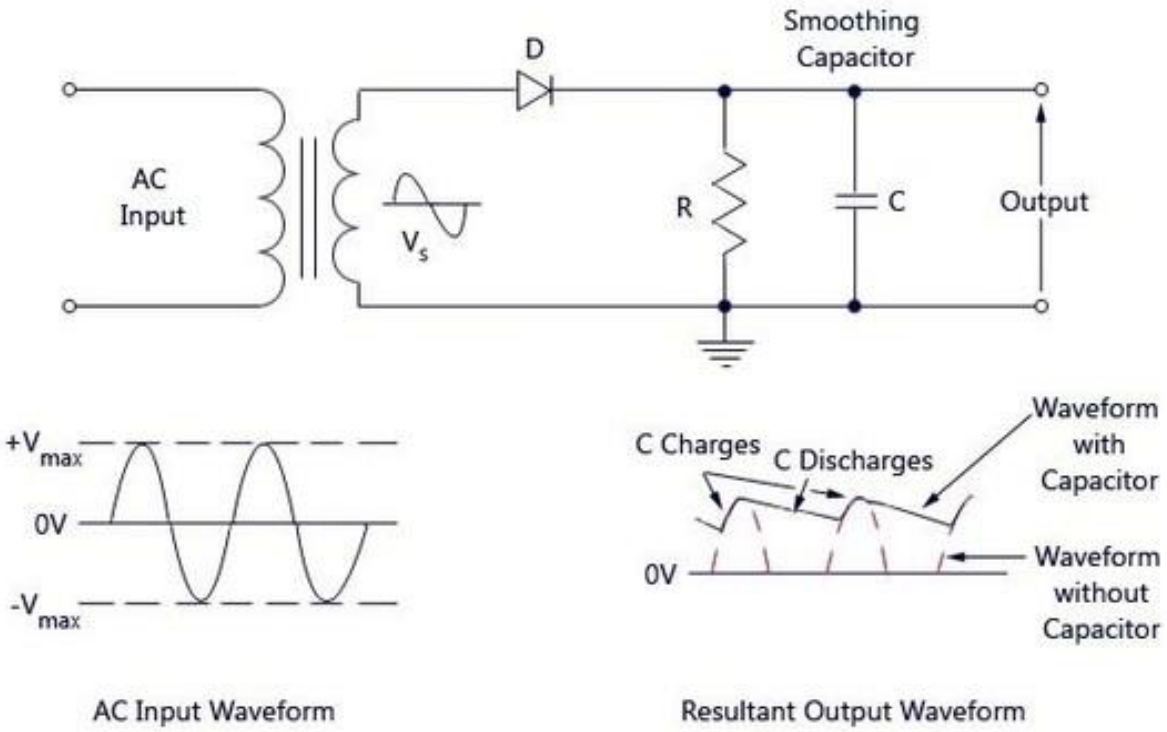


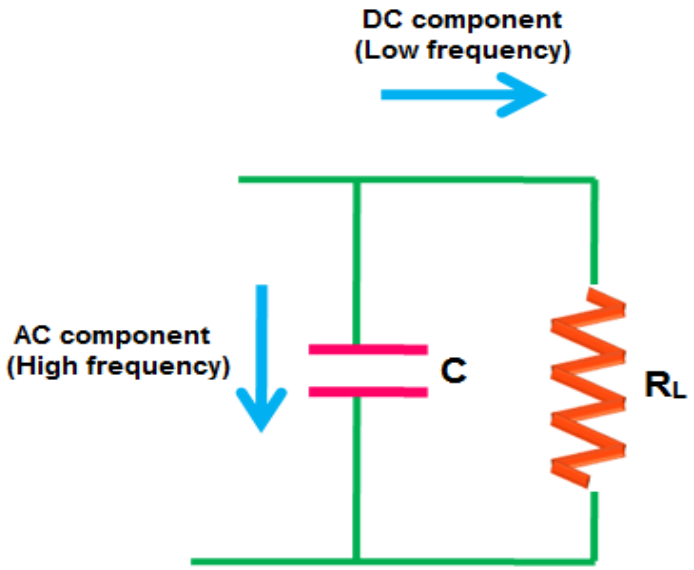


- AC components fluctuate with respect to time while the DC components remain constant with respect to time
- So the AC components present in the pulsating DC is an unwanted signal

Shunt Capacitor Filter for Half – Wave Rectifier

Capacitor C is connected in shunt/parallel with load resistor (R_L)





Shunt Capacitor Filter for Half – Wave Rectifier

Ripple Factor for Capacitor Filter of a Half Wave Rectifier is given by

Ripple Factor for a capacitor filter (HWR) = 1/ (2√3 f C R_L)

f – Frequency of AC input Signal
R_L – Value of Load resistor
C – Capacitance of the Shunt Capacitor

$$\gamma = \frac{V_{r(rms)}}{V_{dc}}, V_{r(rms)} = \frac{I_{DC}}{2\sqrt{3}fc},$$

$$V_{dc} = V_m - \frac{I_{DC}}{2\ fc}$$

Numerical on Shunt Capacitor Filter

1. A full wave rectifier with C filter is supplying a load of 500 Ω. If the ripple factor should not exceed 10 %, find the value of capacitor required. Assume input AC signal frequency is 50 Hz. What is the new value of ripple if capacitor of 500 μF is connected across the load?

Solution:

$Given\ \gamma = 10\ \% = 0.1\ and\ R_L = 500\Omega$

$$\gamma = \frac{1}{4\sqrt{3}\, f\, C\, R_L}$$

$$C = \frac{1}{4\sqrt{3}\, f\, \gamma R_L} = \frac{1}{4\sqrt{3}\ \times 50 \times\ 0.1\ \times 500} = 57.73\ \mu F$$

$If\ a\ capacitor\ of\ 500\ \mu F\ is\ used\ the\ ripple\ factor\ is$

$$\gamma = \frac{1}{4\sqrt{3}\, f\, C\, R_L} = \frac{1}{4\sqrt{3} \times 50 \times 500 \times 10^{-6} \times 500} = 0.0115$$

Numerical on Shunt Capacitor Filter

2. In a full wave rectifier with C filter the output DC voltage is 10 V and load current is 10 mA. Calculate the value of capacitance required such that the output DC voltage will have ripple ≤ 0.001.

Solution:

$$R_L = \frac{Vdc}{Idc} = \frac{10}{10\ m} = 1\ K\Omega$$

$$Assume\ frequency\ of\ input\ AC\ signal, f = 50\ Hz$$

$$\gamma = \frac{1}{4\sqrt{3}\, f\, C\, R_L}$$

$$C = \frac{1}{4\sqrt{3}\, f\, \gamma R_L} = \frac{1}{4\sqrt{3} \times 50 \times 0.001 \times 1 \times 10^3} = 2886\ \mu F$$

Numerical on Shunt Capacitor Filter

3. Calculate the RMS value of the ripple voltage for the FWR in a 100µF Capacitor connected to a load drawing 50mA of current .What is the dc voltage at the output if the peak rectified output voltage is 30V and frequency is 50Hz. Also find the ripple factor

Solution:

$$\gamma = \frac{V_{r(rms)}}{V_{dc}}, V_{r(rms)} = \frac{I_{DC}}{4\sqrt{3}fc},$$

$$V_{dc} = V_m - \frac{I_{DC}}{4fc}$$

Given :
Idc= 50mA, f=50Hz, C=100µF

Therefore Vrms=1.4V

Vm= 30V
Therefore Vdc=27.5 V

Ripple factor=0.05

Numerical on Shunt Capacitor Filter

4. A Half wave rectifier with C filter is supplying a resistive load of 500Ω. If the load ripple content should not exceed 10% find the value of C required

Solution:

For a Half wave rectifier with C filter ,

Ripple Factor=$1/2\sqrt{3}\ f\ C\ R_L$

$0.10=1/\{2\sqrt{3}*50*C*500\}$

C=0.115mF

Numerical on Shunt Capacitor Filter

5. A 100µF capacitor when used as a filter has 15V rms across it with a load resistor of 2.5KΩ. If the filter is the full wave and supply frequency is 50Hz, what is the percentage of ripple factor in the output?

Solution:

For a full wave rectifier with C filter ,

Ripple factor, $\Upsilon = 1/4\sqrt{3}\, f\, C\, R_L$

$= 1/4\sqrt{3} * 50 * 100 * 10^{-6} * 2.5 * 10^{-3}$

$= 0.01154.$

So, ripple factor is 1.154%

Numerical on Shunt Capacitor Filter

6. A full wave rectifier uses a capacitor filter with 500µF capacitor and provides a load current of 200mA at 8% ripple. Calculate the dc voltage and the value of peak rectified voltage?

Solution:

The ripple factor for Full Wave Rectifier with C filter

$\Upsilon = 1/ 4\sqrt{3}\ f\ C\ RL$ substituting $RL = Vdc/Idc$

$\Upsilon = Idc/ 4\sqrt{3}\ f\ C\ Vdc$

after re-arranging

$V_{DC} = 200*10^{-3}/ 4\sqrt{3}\ *50*500*10^{-6}\ *0.08$

$V_{DC} = 14.43V$

We know, $V_m = V_{dc} + I_{dc}/4fC$

$= 14.43 + \{200*\ 10^{-3} / \{\ 4*50*500*10^{-6}\ \}$

$= 14.43 + 2 = 16.43V$

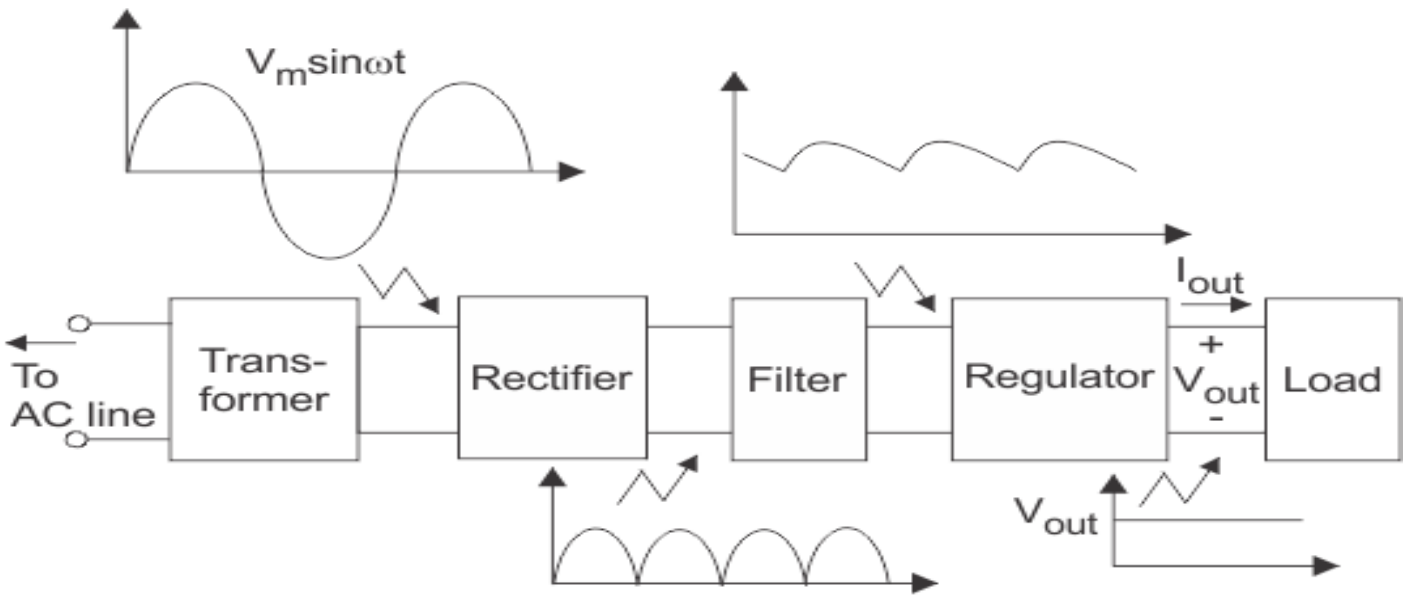
$V_m = 16.43V$

THANK YOU

Department of Electronics and Communication

ELECTRONIC PRINCIPLES AND DEVICES

Department of Electronics and Communication.



Components of typical linear power supply

A regulator is a combination of elements designed to ensure that the output voltage of a supply remains fairly constant.

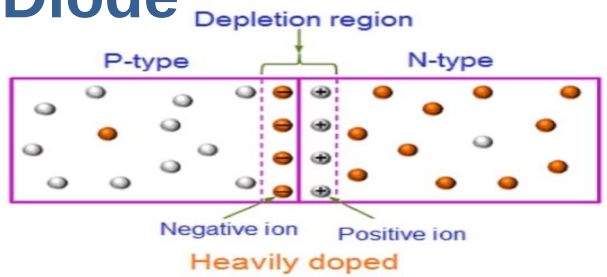
- Heavily Doped PN-Junction Device Specially Designed to operate under breakdown region

- Zener Diode under forward Bias condition works like a normal semiconductor diode

- Zener Diode under reverse bias condition acts like Voltage regulator

- Zener diodes are usually heavily doped diodes hence the depletion layer is very narrow. When the reverse voltage across the junction is increased the electric field across the depletion layer becomes high so that electrons are pulled out of covalent bonds resulting in a sudden rise in current which is known as zener breakdown.

Structure of Zener Diode



Symbol of Zener Diode

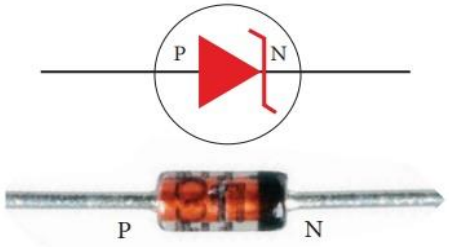


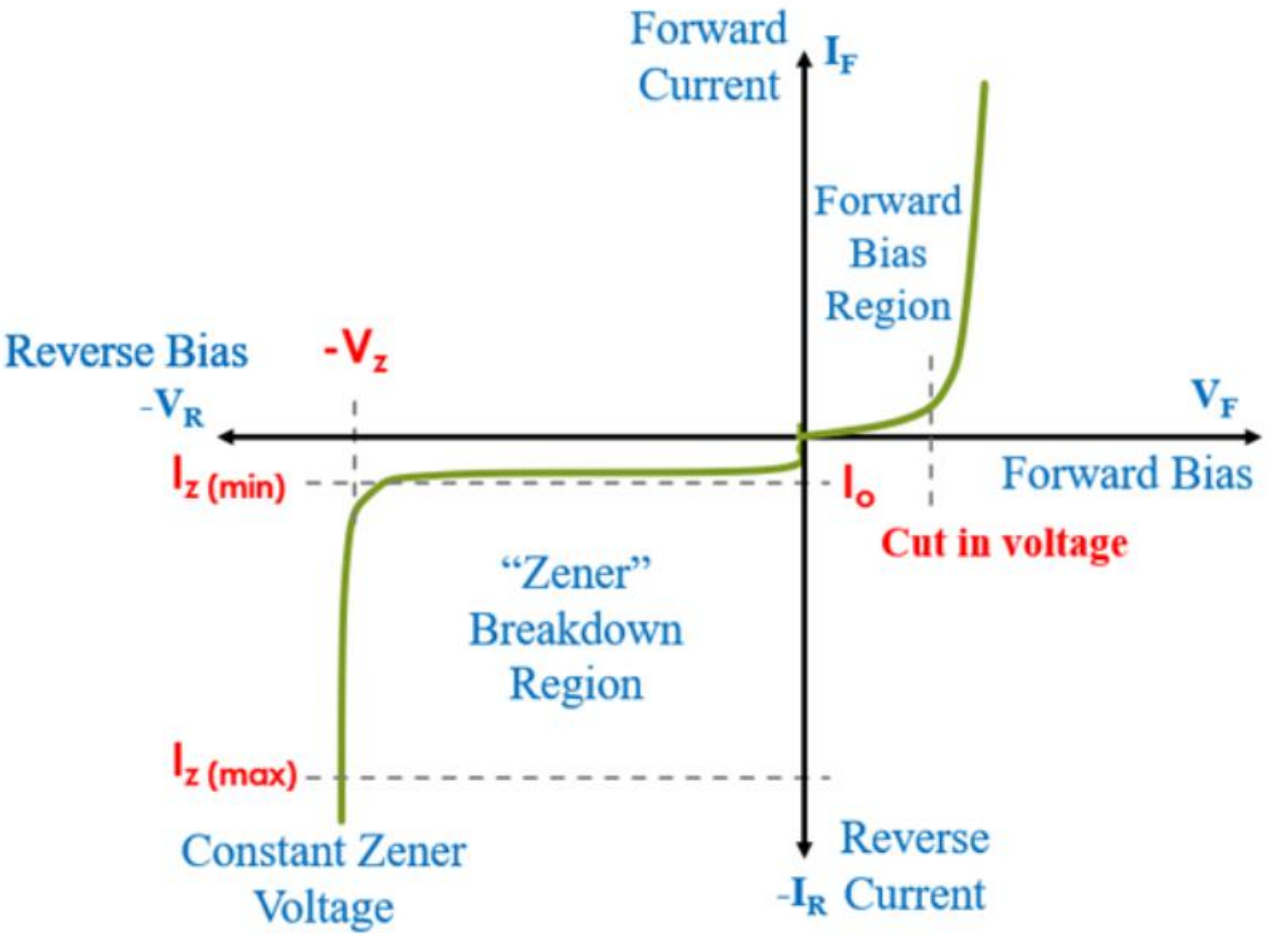
Figure (a) Zener diode and its symbol (The black colour ring denotes the negative terminal of the Zener diode)

V-I Characteristics of Zener Diode

V-I Characteristics of Zener Diode in Forward Bias Condition

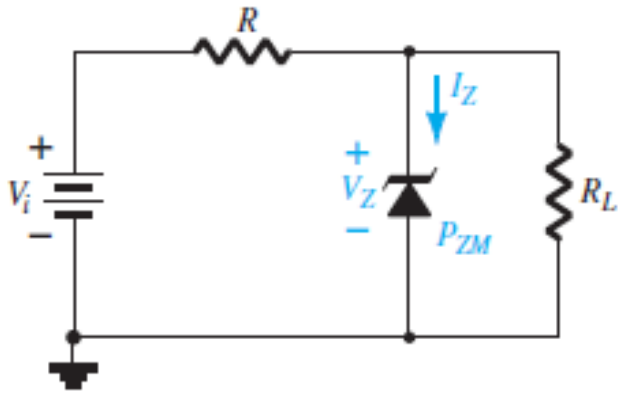
V-I Characteristics of Zener Diode in Reverse Bias Condition

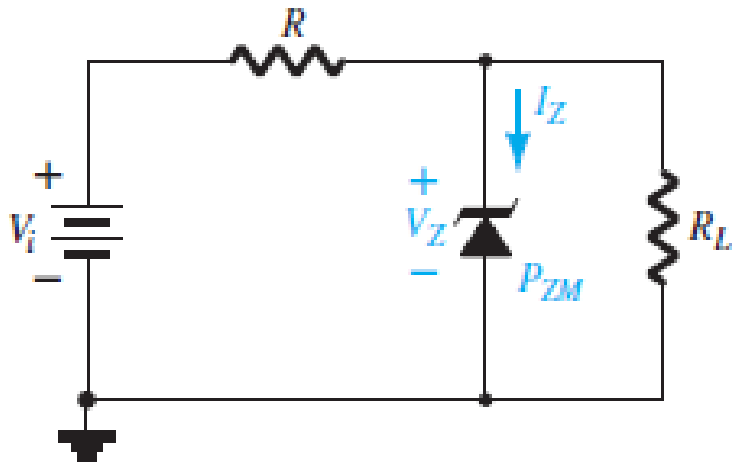
V-I Characteristics



Conditions required to operate Zener Diode as Voltage Regulator

- Zener Diode should be in Reverse Biased Condition
- Vin should be Greater than Vz
- Iz should be greater than Izmin
- Iz should be less than or equal to Izmax





Different operating conditions of Zener Regulator .

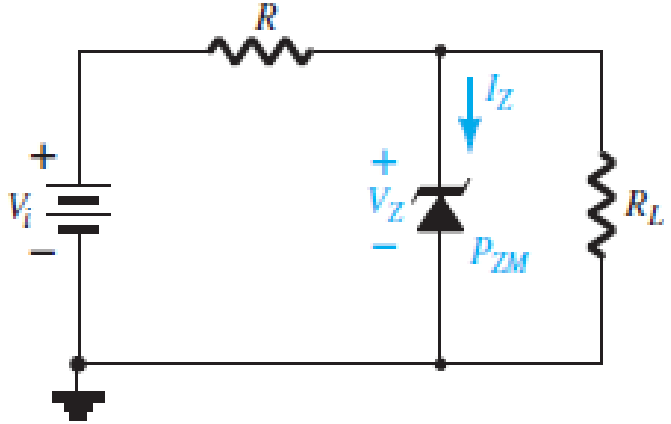
(i) Fixed quantities, (Vi and R are fixed)

(ii) Fixed supply voltage and a variable load,(Fixed Vi and variable RL)

(iii) Fixed load and a variable supply.(Fixed RL and Variable Vi)

(iv) Variable Supply and Variable Load. (Variable Vi and Variable RL)

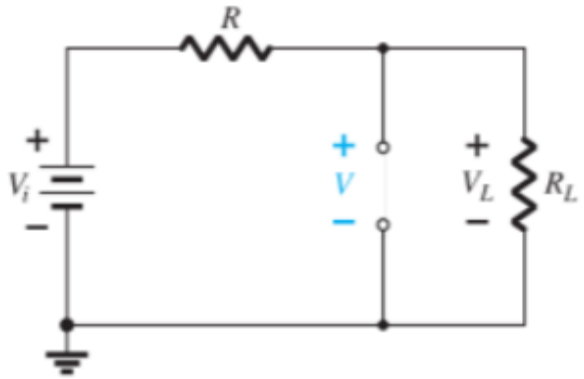
CASE-1: Fixed Vi and fixed R_L Voltage Regulator



The analysis can fundamentally be broken down into two steps.

1. Determine the state of the Zener diode by removing it from the network and calculating the voltage across the resulting open circuit

$$V = V_L = \frac{R_L V_i}{R + R_L}$$



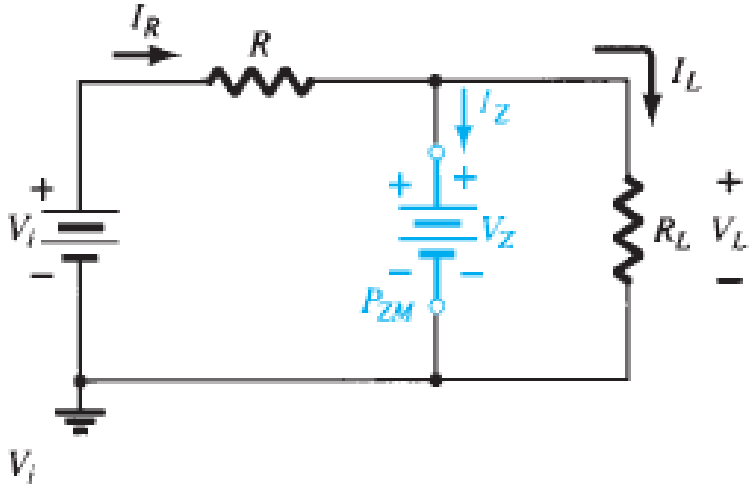
If $V \geq V_Z$, the Zener diode is on, and the appropriate equivalent model can be substituted.
If $V < V_Z$, the diode is off, and the open-circuit equivalence is substituted.

CASE-1: Fixed Vi and fixed R_L Voltage Regulator

Conclusion:

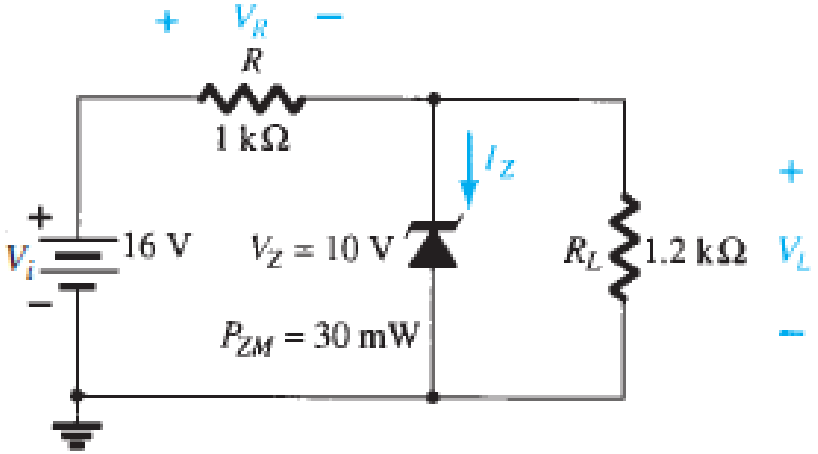
If the Zener diode is in the “on” state, the voltage across the diode is not *V volts.*

The Zener diode will turn on as soon as the voltage across the Zener diode is VZ volts.
It will then “lock in” at this level and never reach the higher level of V volts.



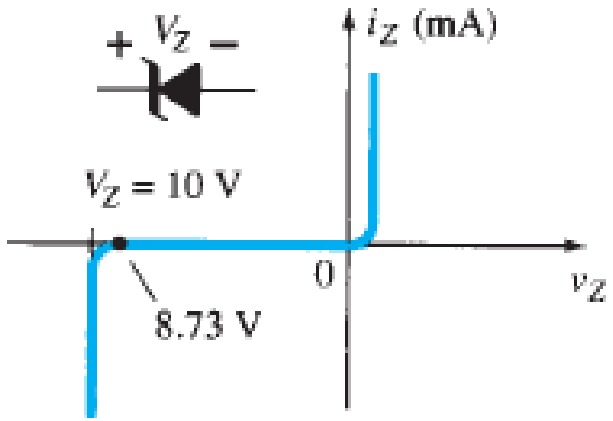
CASE-1: Fixed Vi and fixed R_L Voltage Regulator

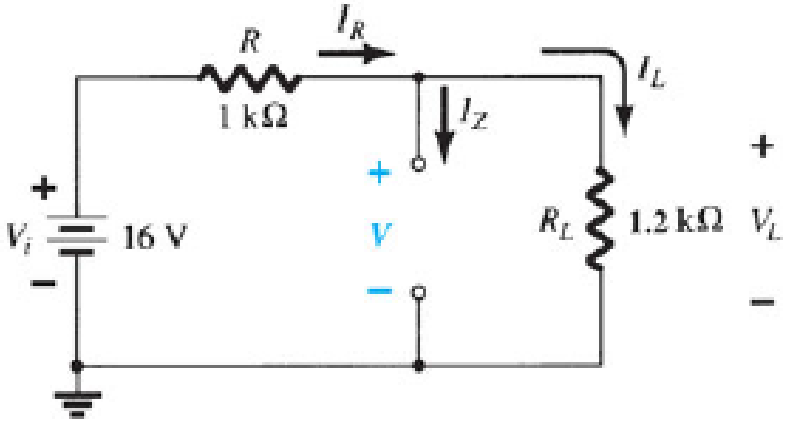
1. **For the Zener diode network of Fig,**
(i) Determine V_L , V_R , I_Z , and P_Z .
(ii) Repeat part (a) with R_L = 3KΩ.



Solution (i):

$$V = \frac{R_L V_i}{R + R_L} = \frac{1.2\ \text{k}\Omega(16\ \text{V})}{1\ \text{k}\Omega + 1.2\ \text{k}\Omega} = 8.73\ \text{V}$$

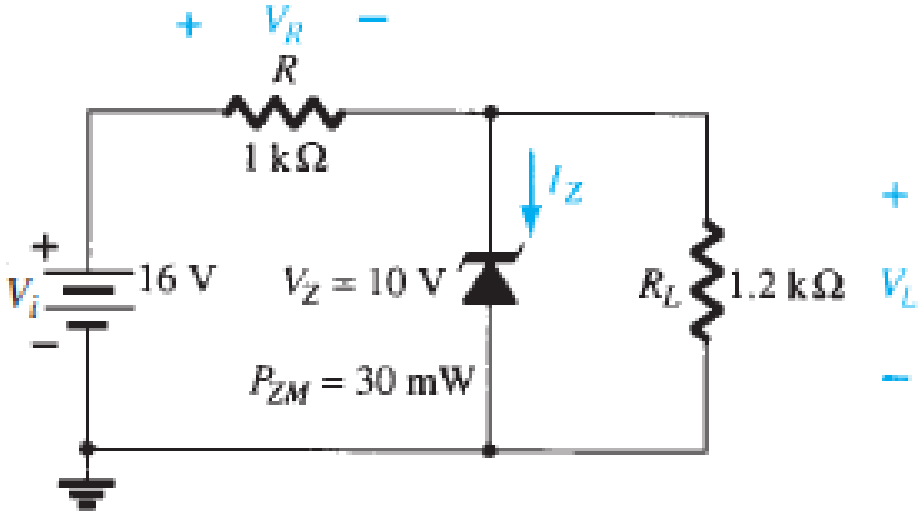




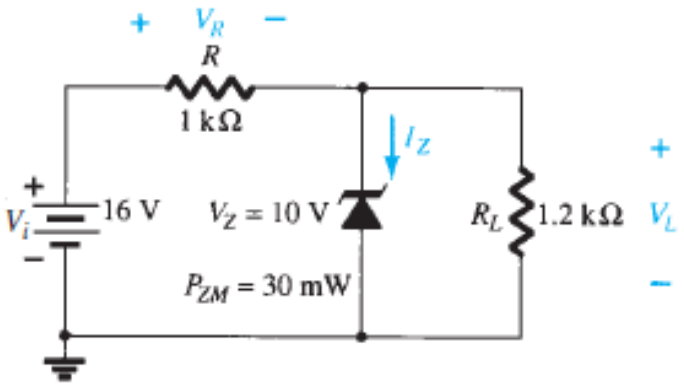
CASE-1: Fixed Vi and fixed R_L Voltage Regulator

Solution (i):

$$V_L = V = 8.73\ \text{V}$$
$$V_R = V_i - V_L = 16\ \text{V} - 8.73\ \text{V} = 7.27\ \text{V}$$
$$I_Z = 0\ \text{A}$$
$$P_Z = V_Z I_Z = V_Z(0\ \text{A}) = 0\ \text{W}$$

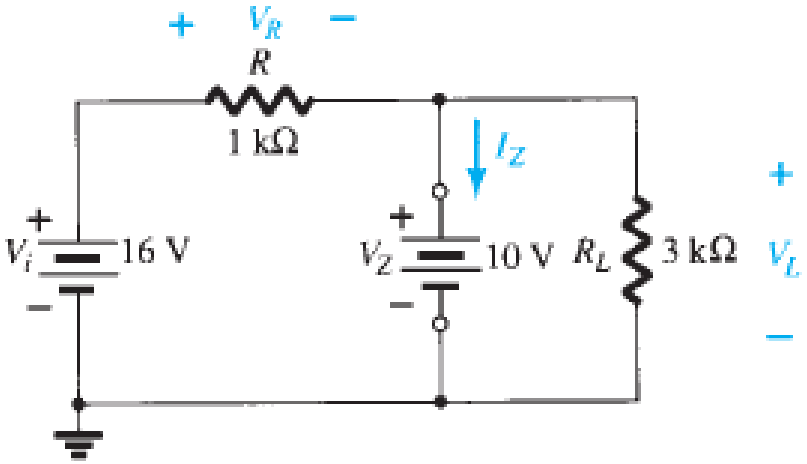


CASE-1: Fixed Vi and fixed R_L Voltage Regulator



Solution: (ii)

$$V = \frac{R_L V_i}{R + R_L} = \frac{3\text{ k}\Omega(16\text{ V})}{1\text{ k}\Omega + 3\text{ k}\Omega} = 12\text{ V}$$



$$V_L = V_Z = \mathbf{10\text{ V}}$$

$$V_R = V_i - V_L = 16\text{ V} - 10\text{ V} = \mathbf{6\text{ V}}$$

$$I_L = \frac{V_L}{R_L} = \frac{10\text{ V}}{3\text{ k}\Omega} = 3.33\text{ mA}$$

$$I_R = \frac{V_R}{R} = \frac{6\text{ V}}{1\text{ k}\Omega} = 6\text{ mA}$$

$$I_Z = I_R - I_L\ [\text{Eq. (2.18)}]$$
$$= 6\text{ mA} - 3.33\text{ mA}$$
$$= \mathbf{2.67\text{ mA}}$$

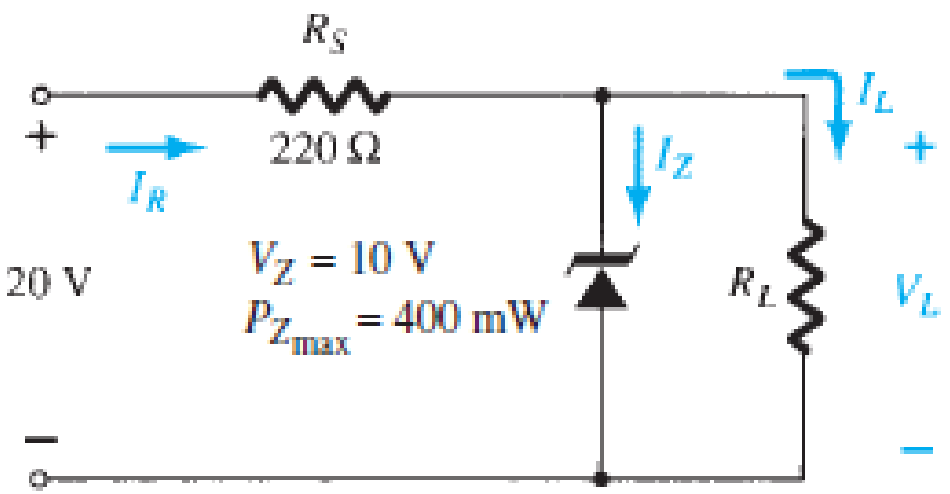
The power dissipated is

$$P_Z = V_Z I_Z = (10\text{ V})(2.67\text{ mA}) = \mathbf{26.7\text{ mW}}$$

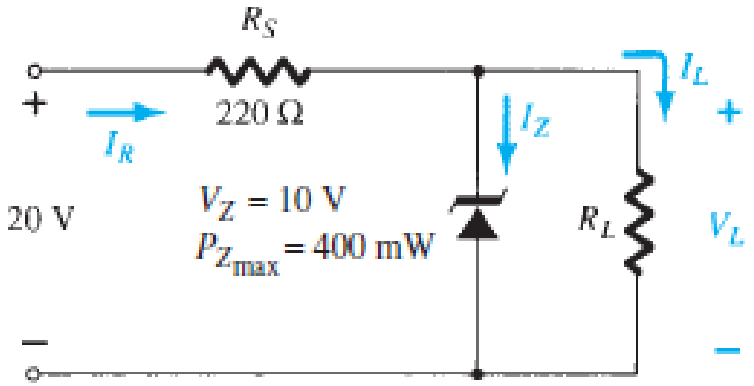
which is less than the specified $P_{ZM} = 30$ mW.

CASE-1: Fixed Vi and fixed R_L Voltage Regulator

2. (a) Determine V_L , I_L , I_Z , and I_R for the network of Fig. if R_L =180 ohm .
(b) Repeat part (a) if R_L = 470 ohm .



CASE-1: Fixed Vi and fixed R_L Voltage Regulator



Solution a:

In the absence of the Zener diode

$$V_L = \frac{180\,\Omega(20\text{ V})}{180\,\Omega + 220\,\Omega} = 9\text{ V}$$

$V_L = 9\text{ V} < V_Z = 10\text{ V}$ and diode non-conducting

Therefore, $I_L = I_R = \dfrac{20\text{ V}}{220\,\Omega + 180\,\Omega} = \mathbf{50\ mA}$

with $I_Z = \mathbf{0\ mA}$
and $V_L = \mathbf{9\ V}$

Solution b:

In the absence of the Zener diode

$$V_L = \frac{470\,\Omega(20\text{ V})}{470\,\Omega + 220\,\Omega} = 13.62\text{ V}$$

$V_L = 13.62\text{ V} > V_Z = 10\text{ V}$ and Zener diode "on"

Therefore, $V_L = \mathbf{10\ V}$ and $V_{R_s} = 10\text{ V}$

$I_{R_s} = V_{R_s} / R_s = 10\text{ V}/220\,\Omega = \mathbf{45.45\ mA}$

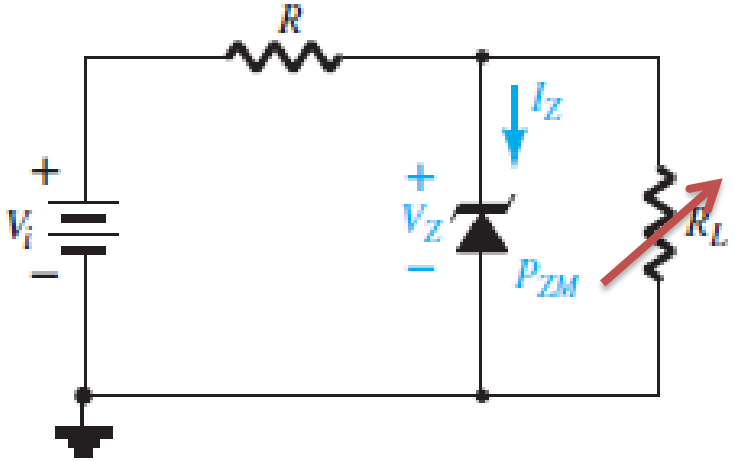
$I_L = V_L/R_L = 10\text{ V}/470\,\Omega = \mathbf{21.28\ mA}$

and $I_Z = I_{R_s} - I_L = 45.45\text{ mA} - 21.28\text{ mA} = \mathbf{24.17\ mA}$

CASE-2: Fixed supply voltage and a variable load

Conditions for R_L to Keep the Zener currnet I_Z in the operating limit
i.e $I_{Zmin} \leq I_Z < I_{Zmax}$

 # 1: Condition for R_{Lmin} :



$$I_L = I_R - I_Z$$

$$R_L = \frac{V_Z}{I_L}$$ *R_L is Minimum when I_L is Maximum*

$$I_{Lmax} = I_R - I_{Zmin}$$ where $I_R = \frac{V_i - V_z}{R}$

$$R_{Lmin} = \frac{V_Z}{I_{Lmax}}$$

If I_{Zmin} = 0 then I_{Lmax} = I_R

hence, $R_{Lmin} = \frac{V_Z}{I_R} = \frac{V_Z R}{V_i - V_Z}$

CASE-2: Fixed supply voltage and a variable load

Conditions for R_L to Keep the Zener currnet I_Z in the operating limit i.e

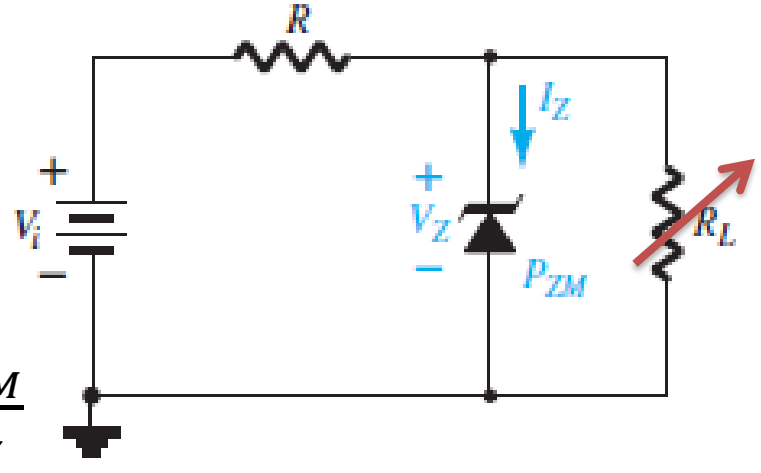
$$I_{Zmin} \leq I_Z < I_{Zmax}$$

 # 2: Condition for R_{Lmax} :

$$I_L = I_R - I_Z$$

$$R_L = \frac{V_Z}{I_L}$$

R_L is Maximum when I_L is Minimum



$$I_{Lmin} = I_R - I_{Zmax} \quad \text{where} \quad I_R = \frac{V_i - V_z}{R} \text{ and } I_{Zmax} = \frac{P_{ZM}}{V_Z}$$

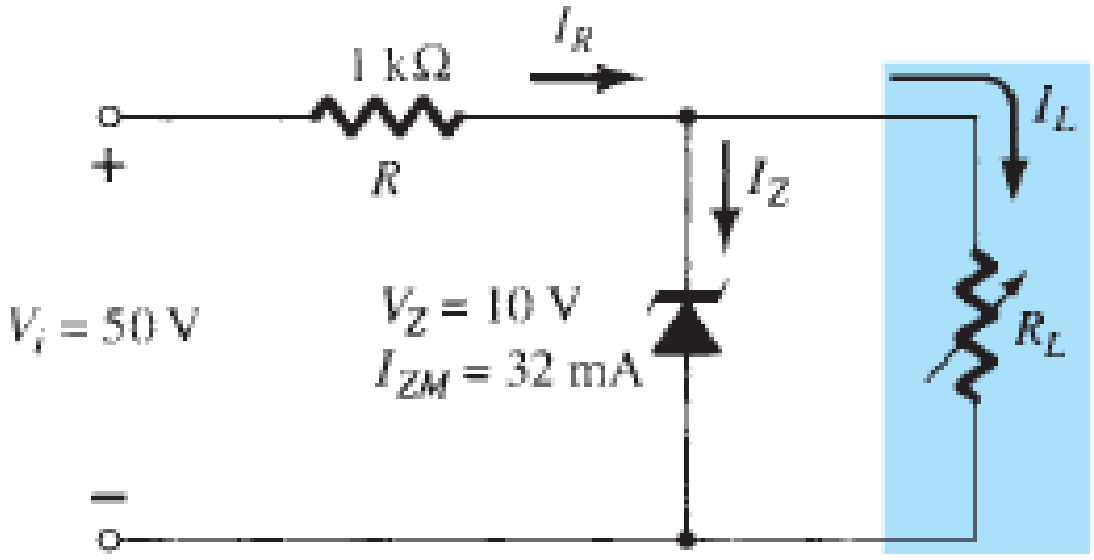
$$R_{Lmax} = \frac{V_Z}{I_{Lmin}}$$

CASE-2: Fixed supply voltage and a variable load

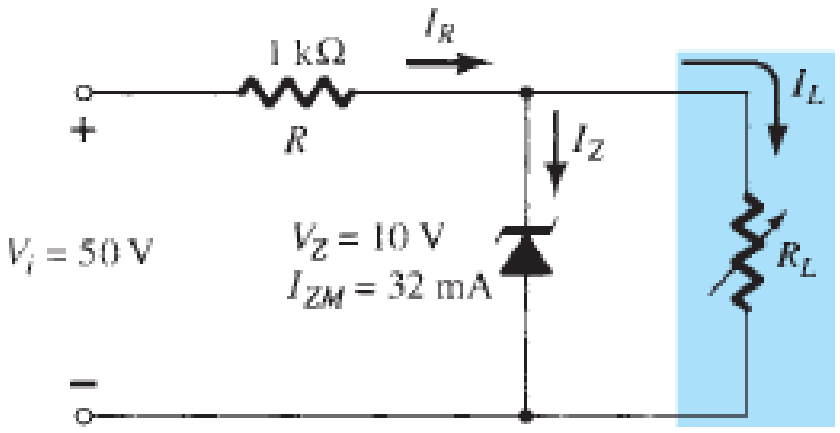
3. For the network of Fig

(i) Determine the range of *R_L and I_L that will result in V_{RL}* being maintained at 10 V. Given I_{Zmin} = 1mA.

(ii) Determine the maximum wattage rating of the diode.



CASE-2: Fixed supply voltage and a variable load



(i) $$I_R = \frac{V_i - V_Z}{R} = \frac{50-10}{1k\Omega} = 40mA$$

$$I_{Lmax} = I_R - I_{Zmin} = 40mA - 1mA = 39mA$$

$$I_{Lmin} = I_R - I_{Zmax} = 40mA - 32mA = 8mA$$

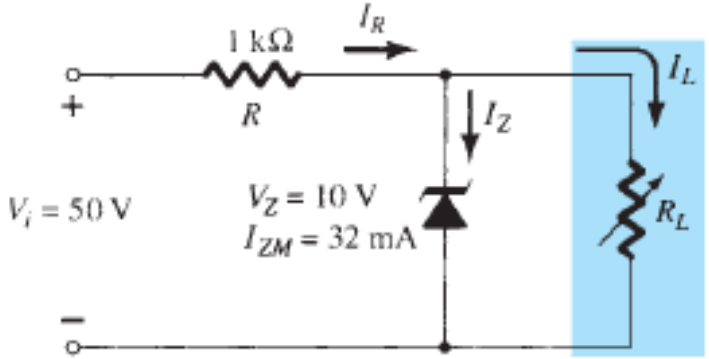
$$R_{Lmax} = \frac{V_Z}{I_{Lmin}} = \frac{10}{8mA} = 1.25K\Omega$$

$$R_{Lmin} = \frac{V_Z}{I_{Lmax}} = \frac{10}{39mA} = 256.41\ \Omega$$

CASE-2: Fixed supply voltage and a variable load

3. For the network of Fig
(ii) Determine the maximum wattage rating of the diode.

(ii) Maximum Watage $P_{Zmax} = Vz * I_{zmax} = 320mW$



CASE-2: Fixed supply voltage and a variable load

4. Determine the value of R_L that will establish maximum power conditions for the Zener diode. Determine the minimum value of R_L to ensure that the Zener diode is in the "on" state.

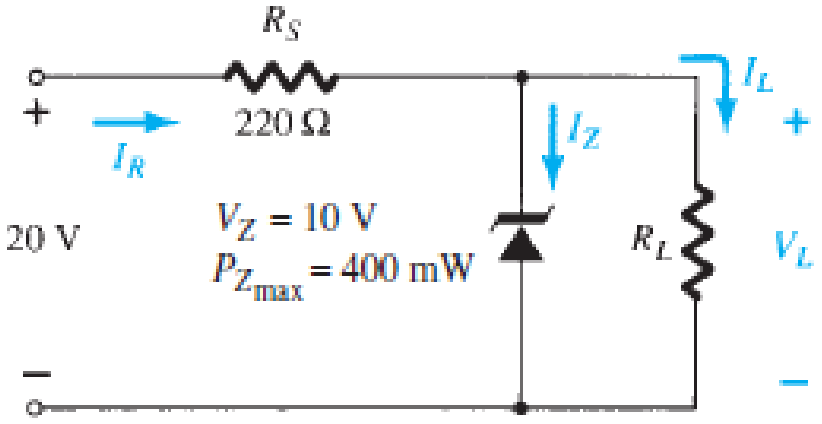
$$P_{Z_{max}} = 400 \text{ mW} = V_Z I_Z = (10 \text{ V})(I_Z)$$

$$I_Z = \frac{400 \text{ mW}}{10 \text{ V}} = 40 \text{ mA}$$

$$I_{L_{min}} = I_{R_s} - I_{Z_{max}} = 45.45 \text{ mA} - 40 \text{ mA} = 5.45 \text{ mA}$$

$$R_L = \frac{V_L}{I_{L_{min}}} = \frac{10 \text{ V}}{5.45 \text{ mA}} = \mathbf{1{,}834.86\ \Omega}$$

Large R_L reduces I_L and forces more of I_{R_s} to pass through Zener diode.



In the absence of the Zener diode

$$V_L = 10 \text{ V} = \frac{R_L(20 \text{ V})}{R_L + 220\ \Omega}$$

$$10R_L + 2200 = 20R_L$$

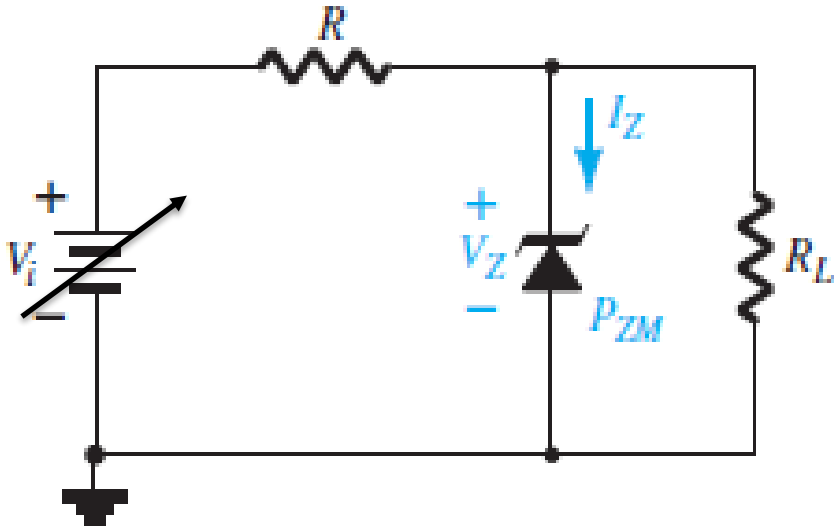
$$10R_L = 2200$$

$$R_L = \mathbf{220\ \Omega}$$

CASE-3: Fixed R_L , Variable Vi

Conditions for Vi to Keep the Zener current I_Z in the operating limit i.e $I_{Zmin} \leq I_Z < I_{Zmax}$

 # 1: Condition for Vi_{min} :



$$I_R = I_Z + I_L$$

$$I_{Rmin} = I_{Zmin} + I_L$$

$$I_{Rmin} = \frac{V_{imin} - V_z}{R}$$

$$V_{imin} = V_Z + I_{Rmin}R$$

If $I_{Zmin} = 0$; $then\ I_{Rmin} = I_L$; $V_{imin} = V_Z + I_L R = \frac{V_Z(R_L+R)}{R_L}$

CASE-3: Fixed R_L , Variable Vi

Conditions for Vi to Keep the Zener currnet I_Z in the operating limit i.e $I_{Zmin} \leq I_Z < I_{Zmax}$

 # 2: Condition for Vi_{max} :

$$I_R = I_Z + I_L$$

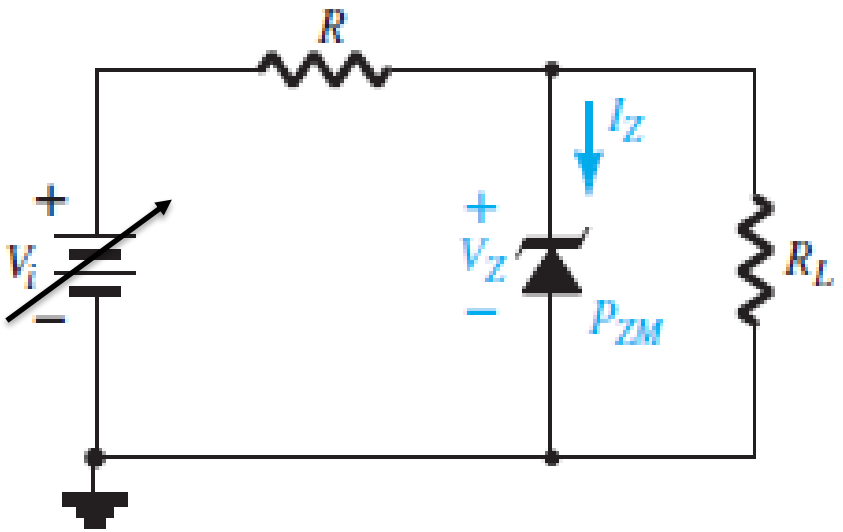
$$I_{Rmax} = I_{Zmax} + I_L$$

$$I_L = \frac{V_Z}{R_L}$$

$$I_{Rmax} = \frac{V_{imax} - V_Z}{R}$$

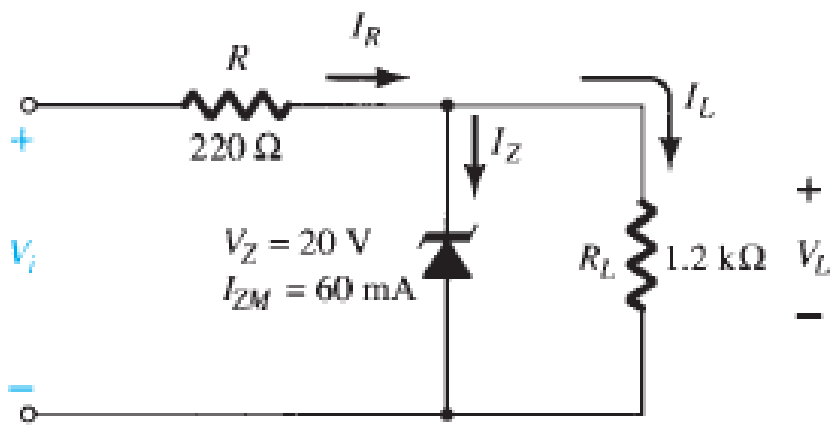
$$I_{Zmax} = \frac{P_{ZM}}{V_Z}$$

$$V_{imax} = V_Z + I_{Rmax}R$$



CASE-3: Fixed R_L , Variable Vi

5. Determine the range of values of *Vi that will maintain the Zener diode of* Fig. in the "on" state. Given I_{Zmin} = 2mA



$$V_{imin} = V_Z + I_{Rmin}R$$

$$I_{Rmin} = I_{Zmin} + I_L$$

$$I_L = \frac{V_Z}{R_L} = \frac{20}{1.2K\Omega} = 16.67mA$$

$$I_{Rmin} = 2mA + 16.67mA = 18.67mA$$

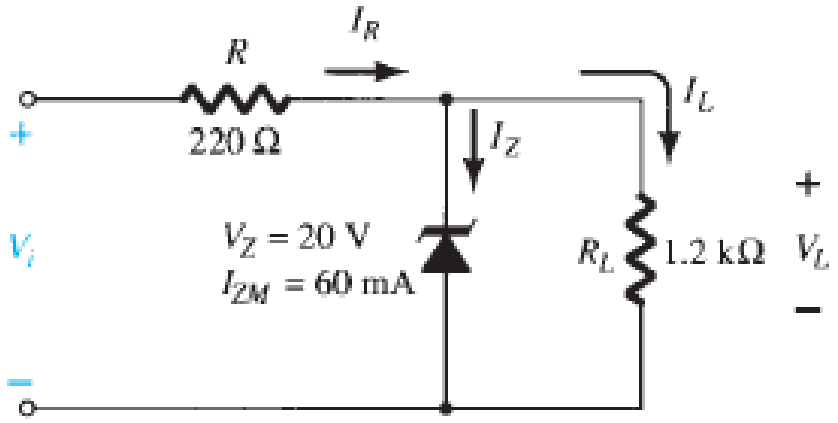
$$V_{imin} = 20 + 18.67mA * 220\Omega = 24.107V$$

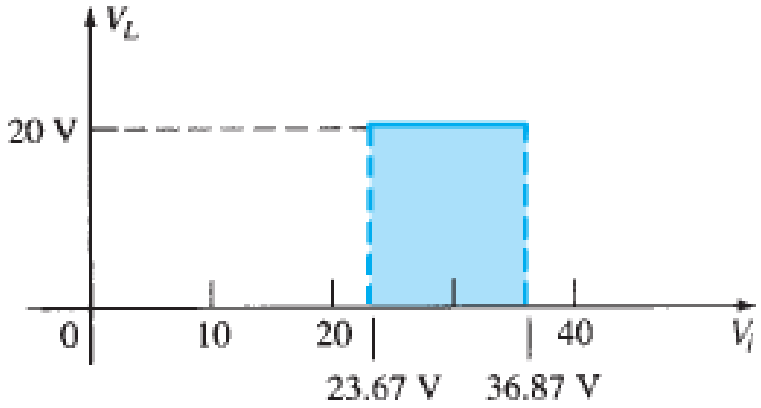
$$V_{imax} = V_Z + I_{Rmax}R$$

$$I_{Rmax} = I_{Zmax} + I_L$$

$$I_{Rmax} = 60mA + 16.67mA = 76.67mA \quad V_{imax} = 20 + 76.67mA * 220\Omega = 36.86V$$

CASE-3: Fixed R_L , Variable Vi

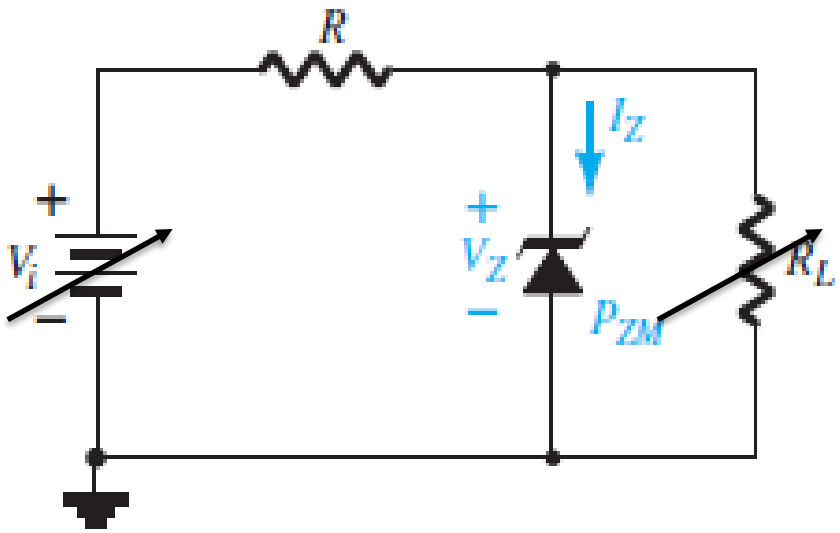




CASE-4: Variable supply voltage and a variable load

Worst case conditions for Zener Diode:

1. For the diode to enter into to the breakdown region, the necessary condition is $I_Z \geq I_{Zmin}$.



I_Z can become less than I_{Zmin} when

(i) I_L increases or R_L decreases.
(ii) R increases or I_R decreases.
(iii) Vin decreases.

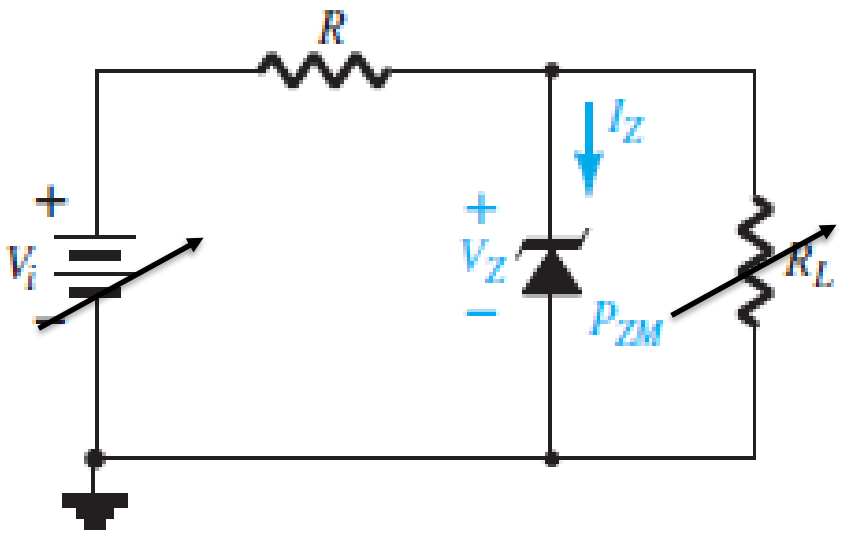
Hence the value for Rmax to ensure $I_Z \geq I_{Zmin}$ is

$$R_{max} = \frac{V_{imin} - V_Z}{I_{Zmin} + I_{Lmax}}$$

CASE-4: Variable supply voltage and a variable load

Worst case conditions for Zener Diode:

2. *The upper limit for the Zener current is* $I_Z < I_{Zmax}$.



I_Z can become greater than I_{Zmax} when

(i) I_L decreases or R_L increases.
(ii) R decreases or I_R increases.
(iii) Vin increases.

Hence the value for Rmin is to ensure $I_Z < I_{Zmax}$ is

$$R_{min} = \frac{V_{imax} - V_Z}{I_{Zmax} + I_{Lmin}}$$

CASE-4: Variable supply voltage and a variable load

6. Design a Zener voltage regulator that maintains Vo at 10V for input voltage variation of 20V±10% and load current variation of 30mA ±20%. Given $I_{Zmin} = 2mA$ and $P_{Zmax} = 0.5W$

Vimin = 20 V - 2V = 18V

Vimax = 2V + 2V = 22 V

I_{Lmin} = 30mA – 6mA = 24mA

I_{Lmax} = 30mA + 6mA = 36mA

$$R_{max} = \frac{V_{imin} - V_Z}{I_{Zmin} + I_{Lmax}} = \frac{18 - 10}{2mA + 36mA} = 210.5\ \Omega$$

$$R_{min} = \frac{V_{imax} - V_Z}{I_{Zmax} + I_{Lmin}} = \frac{22 - 10}{50mA + 24mA} = 162.16\ \Omega$$

$$210.5\ \Omega \leq R \leq 162.16\ \Omega$$

THANK YOU

Department of Electronics and Communication

ELECTRONIC PRINCIPLES AND DEVICES

Department of Electronics and Communication Engineering

ELECTRONIC PRINCIPLES AND DEVICES

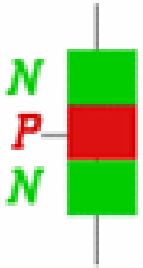
TRANSISTORS

BJT (Bipolar Junction Transistor)

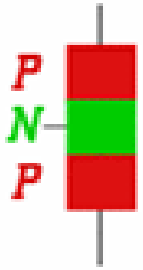
Department of Electronics and Communication.

BJT Transistor: Introduction

- A **bipolar junction transistor (BJT)** is a ***three terminal device*** consisting of either a p-type semiconductor or n-type semiconductor sandwiched between opposite types .It has **two p–n junctions** connected back-to-back.



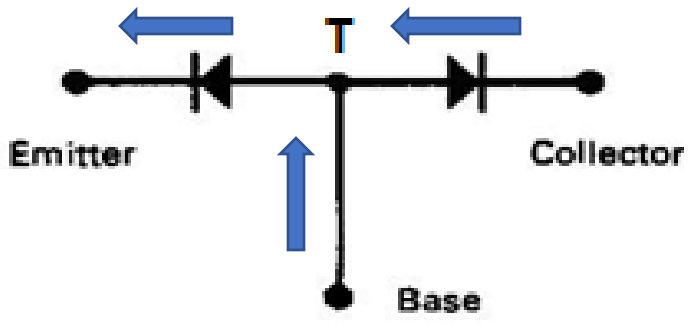
- In a BJT, the operation depends on the active participation of both the **majority carriers**, and the **minority carriers**; hence the name **"bipolar"**.



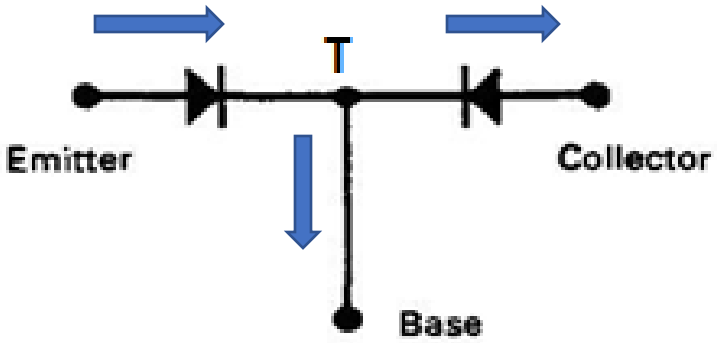
- The combination of two terms ***transfer + resistor*** results in **TRANSISTOR** as the current is transferred from a low to a high-resistance circuit.

BJT Transistor: Construction

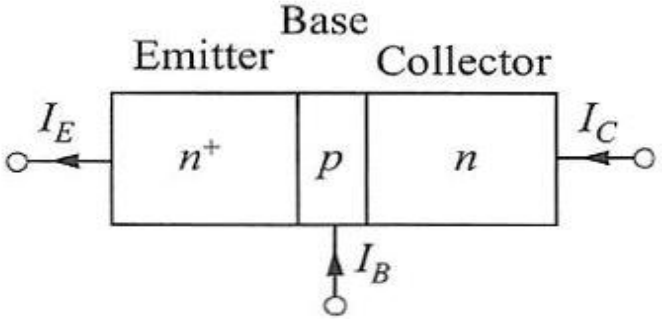
➢The three terminals of a Bipolar junction transistor are Emitter, Base & Collector.

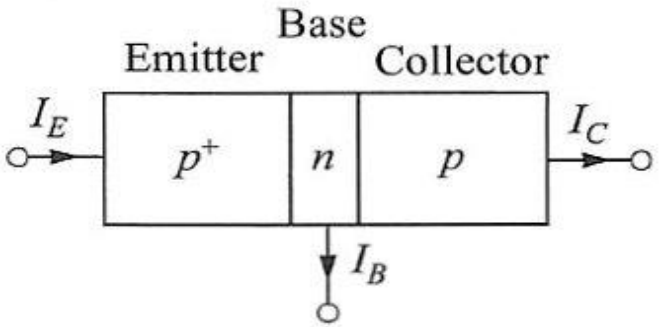


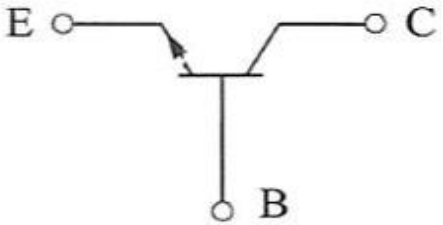
n-p-n



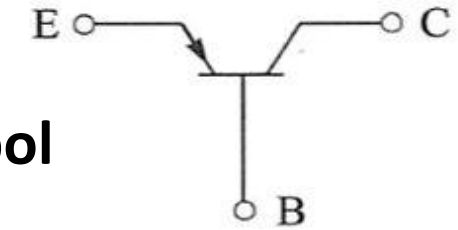
p-n-p

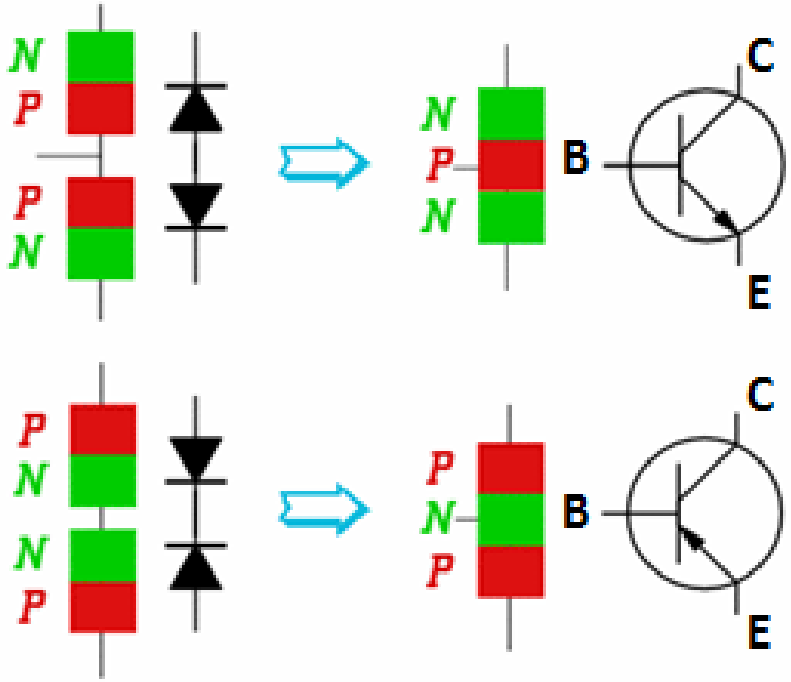






Transistor Symbol





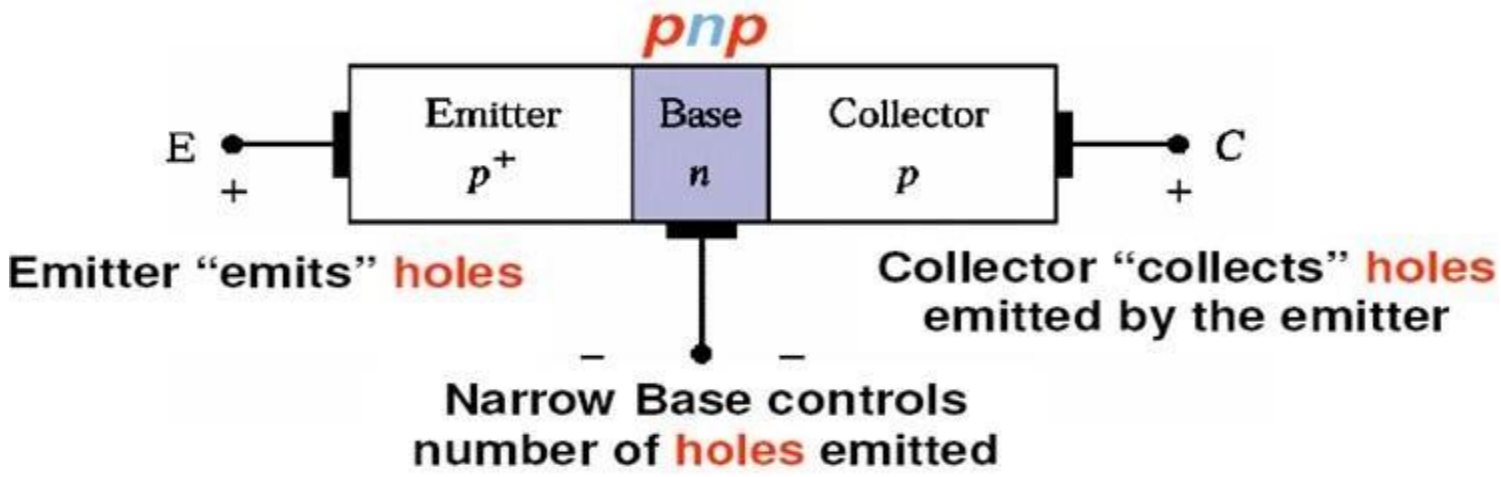
- The **Emitter (E)** is the portion of the transistor that **supplies** charge carriers (either electrons or holes) and it is a **heavily doped** region. The area is moderate in size.

- The **Base (B)** is the **middle** portion of the transistor that forms **two PN junction** between the emitter and the collector and it is a **lightly doped** region. It is the smallest in width of all the three regions.

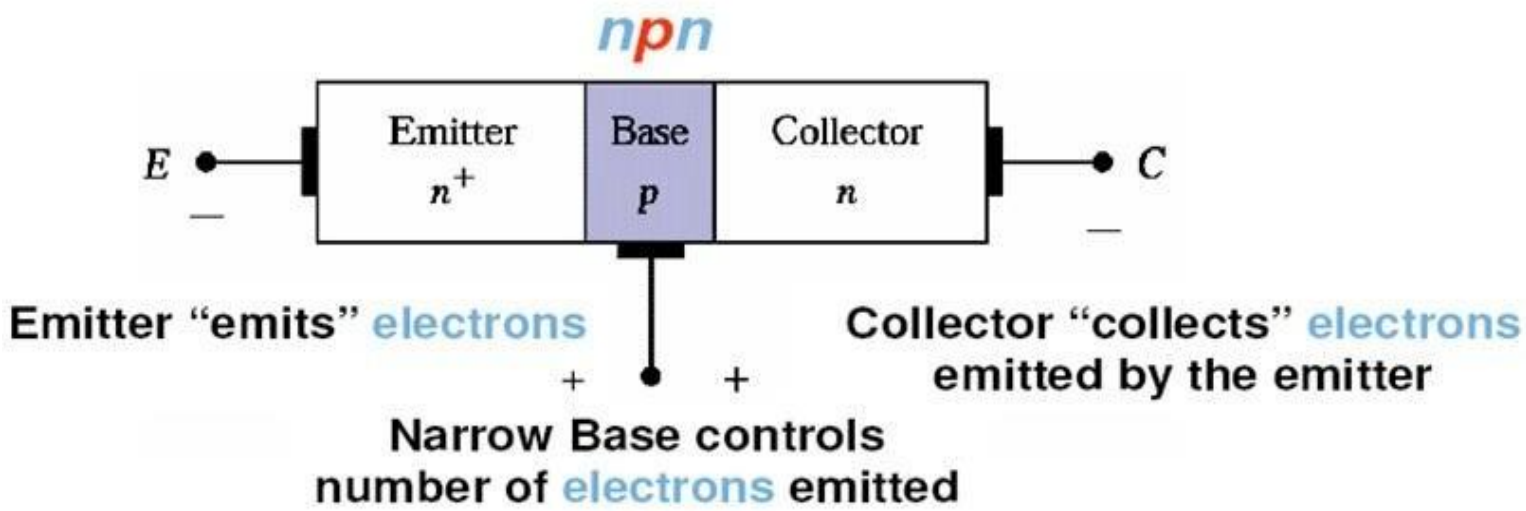
- The **Collector (C)** is the portion of the transistor that **collects** charge carriers (either electrons or holes) and it is a **moderately doped** region. It is the widest of all the three regions as maximum heat is dissipated in this region.

Types of BJTs

1. pnp transistor:



2. npn transistor:



Transistor Configurations

Based on the terminal common to the input and output side of the transistor, following are the transistor configurations:

1)**Common Base (CB)** configuration

2)**Common Emitter (CE)** configuration

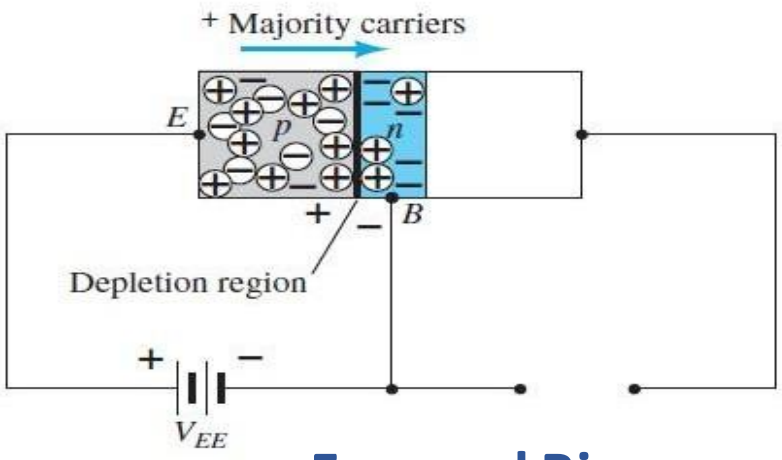
3)**Common Collector (CC)** configuration

BJT Operation

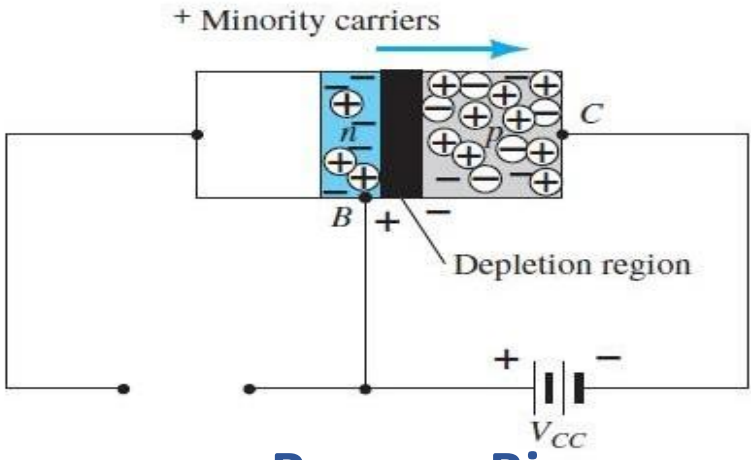
The transistor operated in **Common Base** configuration, with the external sources, **VEE** and **Vcc**, connected as shown:

- The emitter – base junction is **forward biased**
- The collector – base junction is **reverse biased**

- **As the EB junction is forward biased the current flow is because of majority charge carriers.**
- **Similarly as the CB junction is reverse biased the current flow is because of minority charge carriers (Hence wider depletion region)**



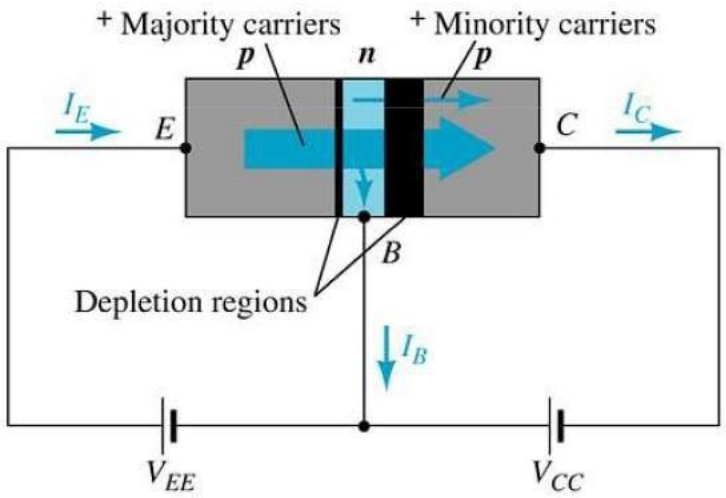
Forward Bias



Reverse Bias

BJT Operation

- A large number of majority carriers will diffuse across the forward biased p–n junction into the n -type material.
- Since the n -type material is very thin and lightly doped, a very small number of these (holes) will recombine with the electrons in base region and flow through the base terminal as base current (is typically in the order of microamperes).
- Thus, a larger number of these majority carriers from the emitter region will diffuse across the reverse-biased junction into the p -type material connected to the collector terminal.



Currents in a BJT

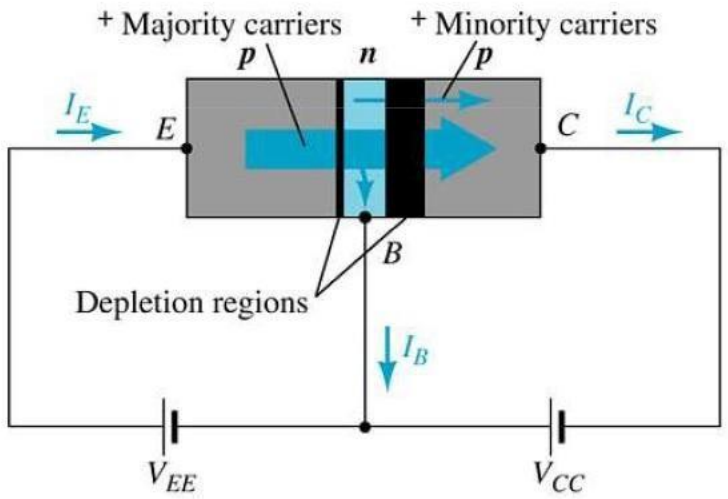
BJT Operation (pnp Transistor)

- Applying KCL to the transistor, we get

$$I_E = I_C + I_B$$

- The collector current, comprises two components—the majority and the minority carriers.
- The minority-current is called as leakage current (I_{CO} - I_C with emitter terminal Open).
- Therefore the total collector current is given as

$$I_C = I_{C_{\text{majority}}} + I_{CO_{\text{minority}}}$$



Currents in a BJT

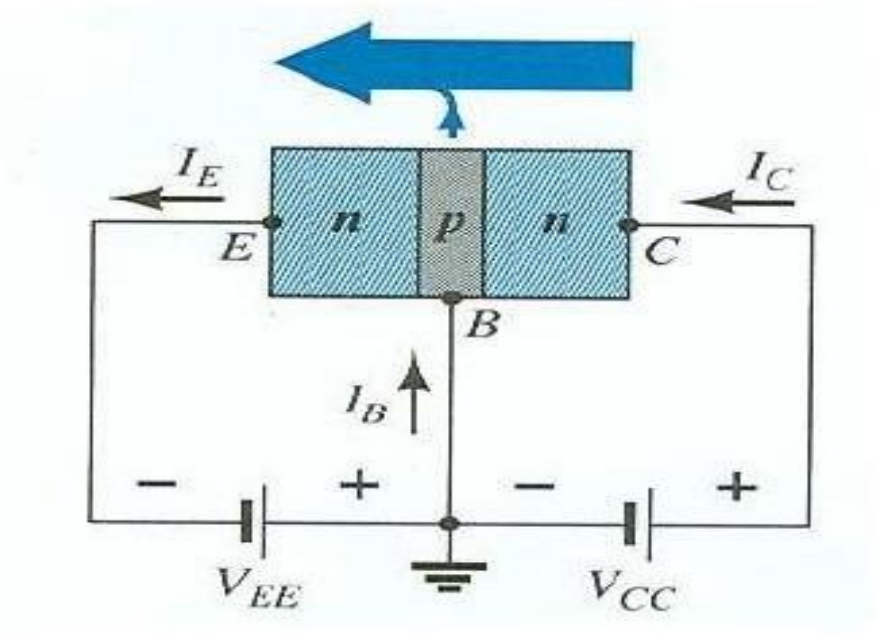
Currents in a transistor

- Emitter current is the sum of the collector and base currents:

$$I_E = I_C + I_B$$

- The collector current is comprised of two currents:

$$I_C = I_{C\,(Majority)} + I_{CO\,(Minority)}$$



Current directions in a BJT

BJT Biasing and Modes of operation

A Transistor has two p-n junctions.

1) Emitter-base (EB) Junction
2) Collector-base (CB) Junction

- Each junction can either be **forward or reverse biased** independently.
- Depending on the bias we have the following regions of operation of BJT

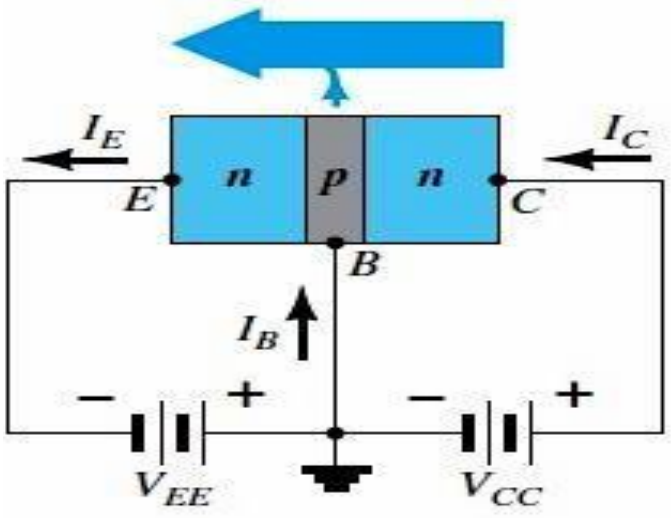
Regions of Operation	Emitter base Junction	Collector-base Junction	Application
Active region(*commonly used*)	Forward biased	Reverse biased	Transistor works as an Amplifier
Saturation region	Forward biased	Forward biased	Transistor works as a switch (ON)– Digital Application
Cut-off region	Reverse biased	Reverse biased	Transistor works as a switch (OFF)– Digital Application
Inverse active region(rarely used)	Reverse biased	Forward biased	Transistor works as an Attenuator

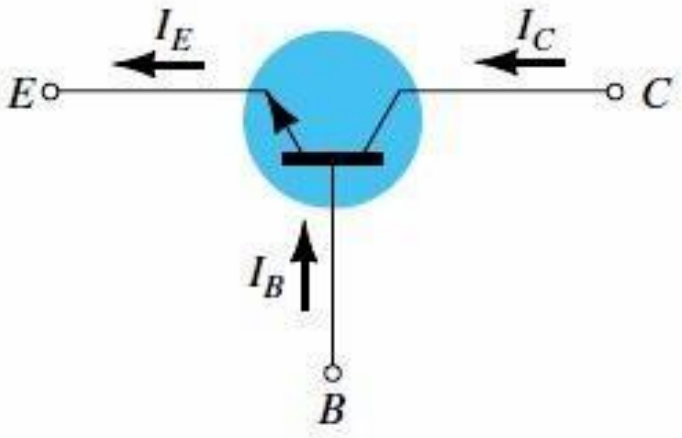
Common Base Configuration

- The arrow in the diagram indicates the direction of the emitter current.

- Easy way to remember matching the letters *npn* of the transistor type and with the appropriate letters of the phrases "*not pointing in*"

- The ***NPN*** transistor requires two voltage sources **V_{EE}** and **V_{CC}** to bias the two junctions respectively.



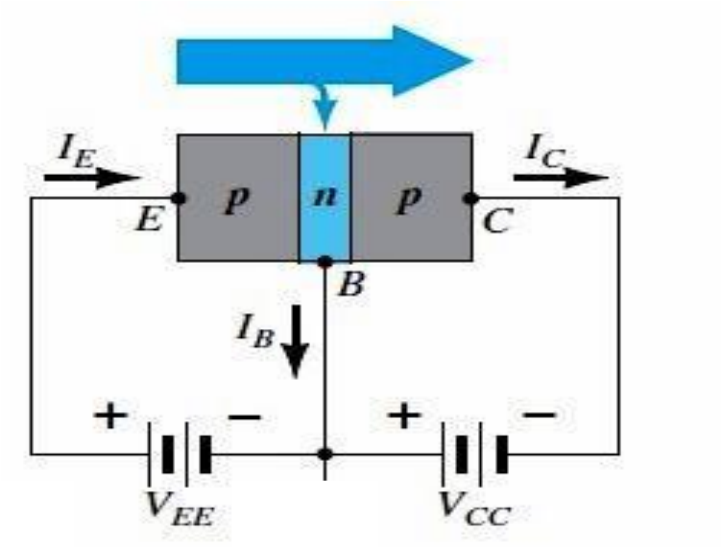


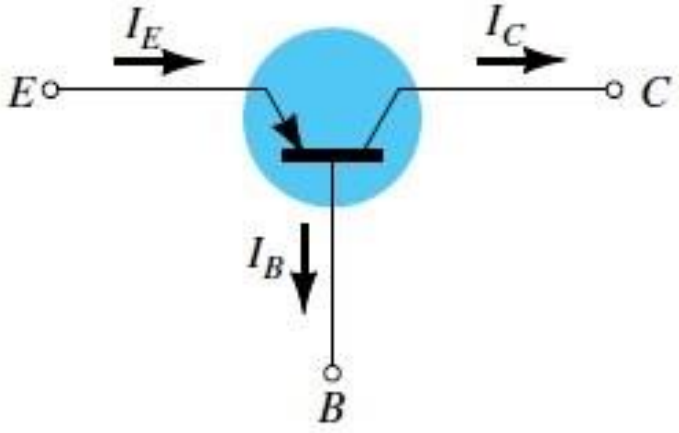
V_{BE} **V_{CB}**

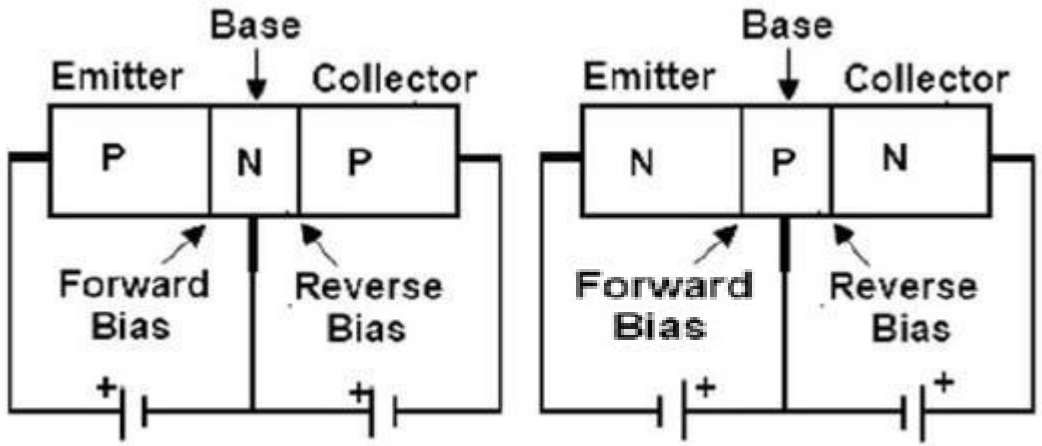
Common Base Configuration

- The arrow in the diagram, indicates the direction of the emitter current and matching the letters *pnp* of the transistor type and with the appropriate letters of the phrases "*pointing in permanently*"

- The ***PNP*** BJT requires two voltage sources **V_{EE}** and **V_{CC}** to bias the two junctions respectively.







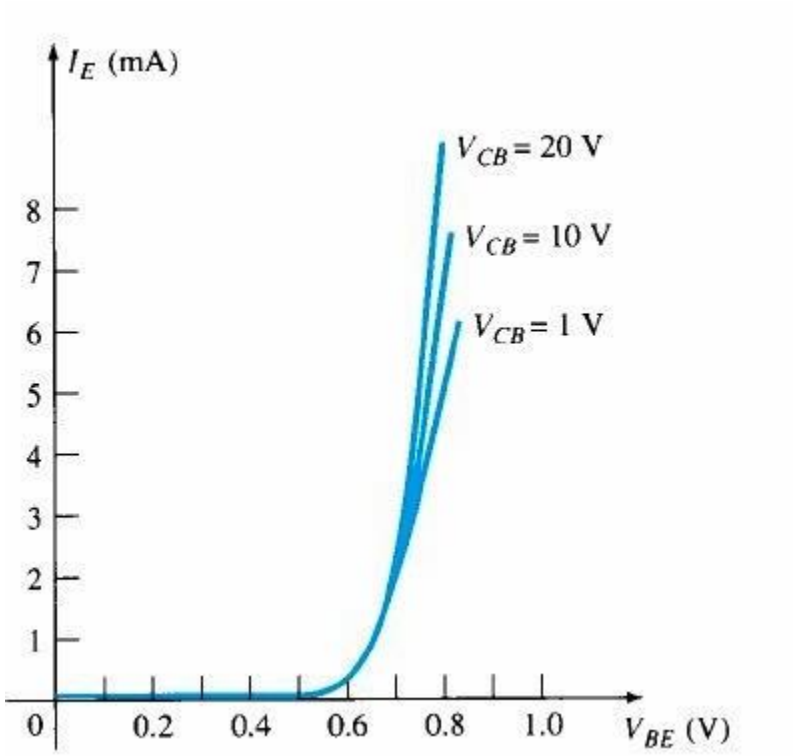
The biasing of ***PNP*** and ***NPN*** transistors to operate in active region

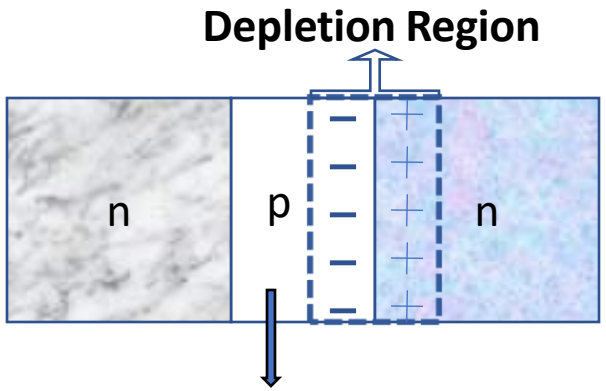
- Since the analogy of transistor is two diodes connected back-to-back. One diode is ***forward biased*** and the other is ***reverse biased*** for the device to operate in **active region**.

- Hence, biasing the ***emitter base junction (EB Jn)*** in forward bias condition and ***collector base junction (CB Jn)*** in reverse bias condition, gives the input characteristic of the device.

CB - Input Characteristics

For the transistor in CB configuration, when the output voltage V_{CB} is increased, it causes an ***increase*** in the emitter current and hence the graph **shifts inwards or towards the left**.





Narrower Base width
(Less chances of recombination)

Base Width Modulation

The input characteristic of BJT (Si) for varying output voltage V_{CB}

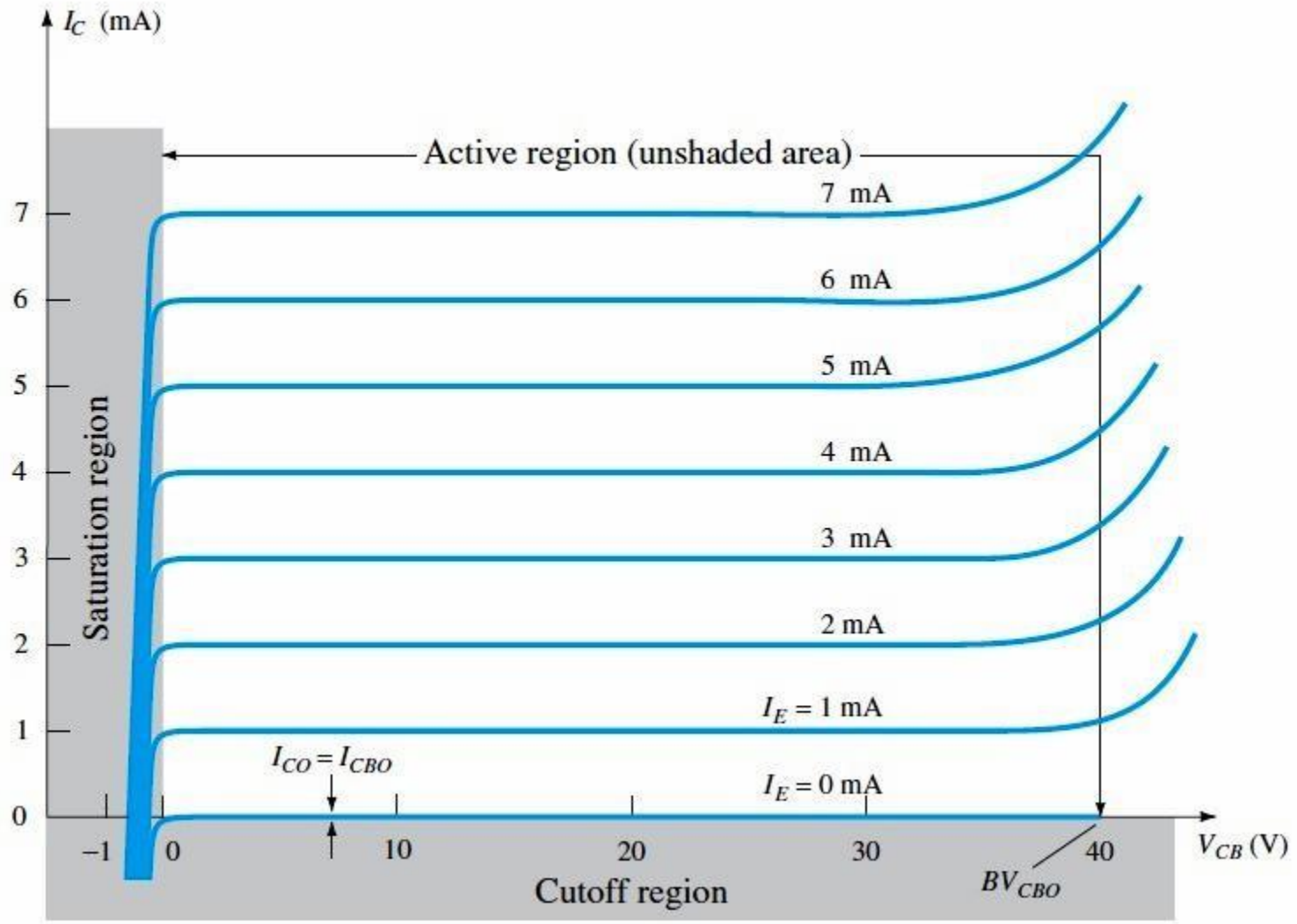
Base Width Modulation or Early Effect :

- A greater reverse bias across the collector- base junction increases the collector-base depletion width. There is a variation in the width of the base in a bipolar transistor due to a variation in the applied base-to-collector voltage.

- Base-narrowing has two consequences that affect the current:
  - There is a lesser chance for recombination within the "smaller" base region.
  - The charge gradient is increased across the base, and consequently, the current of minority carriers injected across the collector-base junction increases.

- The Early effect is observed as an increase in the collector or "output“ current with increasing collector-emitter voltage.

CB - Output Characteristics

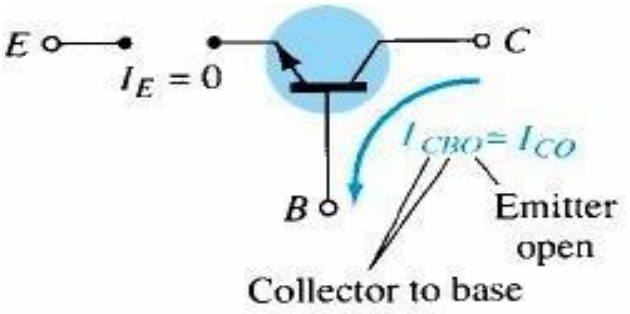


The output characteristic of BJT (Si) for varying input current I_E

CB - Output Characteristics

- **Active region**: The operating range of the amplifier. It is noticed that I_E is approximately equal to I_C ($I_E \approx I_C$). **BJT** is a current controlled device in the active region and is independent of the output voltage V_{CB}

- **Cut-off region**: The region where the collector current I_C is approximately equal to 0 ($I_C < I_{CBO}$). The device is basically **OFF** i.e., there's no input voltage, but only reverse – bias output voltage and negligible reverse saturation current



Reverse saturation current

- **Saturation region**: The region to the left of $V_{CB} = 0V$. Note the exponential increase in collector current I_C as V_{CB} approaches 0V. In this region, I_C depends on V_{CB} but is independent of I_E

CB Configuration - Approximations

- **Emitter and collector current**: $I_E \approx I_C$.

- **Base – emitter voltage (V_{BE})**: $V_{BE} = 0.7V$ (Si).

Alpha (α): Ratio of I_C to I_E.

$$\alpha_{dc} = \frac{I_C}{I_E}$$

$$I_C = \alpha I_E + I_{CBO}$$

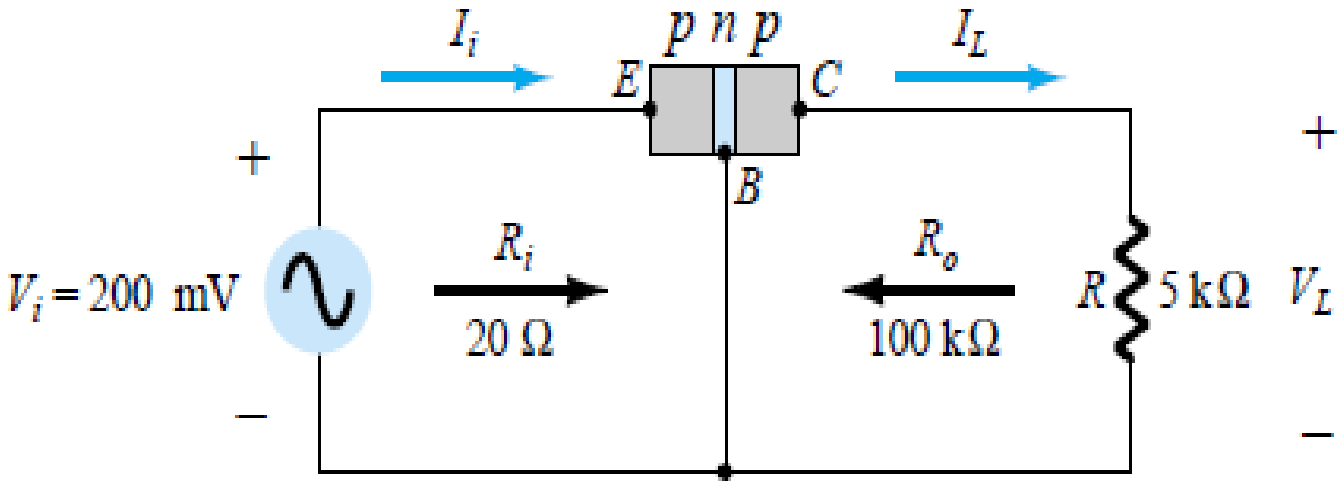
Ideally: α = 1
In reality: α is between 0.9 and 0.998

For AC mode:

$$\alpha_{ac} = \left.\frac{\Delta I_C}{\Delta I_E}\right|_{V_{CB}=\text{constant}}$$

α - Current amplification factor or current gain in CB config.

Common Base Amplifying action



$$I_i = \frac{V_i}{R_i} = \frac{200\text{ mV}}{20\ \Omega} = \mathbf{10\ mA}$$

If we assume for the moment that $\alpha_{ac} = 1$ ($I_c = I_e$),

$$I_L = I_i = 10\text{ mA}$$

and

$$V_L = I_L R$$
$$= (10\text{ mA})(5\text{ k}\Omega)$$
$$= \mathbf{50\ V}$$

The voltage amplification is

$$A_v = \frac{V_L}{V_i} = \frac{50\text{ V}}{200\text{ mV}} = \mathbf{250}$$

Numericals

1. A common base transistor amplifier has an input resistance of 20 Ω and output resistance of 100 kΩ. The collector load is 1 kΩ. If a signal of 500 mV is applied between emitter and base, find the voltage amplification. Assume α_{ac} to be nearly one.

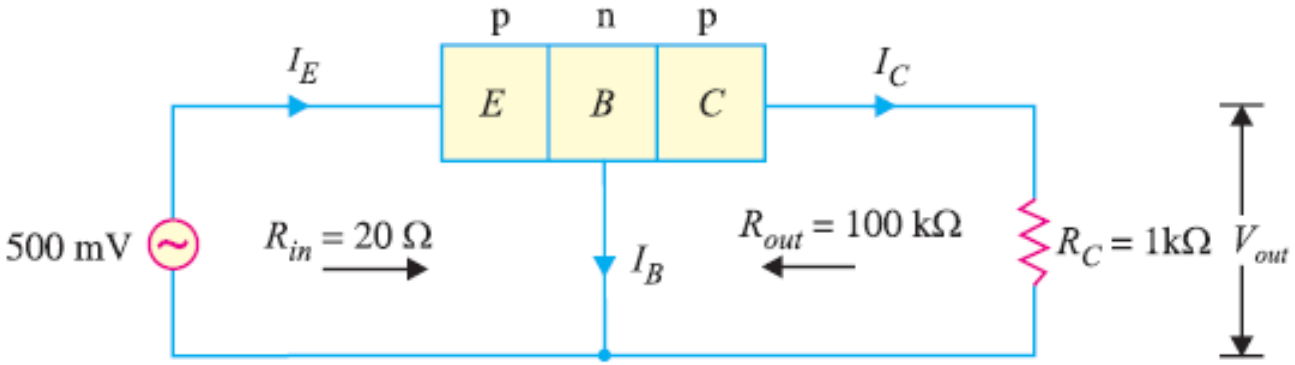


Fig. 1

Input current, $I_E = \dfrac{\text{Signal}}{R_{in}} = \dfrac{500\text{ mV}}{20\ \Omega} = 25$ mA. Since α_{ac} is nearly 1, output current, $I_C = I_E = 25$ mA.

$$\text{Output voltage, } V_{out} = I_C R_C = 25\text{ mA} \times 1\text{ k}\Omega = 25\text{ V}$$

$$\therefore \quad \text{Voltage amplification, } A_v = \frac{V_{out}}{\text{signal}} = \frac{25\ V}{500\ mV} = 50$$

2. In a common base connection, I_E = 1mA, I_C = 0.95mA. Calculate the value of I_B .

Using the relation,

$$I_E = I_B + I_C$$

$$1 = I_B + 0.95$$

$$I_B = 1 - 0.95 = 0.05 \text{ mA}$$

3. In a common base connection, current amplification factor is 0.9. If the emitter current is 1mA, determine the value of base current.

Here, $\alpha = 0.9, \quad I_E = 1 \text{ mA}$

Now $\alpha = \dfrac{I_C}{I_E}$

or $I_C = \alpha I_E = 0.9 \times 1 = 0.9 \text{ mA}$

Also $I_E = I_B + I_C$

$\therefore$ Base current, $I_B = I_E - I_C = 1 - 0.9 = 0.1 \text{ mA}$

4. In a common base connection, I_C = 0.95 mA and I_B = 0.05 mA. Find the value of α.

$$\text{We know } I_E = I_B + I_C = 0.05 + 0.95 = 1 \text{ mA}$$

$$\therefore \quad \text{Current amplification factor, } \alpha = \frac{I_C}{I_E} = \frac{0.95}{1} = \mathbf{0.95}$$

5. In a common base connection, the emitter current is 1mA. If the emitter circuit is open, the collector current is 50 μA. Find the total collector current. Given that α = 0.92.

$$\text{Here, } I_E = 1 \text{ mA}, \alpha = 0.92, \quad I_{CBO} = 50 \ \mu\text{A}$$

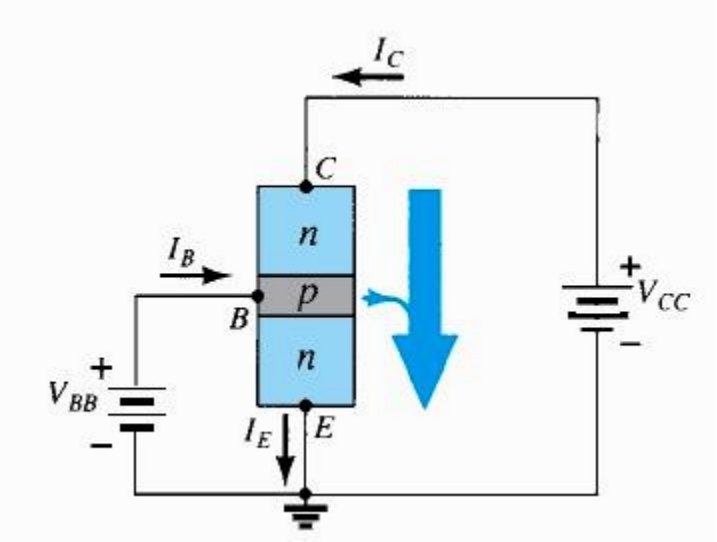
$$\therefore \quad \text{Total collector current, } I_C = \alpha I_E + I_{CBO} = 0.92 \times 1 + 50 \times 10^{-3}$$

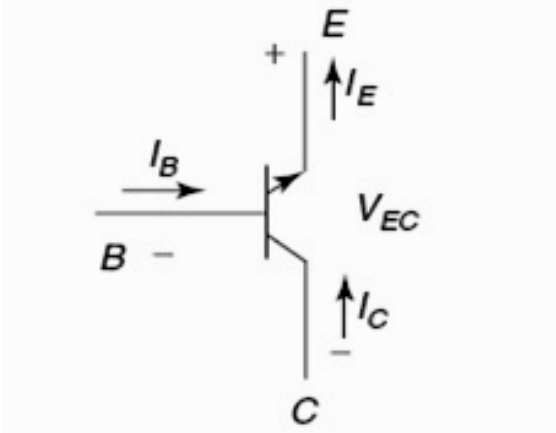
$$= 0.92 + 0.05 = \mathbf{0.97 \text{ mA}}$$

Common Emitter Configuration

- The **arrow** in the diagram, indicates the direction of the emitter current.

- The ***NPN*** BJT requires two voltage sources $\mathbf{V_{BB}}$ and $\mathbf{V_{CC}}$ to bias the two junctions respectively.

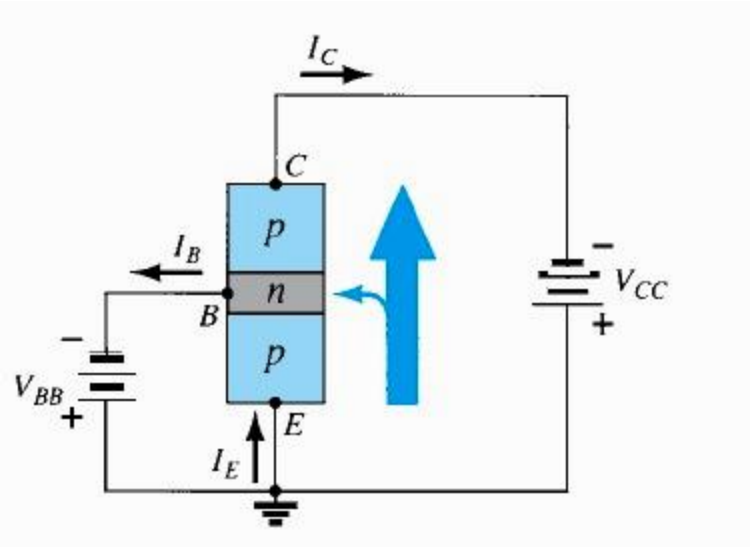


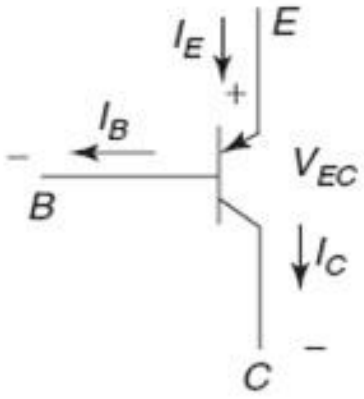


An ***NPN*** transistor used in Common Emitter (CE) configuration

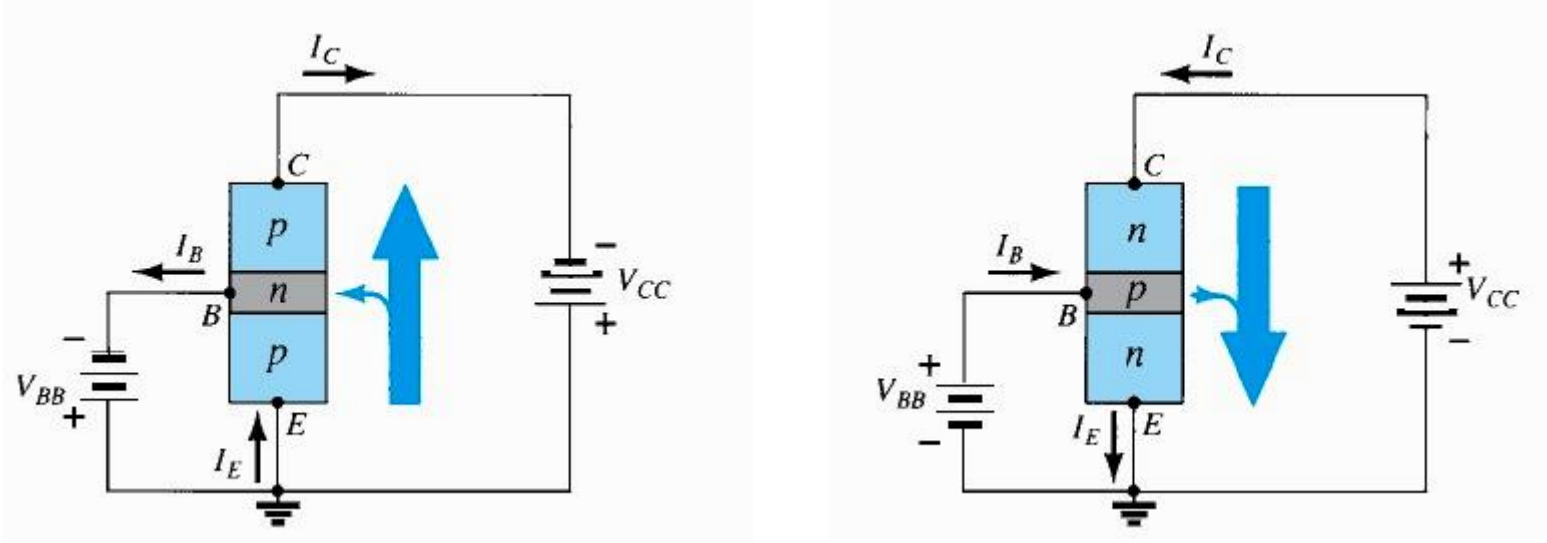
- The **arrow** in the diagram, indicates the direction of the emitter current and we can observe that the ***direction*** of the current in this type of transistor is **opposite** to that of a NPN transistor.

- The ***PNP*** BJT requires two voltage sources **V_{BB}** and **V_{CC}** to bias the two junctions respectively.





A ***PNP*** transistor used in Common Emitter (CE) configuration



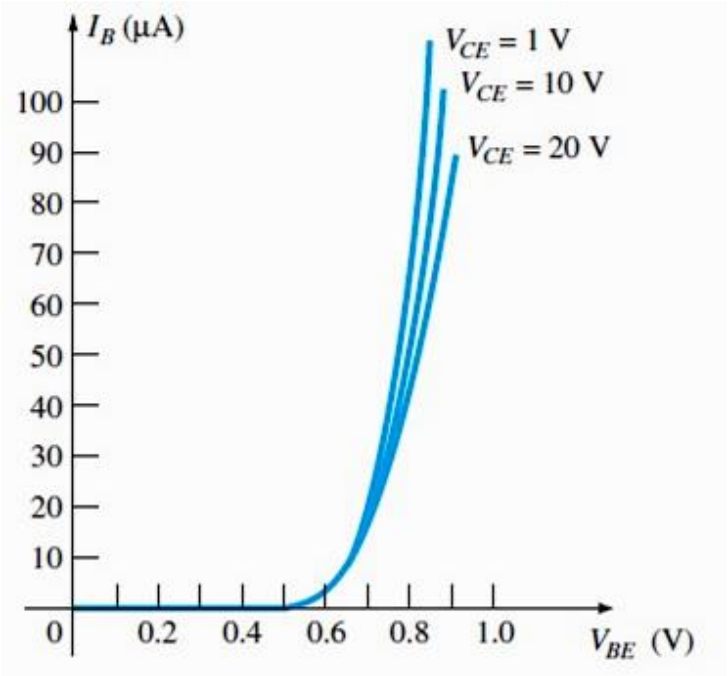
The biasing of ***PNP*** and ***NPN*** transistor to operate in active region

- The analogy of a BJT is two diodes connected back-to-back. One diode is ***forward biased*** and the other is ***reverse biased*** for the device to operate in **active region**.

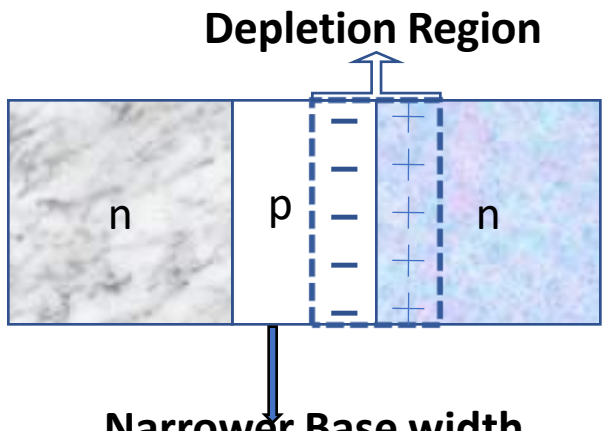
- Hence, biasing the ***emitter base junction (EB Jn)*** in forward bias condition and ***collector base junction (CB Jn)*** in reverse bias condition, gives the input characteristic of the device.

CE Configuration - Input Characteristics

- For the transistor in CE configuration, I_B is the input current (usually in uA) and V_{BE} is the input voltage. A plot of I_B v/s V_{BE} is called the input characteristics.
- The characteristics resemble the forward bias characteristics of a diode.
- When the output voltage $\mathbf{V_{CE}}$ is increased, this high voltage causes a decrease in the current I_B through the device and hence the graph **shifts towards the right**.



The input characteristic of BJT (Si) for varying output voltage $\mathbf{V_{CE}}$



Narrower Base width
(Less chances of recombination)

Base Width Modulation

Base Width Modulation or Early Effect :

- A greater reverse bias across the collector- emitter junction increases the base-**emitter** depletion width. There is a variation in the width of the base in a bipolar transistor due to a variation in the applied collector- to-emitter voltage.

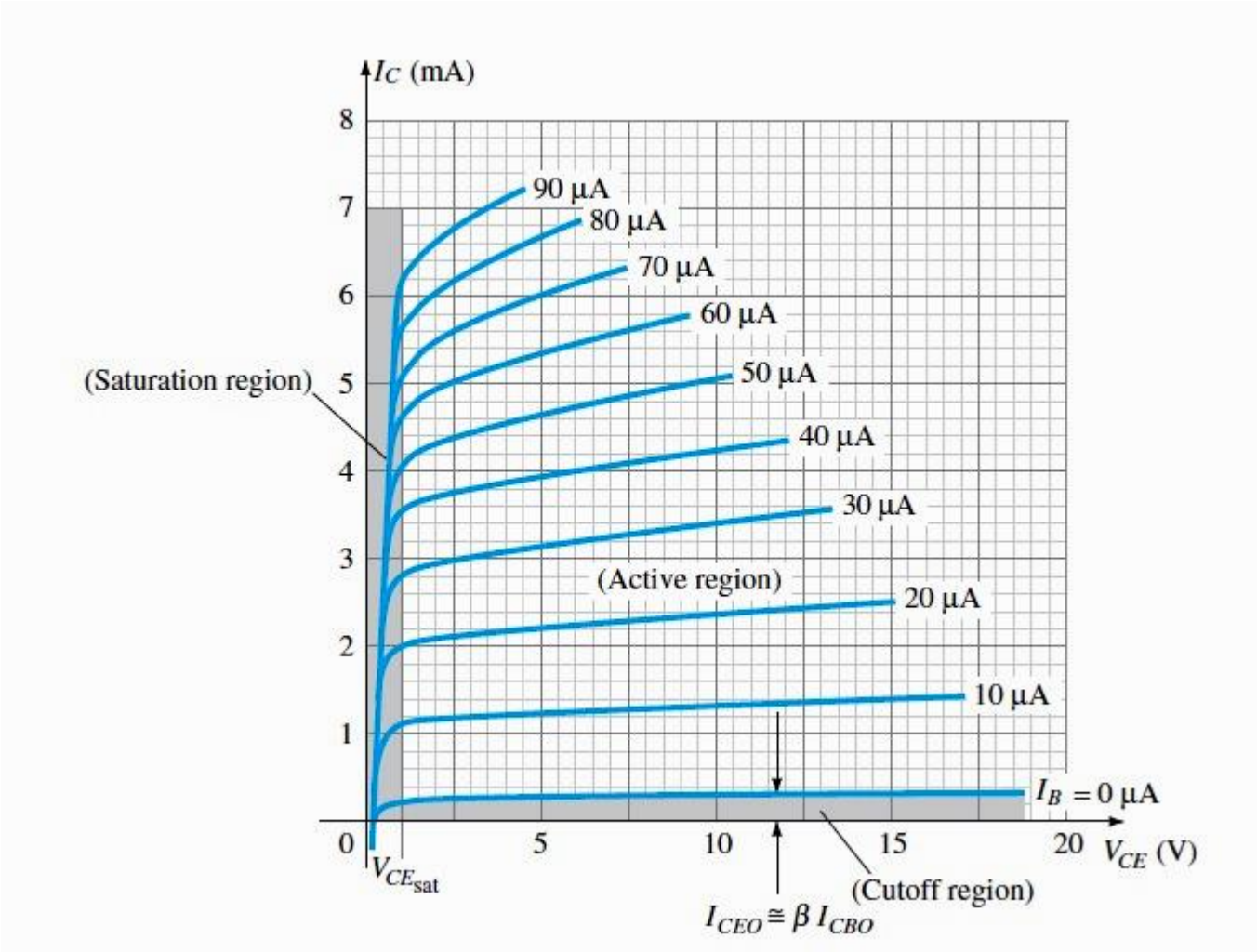
- Base-narrowing has two consequences that affect the current:

• There is a lesser chance for recombination within the "smaller" base region & so I_B decreases further .

• The charge gradient is increased across the base, and consequently, the current of minority carriers injected across the collector-base junction increases.

- The Early effect is observed as an increase in the collector or "output“ current with increasing collector-emitter voltage.

CE Configuration - Output Characteristics



The output characteristic of BJT (Si) for varying input current I_B

CE Configuration - Output Characteristics

- **Active region**: The B-E junction is forward biased. Collector voltage is greater than the base voltage which reverse biases the C-B junction.

$$V_{CE} > V_{BE}$$

In this region, I_C depends on I_E and is almost independent of V_{CE}.

$$Ic = \beta * I_B.$$

- **Cut-off region**: Both junctions are ***reverse biased***. No base current. Only a small reverse leakage current between C and E. For practical purposes, current is assumed to be zero.

- **Saturation region:** The E-B and C-B junctions are forward biased.
  Ic varies with V_{CE} and is ***independent*** of I_B and β.

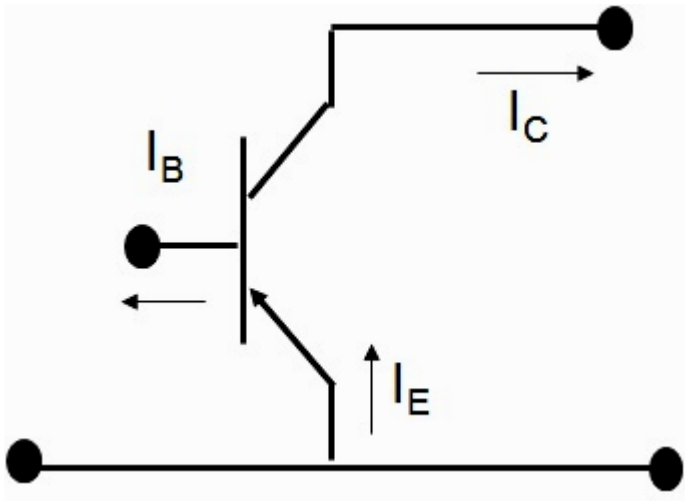
CE Active region

$$I_C = \alpha I_E + I_{CB0}$$

$$= \alpha (I_C + I_B) + I_{CB0} \qquad (\because I_E = I_C + I_B)$$

$$I_C = \frac{\alpha I_B + I_{CB0}}{1-\alpha}$$

Let $\beta = \frac{\alpha}{(1-\alpha)}$ $\qquad [\therefore \frac{1}{(1-\alpha)} = 1+\beta]$



$$I_C = \beta I_B + (1+\beta) I_{CB0}$$

$$\boxed{I_C = \beta I_B + I_{CE0}}$$

$(\because I_{CE0} = (1+\beta) I_{CB0})$

$I_{CE0} \approx \beta I_{CB0}$

or

$$I_{CE0} = \left.\frac{I_{CB0}}{1-\alpha}\right|_{I_B = 0\ uA}$$

$$\boxed{I_C = \beta I_B}$$ Neglecting leakage current I_{CE0}

$$\boxed{50 \le \beta \le 500}$$

Relationship between α and β

A relationship can be developed between α and β using the basic relationships introduced thus far. Using $\beta = I_C / I_B$ we have $I_B = I_C / \beta$, and from $\alpha = I_C / I_E$ we have $I_E = I_C / \alpha$. Substituting into

$$I_E = I_C + I_B$$

$$I_C / \alpha = I_C + I_C / \beta$$

and dividing both sides of the equation by I_C will result in

$$\frac{1}{\alpha} = 1 + \frac{1}{\beta}$$

or

$$\beta = \alpha\beta + \alpha = (\beta + 1)\alpha$$

so that

$$\boxed{\alpha = \frac{\beta}{1+\beta} \quad \text{or} \quad \beta = \frac{\alpha}{(1-\alpha)}}$$

$$I_C = \beta I_B$$

$$I_E = I_C + I_B$$

$$= \beta I_B + I_B$$

$$I_E = (\beta + 1) I_B$$

1. Find the value of β if (i) α = 0.9 (ii) α = 0.98 (iii) α = 0.99.

(i) $\alpha = 0.9$

$$\beta = \frac{\alpha}{1-\alpha} = \frac{0.9}{1-0.9} = 9$$

(ii) $\alpha = 0.98$

$$\beta = \frac{\alpha}{1-\alpha} = \frac{0.98}{1-0.98} = 49$$

(iii) $\alpha = 0.99$

$$\beta = \frac{\alpha}{1-\alpha} = \frac{0.99}{1-0.99} = 99$$

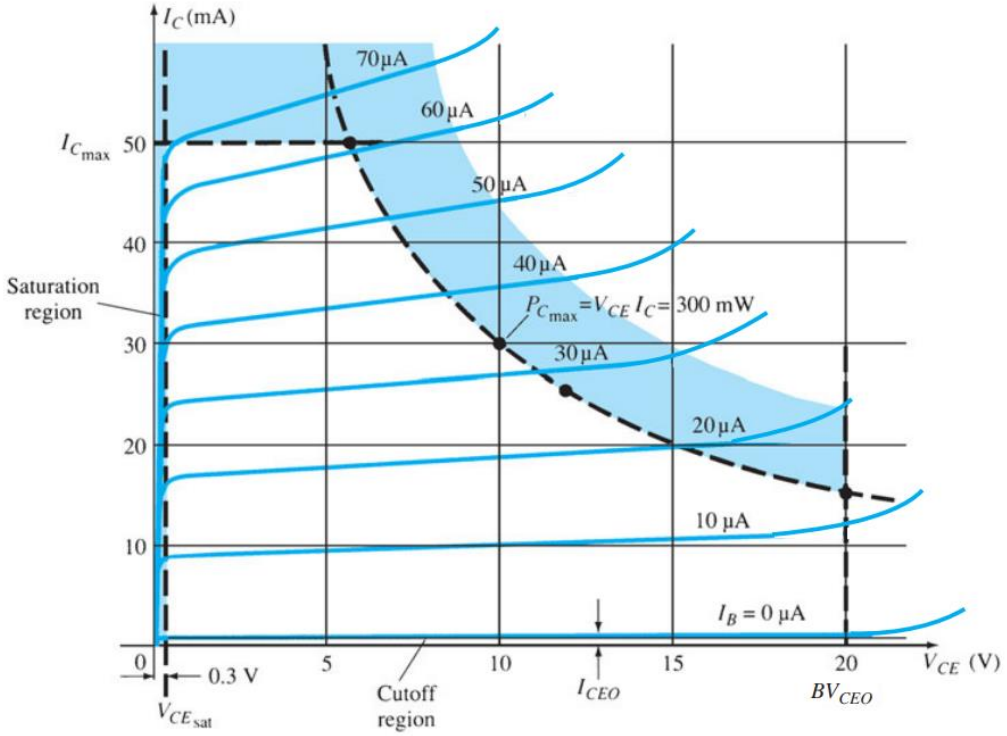
Limits of Operation

The limit of operation ensures that the transistor works within its maximum rating with minimum signal distortion. It is specified in the data sheet.

V_{CESat} : Specifies the minimum V_{CE} that can be applied without transistor going to saturation region.

The maximum power dissipation is given as

$$P_{C_{max}} = V_{CE} I_C$$



Defining the linear (undistorted) region of operation for a transistor.

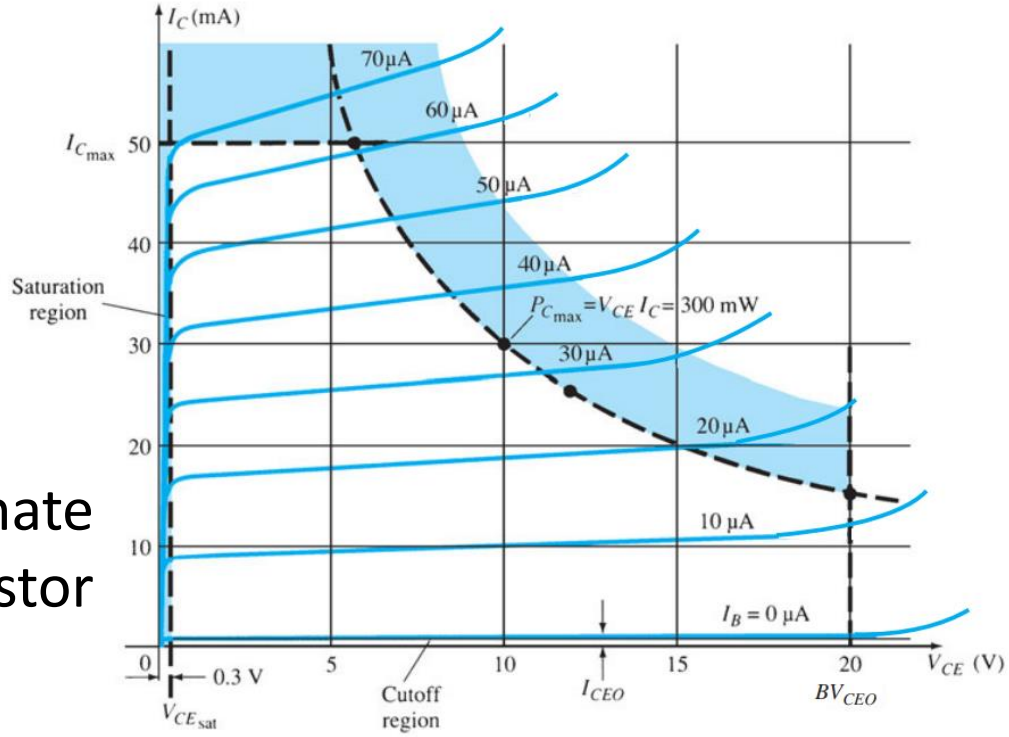
Limits of Operation

For example if,

$$P_{C_{max}} = V_{CE} I_C = 300 \text{ mW}$$

- At $I_C = I_{Cmax}$ i.e, 50 mA, $V_{CE} = 6v$
- At $V_{CE} = V_{CEmax}$ i.e, 20V, $I_C = 15mA$
- At $I_C = I_{Cmax}/2$, $V_{CE} = 12v$

These three points give a rough estimate of the power curve and the transistor must be operated with in this region.



Defining the linear (undistorted) region of operation for a transistor.

Limits of Operation

The cutoff region is the region below $I_C = I_{CEO}$ (= βI_{CBO}). This region must also be avoided to have minimum distortion .

If the characteristic curve/specification sheet is not available, one must ensure the following conditions are satisfied to ensure minimum distortion.

$$I_{CEO} \leqq I_C \leqq I_{C_{max}}$$
$$V_{CE_{sat}} \leqq V_{CE} \leqq V_{CE_{max}}$$
$$V_{CE} I_C \leqq P_{C_{max}}$$

For CB Characteristics, P_{Cmax} is defined as

$$P_{C_{max}} = V_{CB} I_C$$

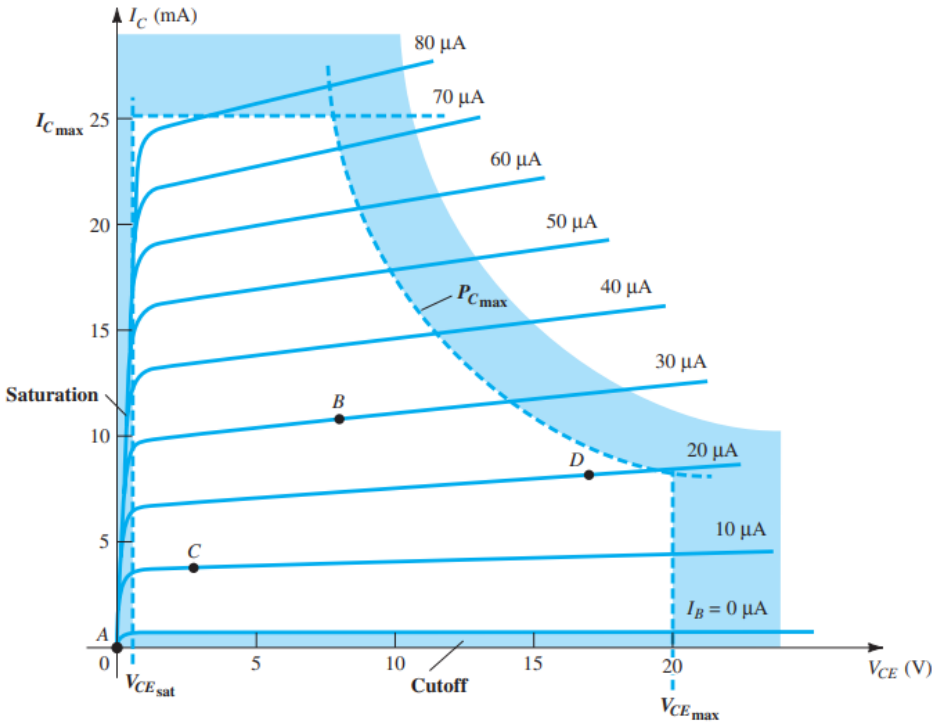
Operating Point

Biasing refers to application of DC voltages to establish a fixed level of current and voltage in a transistor.

For a transistor amplifier, the resulting DC current and voltage on the characteristic curve establish an **Operating Point**. It gives the DC values of I_B, I_C and V_{CE} in the absence of AC input

The operating point is also called as **Quiescent point** or **Q point** where **Quiescent** means 'silent' i.e., in the absence of ac signal.

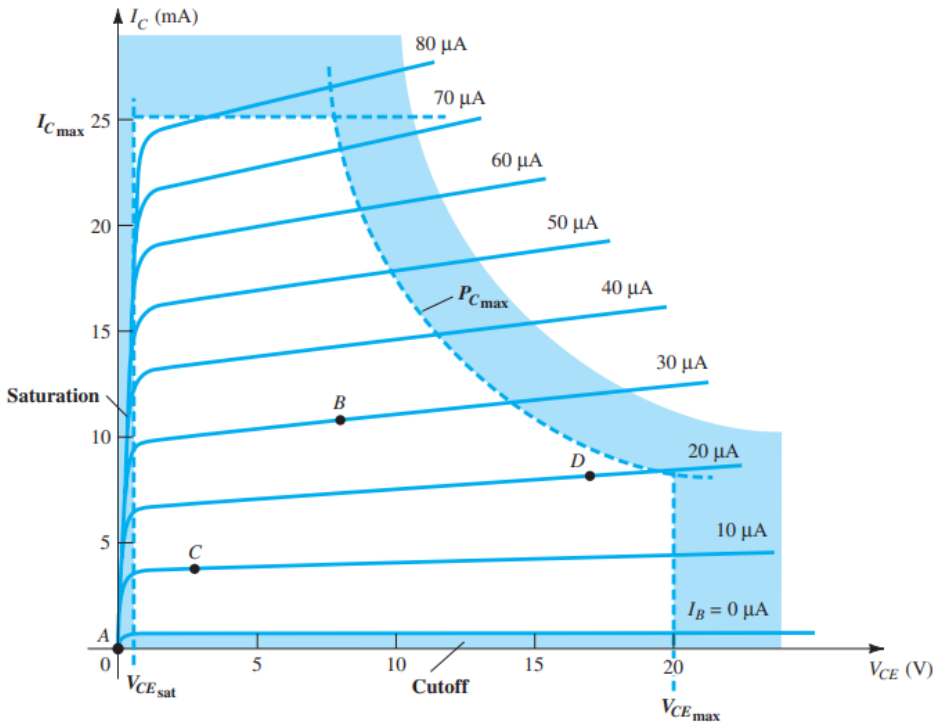
Biasing circuit can be used to set the operating point within the active region. A, B, C, D are some of the possible operating points.



Various operating points within the limits of operation of a transistor.

Operating Point

- **Q Point at A**: If there is no bias, the device is completely off, resulting in Q point at A. This point is not suitable as complete input range can not be covered for amplification.
- **Q Point at B**: can cover a large range of input signal. It is also far from both cut-off and saturation region.
- **Q Point at C**: This is near to both cutoff and saturation region thus limiting the swing of input signal.
- **Q Point at D**: as is near to the maximum voltage and power level, limits the positive swing of input signal



Various operating points within the limits of operation of a transistor.

Operating Point

- Figure 4.1 shows a general output device characteristic with four operating points indicated.

The maximum ratings are indicated on the characteristics of Fig. 4.1 by

- ✓ a horizontal line for the maximum collector current I_{Cmax} and a vertical line at the maximum collector-to-emitter voltage V_{CEmax} .
- ✓ The maximum power constraint is defined by the curve P_{Cmax}.
- ✓ At the lower end of the scales are the cutoff region , defined by I_B=0 mA, and the saturation region , defined by V_{CE} =V_{CEsat} .

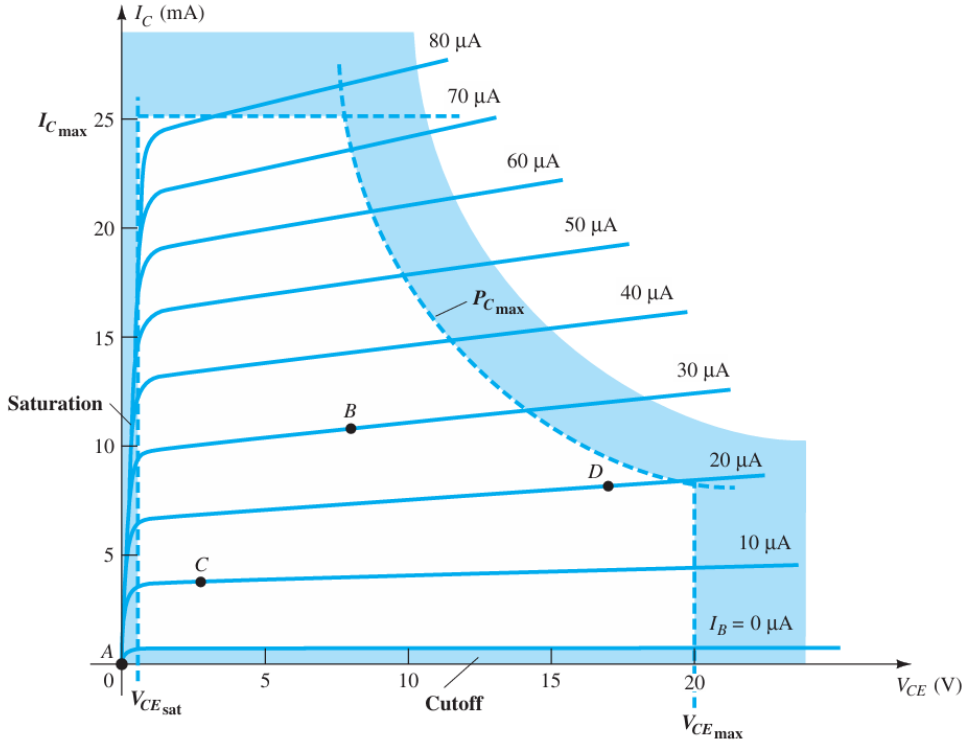


FIG. 4.1
Various operating points within the limits of operation of a transistor.

Operating Point

Temperature also has its effect on the Operating point.

Temperature causes the device parameters like transistor current gain (β_{ac}) and the transistor leakage current (I_{CEO}) to change.

As temperature increases, I_{CEO} increases, resulting in changing the Q point. Thus the network design must also consider temperature stability to reduce the changes in Q point.

The variation of operating point due to variation in temperature is indicated by stability factor (S). Higher the stability of the circuit, better is the circuit.

Transistor Biasing

Transistor Biasing:

Biasing is the process of providing DC voltage which helps in the functioning of the circuit. A transistor is based in order to make the base- emitter junction forward biased and base-collector junction reverse biased, so that it maintains in active region, to work as an amplifier.

Need for DC biasing:

If a signal of very small voltage is given to the input of BJT, it cannot be amplified. Because, for a BJT, to amplify a signal, two conditions have to be met.

- The input voltage should exceed cut-in voltage for the transistor to be ON.
- The BJT should be in the linear / active region, to be operated as an amplifier.

DC biasing:

- The operating point is a fixed point on the characteristics and is also called quiescent point, denoted by Q-point. The term biasing means the application of dc voltages used to setup a fixed level of current and voltage. Called “dc basing” or “biasing analysis”
- This step determines both the region of operation and the small-signal parameters of each device

Different regions of operation of BJT

Operation in the cutoff, saturation, and linear regions of the BJT characteristic are pro vided as follows:

1. Linear-region (or Active region) operation:

Base–emitter junction forward-biased Base–collector junction reverse-biased

2. Cutoff-region operation:

Base–emitter junction reverse-biased Base–collector junction reverse-biased

3. Saturation-region operation:

Base–emitter junction forward-biased Base–collector junction forward-biased

Types of BJT Biasing Configuration

Objective is to **determine the terminal voltages and currents of *BJT transistor* and obtain the conditions that ensure biasing in the Active /Linear mode**

Types of Biasing (only the first 3 is included in the syllabus)

1. Fixed Bias configuration
2. Emitter- bias configuration
3. Voltage –divider bias configuration
4. Collector-feedback
5. Emitter-follower
6. Common-base

Fixed-Bias Configuration

- The fixed-bias circuit of Fig. 4.2 is the simplest transistor dc bias configuration. Hence, it is also called as simple biasing.
- For dc, f = 0 Hz, and XC = 1>2pfC = 1>2p(0)C = ∞Ω.

Forward Bias of Base–Emitter

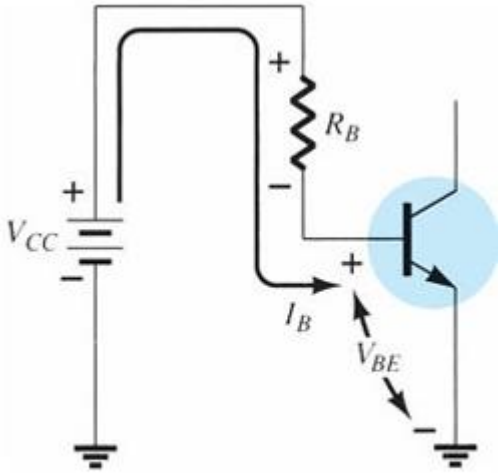
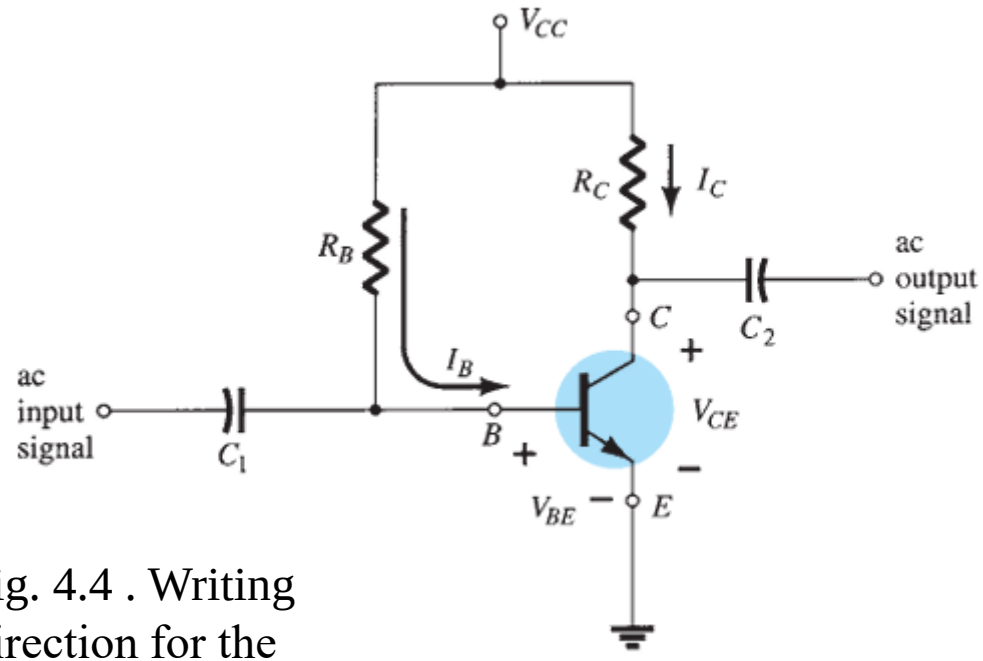


FIG. 4.4
Base–emitter loop.



Consider first the base–emitter circuit loop of Fig. 4.4 . Writing Kirchhoff's voltage equation in the clockwise direction for the loop, we obtain $+V_{CC} - I_B R_B - V_{BE} = 0$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

Fixed-Bias Configuration

The supply voltage V_{CC} and the base–emitter voltage V_{BE} are constants, the selection of a base resistor R_B sets the level of base current for the operating point.

Collector–Emitter Loop

The collector–emitter section of the network appears in Fig. 4.5 with the indicated direction of current I_C and the resulting polarity across R_C $\mathbf{I_C = \beta I_B}$

- Changing R_C to any level will not affect the level of I_B or I_C as long as the device in the active region.
- The level of R_C will determine the magnitude of V_{CE}.

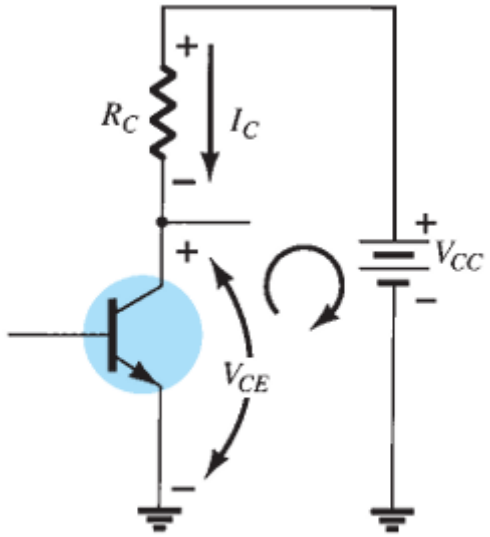


FIG. 4.5
Collector–emitter loop.

$$V_{CE} + I_C R_C - V_{CC} = 0$$

$$\boxed{V_{CE} = V_{CC} - I_C R_C}$$

$$\boxed{V_{CE} = V_C - V_E}$$

$$\boxed{V_{BE} = V_B - V_E}$$

Since, emitter is ground

$$\boxed{V_{CE} = V_C}$$

$$\boxed{V_{BE} = V_B}$$

Fixed-Bias Configuration

Determine the following for the fixed-bias configuration of Fig. 4.7

a. I_{B_Q} and I_{C_Q}.
b. V_{CE_Q}.
c. V_B and V_C.
d. V_{BC}.

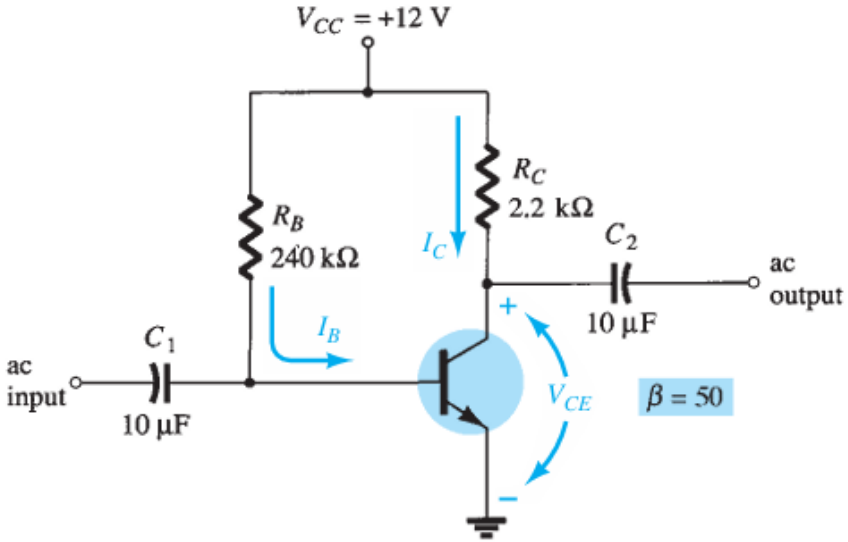


FIG. 4.7
DC fixed-bias circuit for Example 4.1.

a) $$I_{B_Q} = \frac{V_{CC} - V_{BE}}{R_B} = \frac{12\text{ V} - 0.7\text{ V}}{240\text{ k}\Omega} = \mathbf{47.08\ \mu A}$$

$$I_{C_Q} = \beta I_{BQ} = (50)(47.08\ \mu\text{A}) = \mathbf{2.35\ mA}$$

b) $$V_{CE_Q} = V_{CC} - I_C R_C = 12\text{ V} - (2.35\text{ mA})(2.2\text{ k}\Omega) = \mathbf{6.83\ V}$$

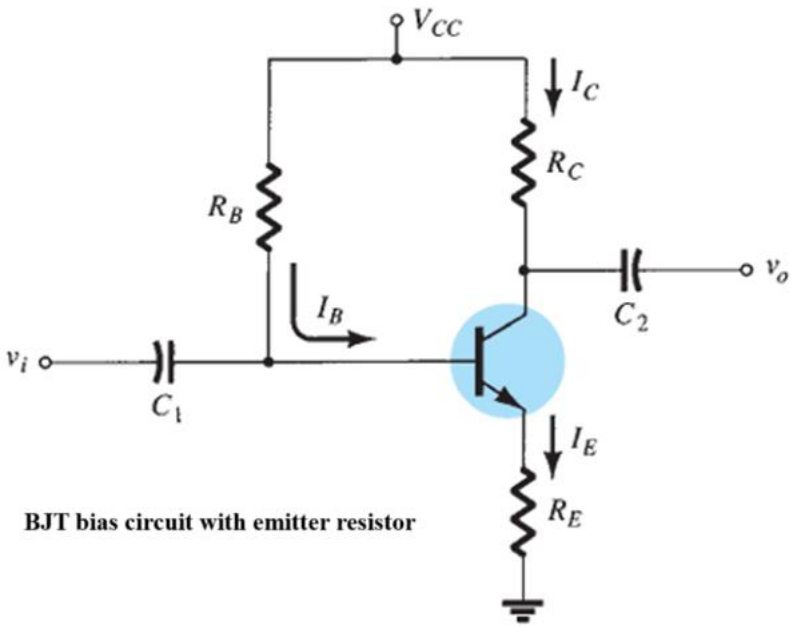
c) $$V_B = V_{BE} = \mathbf{0.7\ V}$$
$$V_C = V_{CE} = \mathbf{6.83\ V}$$

d) $$V_{BC} = V_B - V_C = 0.7\text{ V} - 6.83\text{ V} = \mathbf{-6.13\ V}$$

The negative sign revealing that the junction is reversed-biased, as it should be for linear amplification.

Emitter-Bias Configuration

- The DC bias network of fig below contains an emitter resistor to improve the stability level over that of the fixed bias configuration.



BJT bias circuit with emitter resistor

Emitter-Bias Configuration

Base–Emitter Loop

Applying Kirchhoff's voltage law around the indicated loop in the clockwise direction results in the following equation:

$$+V_{CC} - I_B R_B - V_{BE} - I_E R_E = 0$$

Since $I_E = (\beta + 1)I_B$, substitute in the above equation

$$V_{CC} - I_B R_B - V_{BE} - (\beta + I)I_B R_E = 0$$

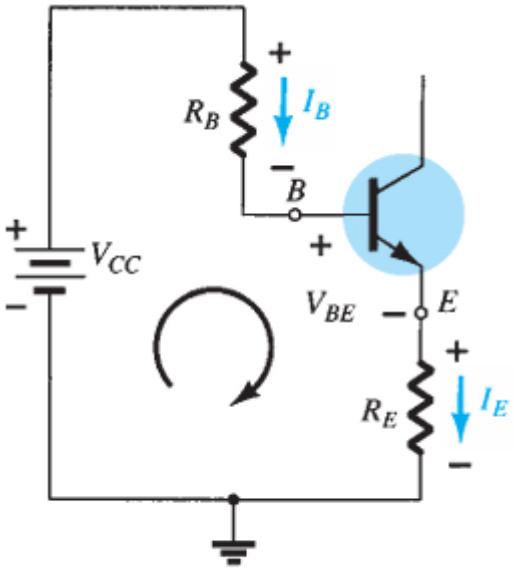
$$-I_B(R_B + (\beta + 1)R_E) + V_{CC} - V_{BE} = 0$$

Multiplying through by (-1), we have

$$I_B(R_B + (\beta + 1)R_E) - V_{CC} + V_{BE} = 0$$

$$I_B(R_B + (\beta + 1)R_E) = V_{CC} - V_{BE}$$

$$\boxed{I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)R_E}}$$



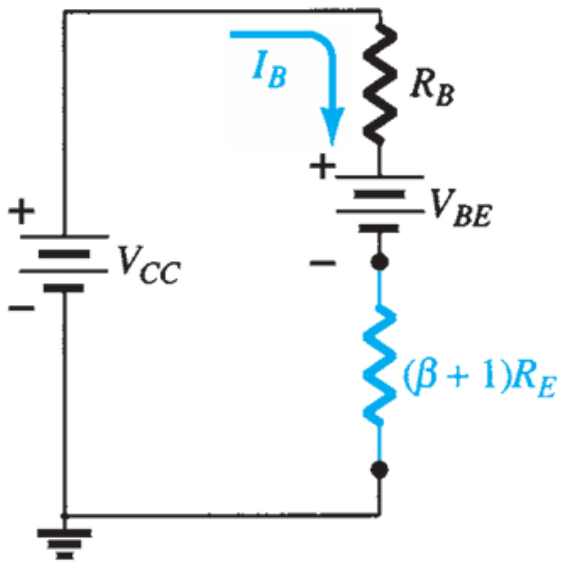
Base-emitter loop

Note: that the only difference between this equation for I_B and that obtained for the fixed bias configuration is the term $(\beta + 1)R_E$.

Emitter-Bias Configuration

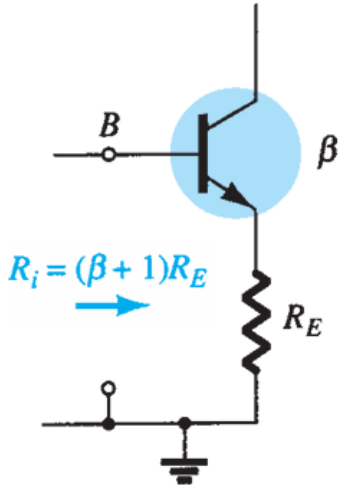
$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)R_E}$$

the network derived from this I_B equation is



- ✓ Note that aside from the base-to-emitter voltage V_{BE}, the resistor RE is reflected back to the input base circuit by a factor (β+1).
- ✓ In other words, the emitter resistor, which a part of the collector-emitter loop, "appears as" $(\beta+1)R_E$ in the base-emitter loop.
- ✓ Thus, the reflected impedance level of R_E, in the base circuit as shown in figure. Therefore, for this configuration the input impedance is given by

$$R_i = (\beta + 1)R_E$$



Emitter-Bias Configuration

Collector–Emitter Loop

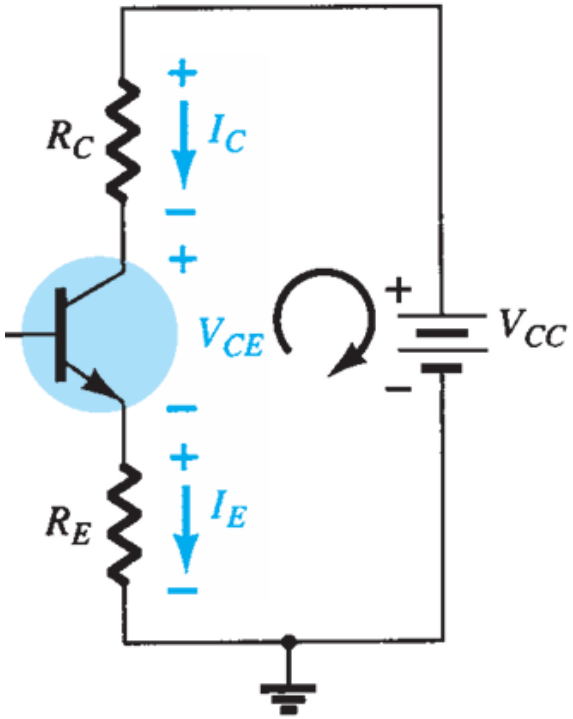
The collector–emitter loop appears as shown in figure. Applying Kirchhoff's voltage law for the indicated loop in the clockwise direction results in

$$+I_E R_E + V_{CE} + I_C R_C - V_{CC} = 0$$

Substituting $I_E \cong I_C$ and grouping terms gives

$$V_{CE} - V_{CC} + I_C(R_C + R_E) = 0$$

$$\boxed{V_{CE} = V_{CC} - I_C(R_C + R_E)}$$



Collector - Emitter loop

Voltage from emitter to ground is given by $\boxed{V_E = I_E R_E}$

Voltage between collector and emitter is $V_{CE} = V_C - V_E$

Voltage from collector to ground is given by $\boxed{V_C = V_{CE} + V_E}$

$$\boxed{V_C = V_{CC} - I_C R_C}$$

Voltage at base w.r.t to ground is given by $\boxed{V_B = V_{CC} - I_B R_B}$

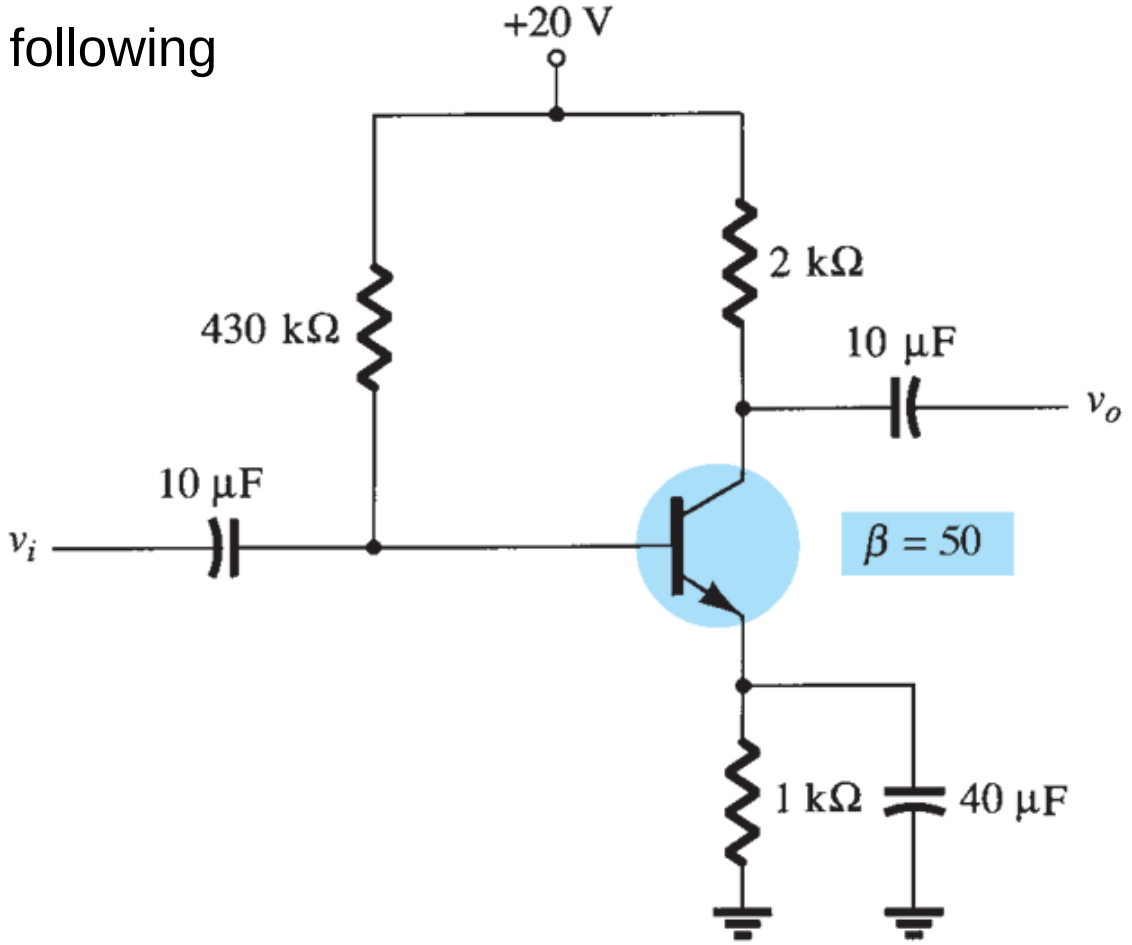
$$\boxed{V_B = V_{BE} + V_E}$$

Emitter-Bias Configuration

Problem

For the emitter-bias network of Fig. 4.23 , determine the following

a. I_B.
b. I_C.
c. V_{CE}.
d. V_C.
e. V_E.
f. V_B.
g. V_{BC}.



Emitter-Bias Configuration

Solution

a) $$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)R_E} = \frac{20\text{ V} - 0.7\text{ V}}{430\text{ k}\Omega + (51)(1\text{ k}\Omega)}$$

$$= \frac{19.3\text{ V}}{481\text{ k}\Omega} = \mathbf{40.1\ \mu A}$$

b) $$I_C = \beta I_B$$

$$= (50)(40.1\ \mu\text{A})$$

$$\cong \mathbf{2.01\ mA}$$

c) $$V_{CE} = V_{CC} - I_C(R_C + R_E)$$

$$= 20\text{ V} - (2.01\text{ mA})(2\text{ k}\Omega + 1\text{ k}\Omega) = 20\text{ V} - 6.03\text{ V}$$

$$= \mathbf{13.97\ V}$$

d) $$V_C = V_{CC} - I_C R_C$$

$$= 20\text{ V} - (2.01\text{ mA})(2\text{ k}\Omega) = 20\text{ V} - 4.02\text{ V}$$

$$= \mathbf{15.98\ V}$$

e) $$V_E = V_C - V_{CE}$$

$$= 15.98\text{ V} - 13.97\text{ V}$$

$$= \mathbf{2.01\ V}$$

f) $$V_B = V_{BE} + V_E$$

$$= 0.7\text{ V} + 2.01\text{ V}$$

$$= \mathbf{2.71\ V}$$

or

$$V_E = I_E R_E \cong I_C R_E$$

$$= (2.01\text{ mA})(1\text{ k}\Omega)$$

$$= \mathbf{2.01\ V}$$

g) $$V_{BC} = V_B - V_C$$

$$= 2.71\text{ V} - 15.98\text{ V}$$

$$= \mathbf{-13.27\ V}\ \text{(reverse-biased as required)}$$

Emitter-Bias Configuration

- **Improved Bias Stability in Emitter bias configuration**

The addition of the emitter resistor to the dc bias of the BJT provides improved stability, that is, the dc bias currents and voltages remain closer to where they were set by the circuit when outside conditions, such as temperature and transistor beta, change.

- The comparison table of the bias voltage and currents of the circuits of Fixed and emitter bias for the given value of beta= 50 and for a new value of beta = 100. The changes in I_C and V_{CE} for the same increase in beta is.

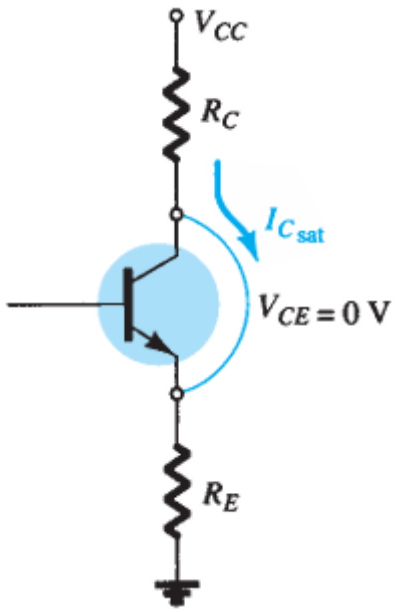
Fixed bias configuration	Emitter bias configuration
β / I_B (μA) / I_C (mA) / V_{CE} (V) 50 / 47.08 / 2.35 / 6.83 100 / 47.08 / 4.71 / 1.64	β / I_B (μA) / I_C (mA) / V_{CE} (V) 50 / 40.1 / 2.01 / 13.97 100 / 36.3 / 3.63 / 9.11
The collector current is seen to change by 100% due to the 100% change in the value of beta. The value of I_B is the same, and V_{CE} decreased by 76%	The collector current increases by about 81% due to the 100% increase in beta. I_B decreased, maintain the value of I_C —or at least reducing the overall change in I_C due to the change in beta. The change in V_{CE} has dropped to about 35%

- Thus, the emitter – bias configuration is therefore more stable than that of fixed bias for the same change in beta.

Emitter-Bias Configuration

Saturation Level

- The collector saturation level or maximum collector current for an emitter-bias design can be determined using the same approach applied to the fixed-bias configuration
- Apply a short circuit between the collector–emitter terminals as shown in below and calculate the resulting collector current.



$$I_{C_{sat}} = \frac{V_{CC}}{R_C + R_E}$$

Voltage- Divider Bias Configuration

- In the previous bias configurations, the bias current I_{CQ} and voltage V_{CEQ} were a function of the current gain β of the transistor.
- Since, β is temperature sensitive, especially for silicon transistors, and the actual value of beta is usually not well defined.
- it is necessary to develop a bias circuit that is less dependent on, or independent of, the transistor beta.
- Thus, Voltage divider bias configuration is preferred.

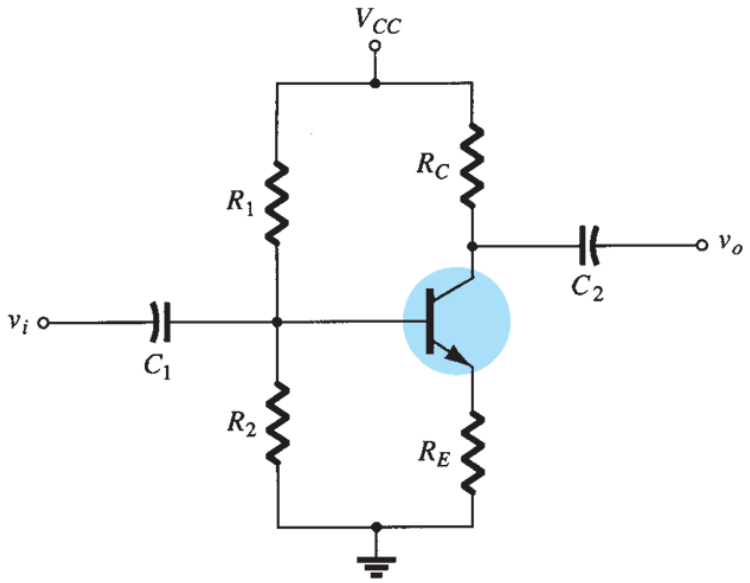


FIG. 4.28
Voltage-divider bias configuration.

Voltage- Divider Bias Configuration

- Approximate Analysis: can be applied only if specific conditions are satisfied

➢ The input section of the voltage-divider configuration can be represented by the network of Fig. 4.36

➢ The R_i is the resistance between base and ground for the transistor with the emitter resistance, with the reflected resistance between the base and emitter, similar to the Emitter bias configuration and is given by $R_i = (\beta+1)R_E$

➢ If R i is much larger than the resistance R_2 , the current I_B will be much smaller than I_2 and I_2 will be approximately equal to I_1

Since, $I_B \cong 0$, the voltage drop across R_2 is given by $\frac{R_2}{R_1+R_2}V_{CC}$

(using the voltage divider rule, hence the name of the configuration)

➢ **If $\beta R_E \geq 10R_2$, then the approximation method can be applied to determine the biasing current and voltage.**

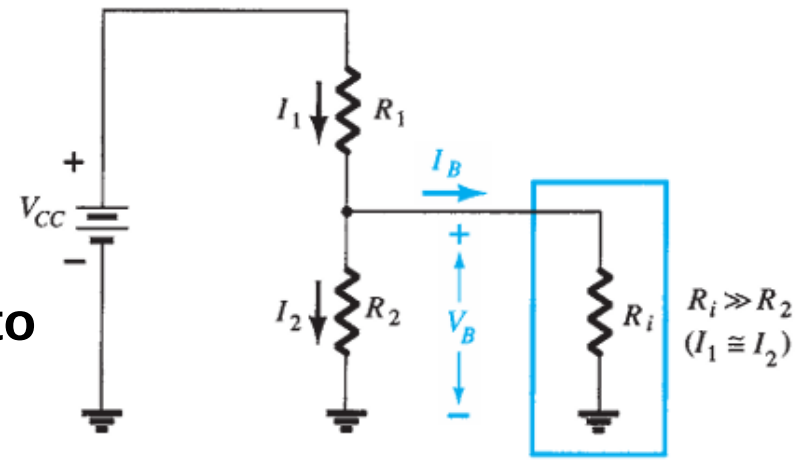


FIG. 4.36
Partial-bias circuit for calculating the approximate base voltage V_B.

Voltage- Divider Bias Configuration

- Approximate Analysis:

➢ V_E and I_E are calculated by $V_E = V_B - V_{BE}$ and $I_E = \frac{V_E}{R_E}$

➢ And $I_{C_Q} \cong I_E$

➢ The collector-to-emitter voltage is determined by $V_{CE} = V_{CC} - I_C R_C - I_E R_E$

➢ Since $I_E \cong I_C$,

$$V_{CE_Q} = V_{CC} - I_C(R_C + R_E)$$

➢ In all the biasing voltage and current equation β does not appear and the Q -point (as determined by I_{CQ} and V_{CEQ}) is therefore independent of the value of β.

➢ Transistor Saturation

$$I_{C_{sat}} = I_{C_{max}} = \frac{V_{CC}}{R_C + R_E}$$

Voltage- Divider Bias Configuration

Determine the dc bias voltage V_{CE} and the current I_C for the voltage divider configuration of Fig. 4.35 .

Solution: check the condition to apply approximate method

$$\beta R_E \geq 10R_2$$
$$(100)(1.5\ \text{k}\Omega) \geq 10(3.9\ \text{k}\Omega)$$
$$150\ \text{k}\Omega \geq 39\ \text{k}\Omega\ (\textit{satisfied})$$

I_{CQ} calculation

$$V_B = \frac{R_2 V_{CC}}{R_1 + R_2} = \frac{(3.9\ \text{k}\Omega)(22\ \text{V})}{39\ \text{k}\Omega + 3.9\ \text{k}\Omega} = 2\ \text{V}$$

$$V_E = V_B - V_{BE} = 2\ \text{V} - 0.7\ \text{V} = 1.3\ \text{V}$$

$$I_{CQ} \cong I_E = \frac{V_E}{R_E} = \frac{1.3\ \text{V}}{1.5\ \text{k}\Omega} = \mathbf{0.867\ mA}$$

V_{CEQ} Calculation

$$V_{CE_Q} = V_{CC} - I_C(R_C + R_E) = 22\ \text{V} - (0.867\ \text{mA})(10\ \text{kV} + 1.5\ \text{k}\Omega) = 22\ \text{V} - 9.97\ \text{V} = \mathbf{12.03\ V}$$

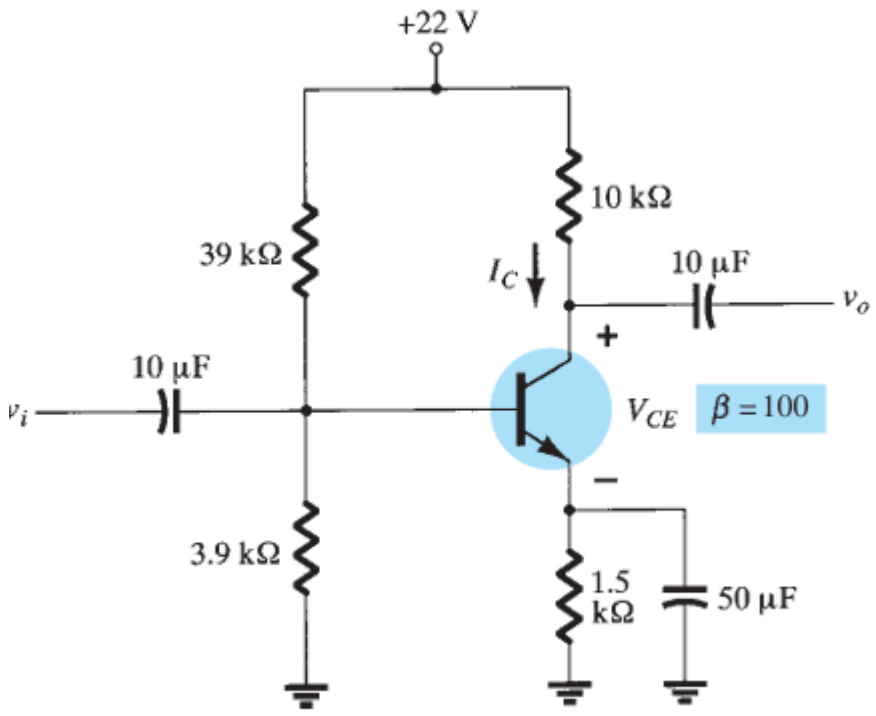
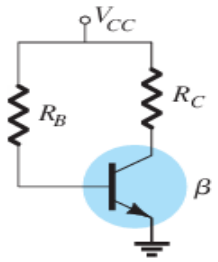
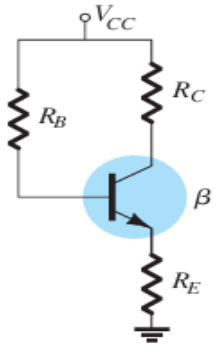
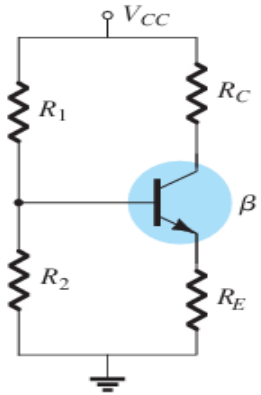


FIG. 4.35

Summary Table of biasing circuits

Type	Configuration	Pertinent Equations
Fixed-bias		$I_B = \frac{V_{CC} - V_{BE}}{R_B}$ $I_C = \beta I_B, I_E = (\beta + 1)I_B$ $V_{CE} = V_{CC} - I_C R_C$
Emitter-bias		$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)R_E}$ $I_C = \beta I_B, I_E = (\beta + 1)I_B$ $R_i = (\beta + 1)R_E$ $V_{CE} = V_{CC} - I_C(R_C + R_E)$
Voltage-divider bias		APPROXIMATE: $\beta R_E \geq 10R_2$ $V_B = \frac{R_2 V_{CC}}{R_1 + R_2}, V_E = V_B - V_{BE}$ $I_E = \frac{V_E}{R_E}, I_B = \frac{I_E}{\beta + 1}$ $V_{CE} = V_{CC} - I_C(R_C + R_E)$

DESIGN OPERATIONS

- The design process is one where a current and/or voltage may be specified and the elements required to establish the designated levels must be determined.
- This synthesis process requires a clear understanding of the characteristics of the device, the basic equations for the network, and a firm understanding of the basic laws of circuit analysis, such as Ohm's law, Kirchhoff's voltage law, and so on.
- EXAMPLE 4.21 Given the device characteristics of Fig. 4.59a , determine V_{CC}, R_B, and R_C for the fixed-bias configuration of Fig. 4.59b .

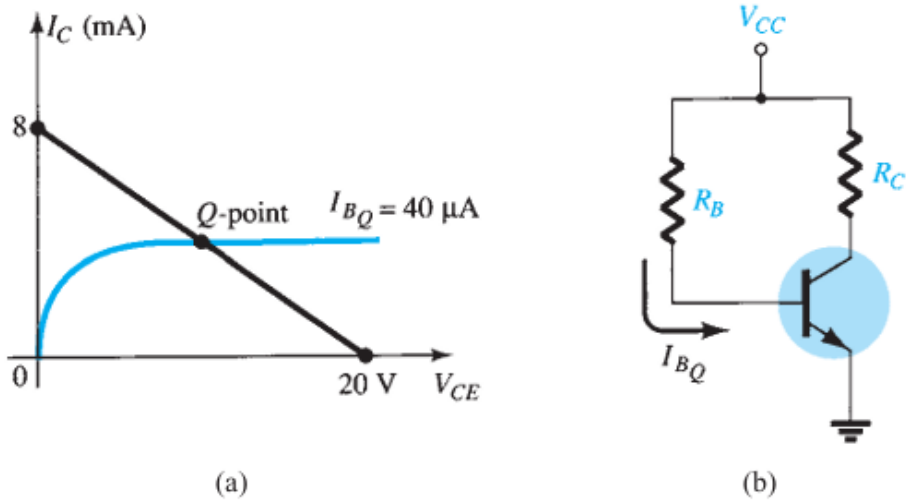


FIG. 4.59
Example 4.21.

DESIGN OPERATIONS

- EXAMPLE 4.21 Given the device characteristics of Fig. 4.59a , determine V_{CC}, R_B, and R_C for the fixed-bias configuration of Fig. 4.59b .

Solution: From the load line

R_C calculation

$$V_{CC} = \mathbf{20\ V}$$

$$I_C = \left.\frac{V_{CC}}{R_C}\right|_{V_{CE}=0\ \text{V}}$$

$$R_C = \frac{V_{CC}}{I_C} = \frac{20\ \text{V}}{8\ \text{mA}} = \mathbf{2.5\ k\Omega}$$

R_B calculation

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

$$R_B = \frac{V_{CC} - V_{BE}}{I_B}$$

$$= \frac{20\ \text{V} - 0.7\ \text{V}}{40\ \mu\text{A}} = \frac{19.3\ \text{V}}{40\ \mu\text{A}}$$

$$= \mathbf{482.5\ k\Omega}$$

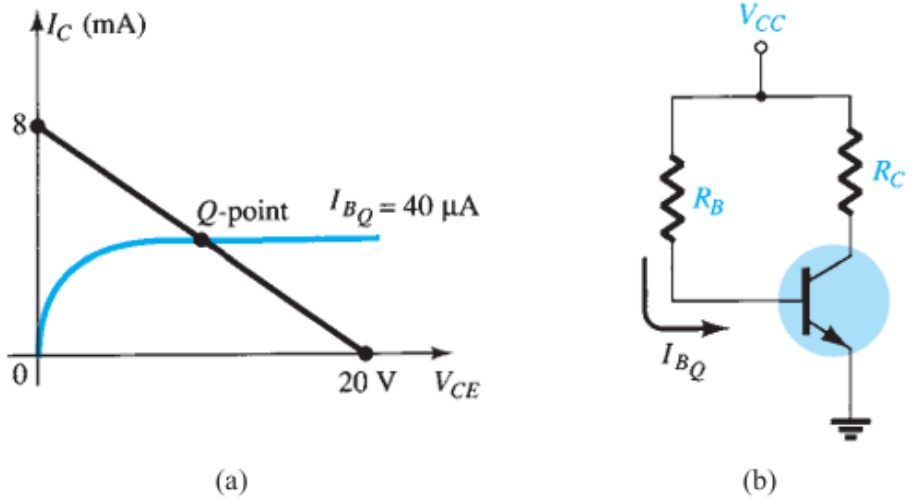


FIG. 4.59
Example 4.21.

Standard resistor values are

$$R_C = 2.4\ \text{k}\Omega$$

$$R_B = 470\ \text{k}\Omega$$

Using standard resistor values gives

$$I_B = 41.1\ \mu\text{A}$$

which is well within 5% of the value specified.

DESIGN OPERATIONS

- EXAMPLE 4.22 Given that I_{CQ} = 2 mA and V_{CEQ} = 10 V, determine R_1 and R_C for the network of Fig. 4.60

Solution:

R1 calculation

$$V_E = I_E R_E \cong I_C R_E$$
$$= (2\text{ mA})(1.2\text{ k}\Omega) = 2.4\text{ V}$$
$$V_B = V_{BE} + V_E = 0.7\text{ V} + 2.4\text{ V} = 3.1\text{ V}$$
$$V_B = \frac{R_2 V_{CC}}{R_1 + R_2} = 3.1\text{ V}$$
$$\frac{(18\text{ k}\Omega)(18\text{ V})}{R_1 + 18\text{ k}\Omega} = 3.1\text{ V}$$
$$324\text{ k}\Omega = 3.1R_1 + 55.8\text{ k}\Omega$$
$$3.1R_1 = 268.2\text{ k}\Omega$$
$$R_1 = \frac{268.2\text{ k}\Omega}{3.1} = \mathbf{86.52\text{ k}\Omega}$$

R_C Calculation

$$R_C = \frac{V_{R_C}}{I_C} = \frac{V_{CC} - V_C}{I_C}$$
$$V_C = V_{CE} + V_E = 10\text{ V} + 2.4\text{ V} = 12.4\text{ V}$$
$$R_C = \frac{18\text{ V} - 12.4\text{ V}}{2\text{ mA}}$$
$$= \mathbf{2.8\text{ k}\Omega}$$

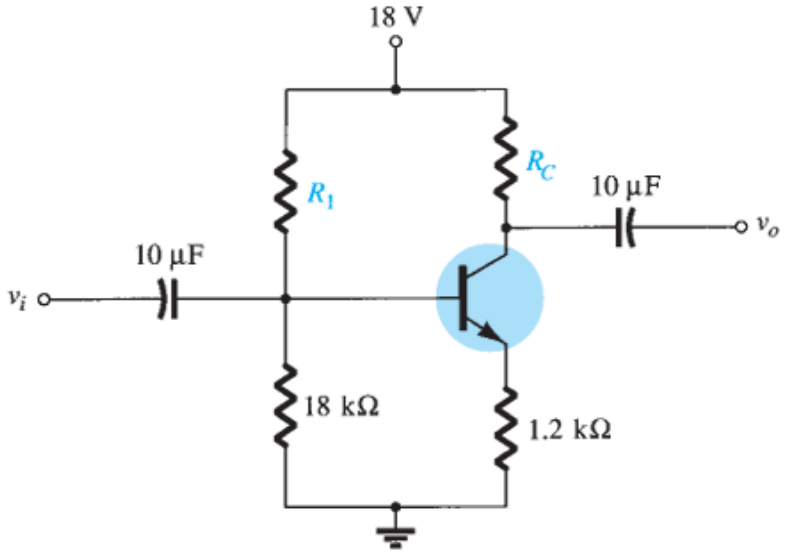


FIG. 4.60
Example 4.22.

DESIGN OPERATIONS

- EXAMPLE 4.23 The emitter-bias configuration of Fig. 4.61 has the following specifications: $I_{CQ} = 1/2 I_{sat}$, $I_{Csat} = 8$ mA, $V_C = 18$ V, and $\beta = 110$. Determine R_C , R_E , and R_B .

- **Solution:**

R_C calculation

$$I_{C_Q} = \tfrac{1}{2} I_{C_{sat}} = 4 \text{ mA}$$

$$R_C = \frac{V_{R_C}}{I_{C_Q}} = \frac{V_{CC} - V_C}{I_{C_Q}}$$

$$= \frac{28 \text{ V} - 18 \text{ V}}{4 \text{ mA}} = \mathbf{2.5\ k\Omega}$$

R_E calculation

$$I_{C_{sat}} = \frac{V_{CC}}{R_C + R_E}$$

$$R_C + R_E = \frac{V_{CC}}{I_{C_{sat}}} = \frac{28 \text{ V}}{8 \text{ mA}} = 3.5 \text{ k}\Omega$$

$$R_E = 3.5 \text{ k}\Omega - R_C$$

$$= 3.5 \text{ k}\Omega - 2.5 \text{ k}\Omega$$

$$= \mathbf{1\ k\Omega}$$

R_B calculation

$$I_{B_Q} = \frac{I_{C_Q}}{\beta} = \frac{4 \text{ mA}}{110} = 36.36\ \mu\text{A}$$

$$I_{B_Q} = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)R_E}$$

$$R_B + (\beta + 1)R_E = \frac{V_{CC} - V_{BE}}{I_{B_Q}}$$

$$R_B = \frac{V_{CC} - V_{BE}}{I_{B_Q}} - (\beta + 1)R_E$$

$$= \frac{28 \text{ V} - 0.7 \text{ V}}{36.36\ \mu\text{A}} - (111)(1 \text{ k}\Omega)$$

$$= \frac{27.3 \text{ V}}{36.36\ \mu\text{A}} - 111 \text{ k}\Omega$$

$$= \mathbf{639.8\ k\Omega}$$

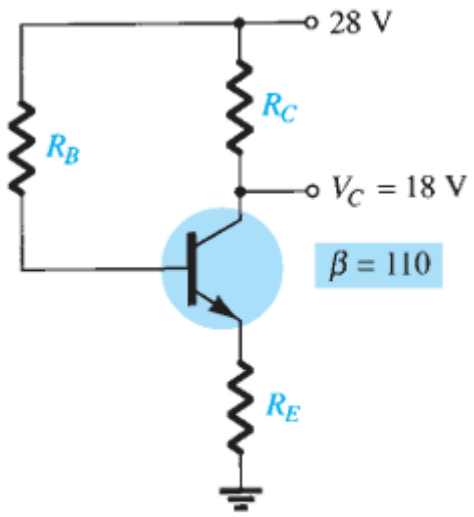


FIG. 4.61
Example 4.23.

For standard values,

$$R_C = 2.4 \text{ k}\Omega$$

$$R_E = 1 \text{ k}\Omega$$

$$R_B = 620 \text{ k}\Omega$$

DESIGN OPERATIONS

- EXAMPLE 4.24 Determine the resistor values for the network of Fig. 4.62 for the indicated operating point and supply voltage.

- **Solution:**

$$V_E = \tfrac{1}{10}V_{CC} = \tfrac{1}{10}(20\text{ V}) = 2\text{ V}$$

$$R_E = \frac{V_E}{I_E} \cong \frac{V_E}{I_C} = \frac{2\text{ V}}{2\text{ mA}} = \mathbf{1\ k\Omega}$$

$$R_C = \frac{V_{R_C}}{I_C} = \frac{V_{CC} - V_{CE} - V_E}{I_C} = \frac{20\text{ V} - 10\text{ V} - 2\text{ V}}{2\text{ mA}} = \frac{8\text{ V}}{2\text{ mA}}$$

$$= \mathbf{4\ k\Omega}$$

$$I_B = \frac{I_C}{\beta} = \frac{2\text{ mA}}{150} = 13.33\ \mu\text{A}$$

$$R_B = \frac{V_{R_B}}{I_B} = \frac{V_{CC} - V_{BE} - V_E}{I_B} = \frac{20\text{ V} - 0.7\text{ V} - 2\text{ V}}{13.33\ \mu\text{A}}$$

$$\cong \mathbf{1.3\ M\Omega}$$

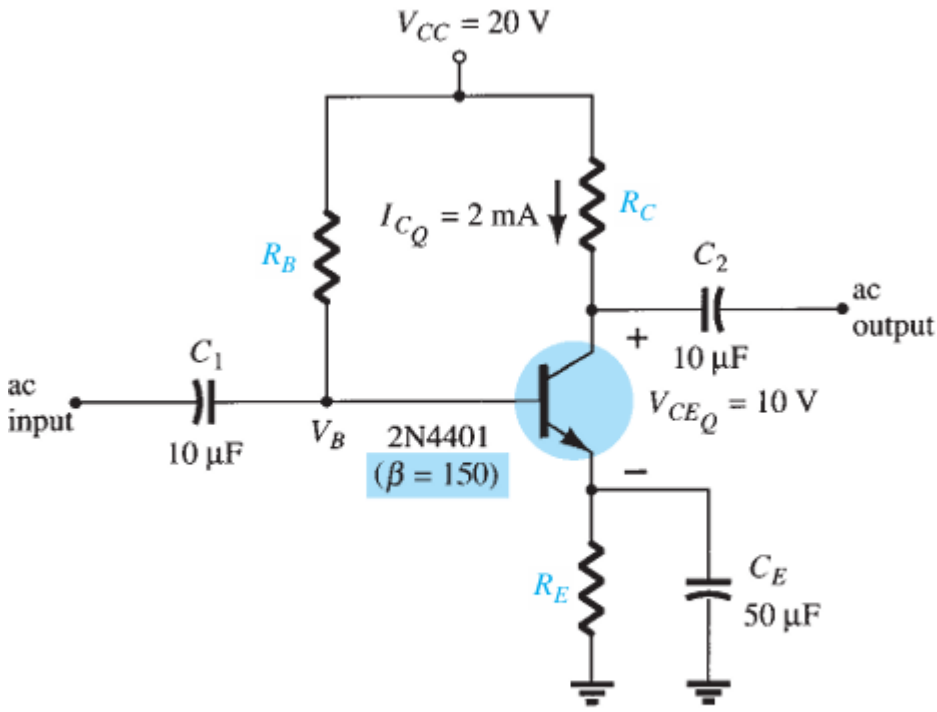


FIG. 4.62
Emitter-stabilized bias circuit for design consideration.

DESIGN OPERATIONS

- EXAMPLE 4.25 Determine the levels of RC, RE, R1, and R2 for the network of Fig. 4.63 for the operating point indicated.

- **Solution:**

$$V_E = \tfrac{1}{10}V_{CC} = \tfrac{1}{10}(20\text{ V}) = 2\text{ V}$$

$$R_E = \frac{V_E}{I_E} \cong \frac{V_E}{I_C} = \frac{2\text{ V}}{10\text{ mA}} = \mathbf{200\ \Omega}$$

$$R_C = \frac{V_{R_C}}{I_C} = \frac{V_{CC} - V_{CE} - V_E}{I_C} = \frac{20\text{ V} - 8\text{ V} - 2\text{ V}}{10\text{ mA}} = \frac{10\text{ V}}{10\text{ mA}}$$

$$= \mathbf{1\ k\Omega}$$

$$V_B = V_{BE} + V_E = 0.7\text{ V} + 2\text{ V} = 2.7\text{ V}$$

- **Using $\beta R_E \geq 10R_2$,**

R_2 calculation

$$R_2 \leq \tfrac{1}{10}\beta R_E$$

$$V_B = \frac{R_2}{R_1 + R_2}V_{CC}$$

$$R_2 \leq \tfrac{1}{10}(80)(0.2\text{ k}\Omega)$$

$$= \mathbf{1.6\ k\Omega}$$

R_1 calculation

$$V_B = 2.7\text{ V} = \frac{(1.6\text{ k}\Omega)(20\text{ V})}{R_1 + 1.6\text{ k}\Omega}$$

$$2.7R_1 + 4.32\text{ k}\Omega = 32\text{ k}\Omega$$

$$2.7R_1 = 27.68\text{ k}\Omega$$

$$R_1 = \mathbf{10.25\ k\Omega} \quad (\text{use } 10\text{ k}\Omega)$$

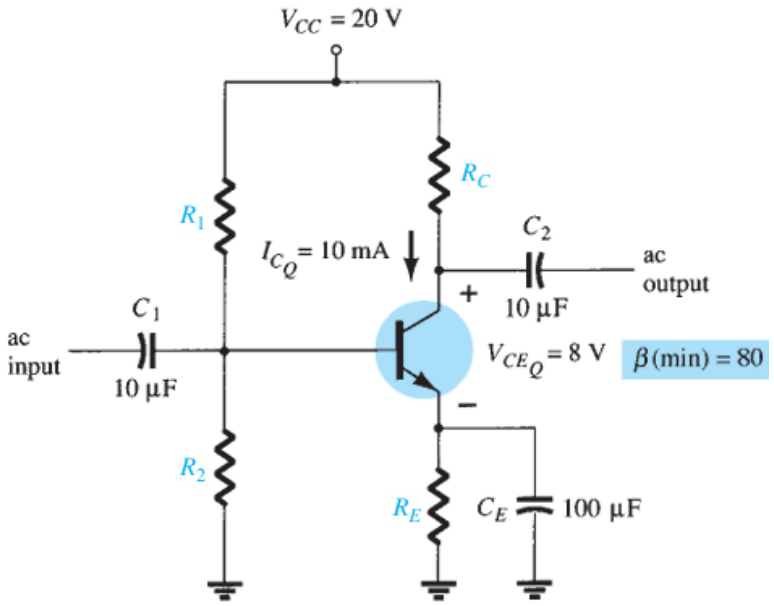


FIG. 4.63
Current-gain-stabilized circuit for design considerations.

Single stage CE Amplifier

- Fig shows a single stage CE amplifier. The different circuit elements and their functions are described as follows.

(i) Biasing circuit :

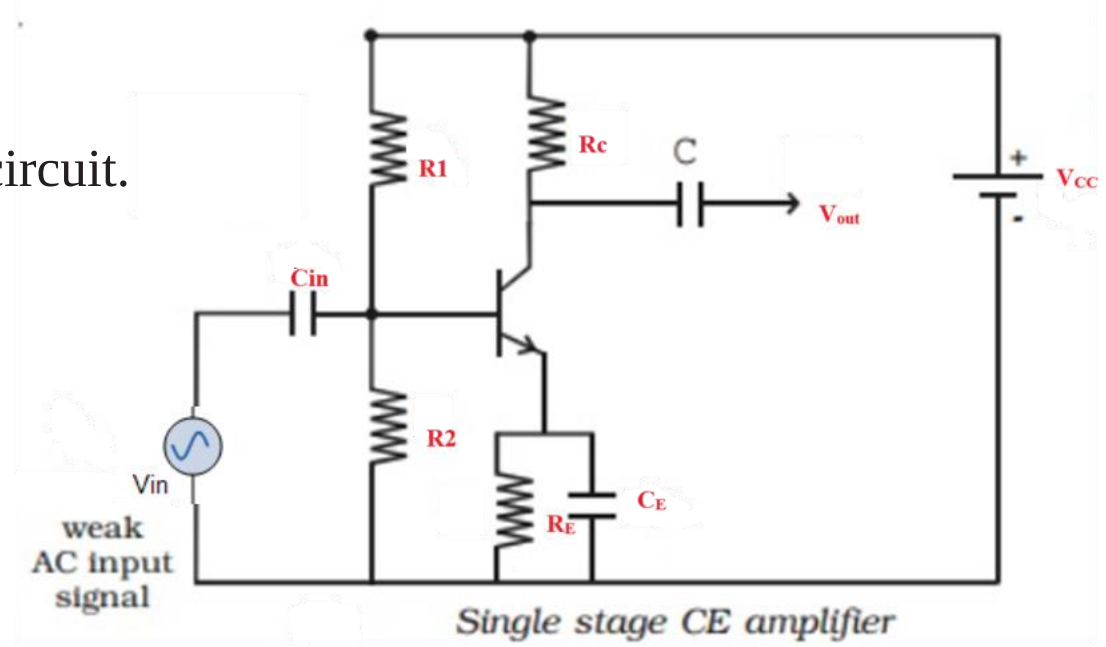
The resistances R_1, R_2 and R_E form the biasing and stabilization circuit.

(ii)Input capacitance C_{in} :

This is used to couple the signal to the base of the transistor.

If this is not used, the signal source resistance will come across R_2 and thus changes the bias condition of the transistor.

The capacitor C_{in} allows only a.c. signal to flow.



Single stage CE amplifier

(iii) Emitter bypass capacitor C_E :

This is connected in parallel with R_E to provide a low reactance path to the amplified a.c. signal. If it is not used, then amplified a.c. signal flowing through R_E will cause a voltage drop across it, thereby shifting the output voltage.

Single stage CE Amplifier

(iv)**Coupling capacitor C :**

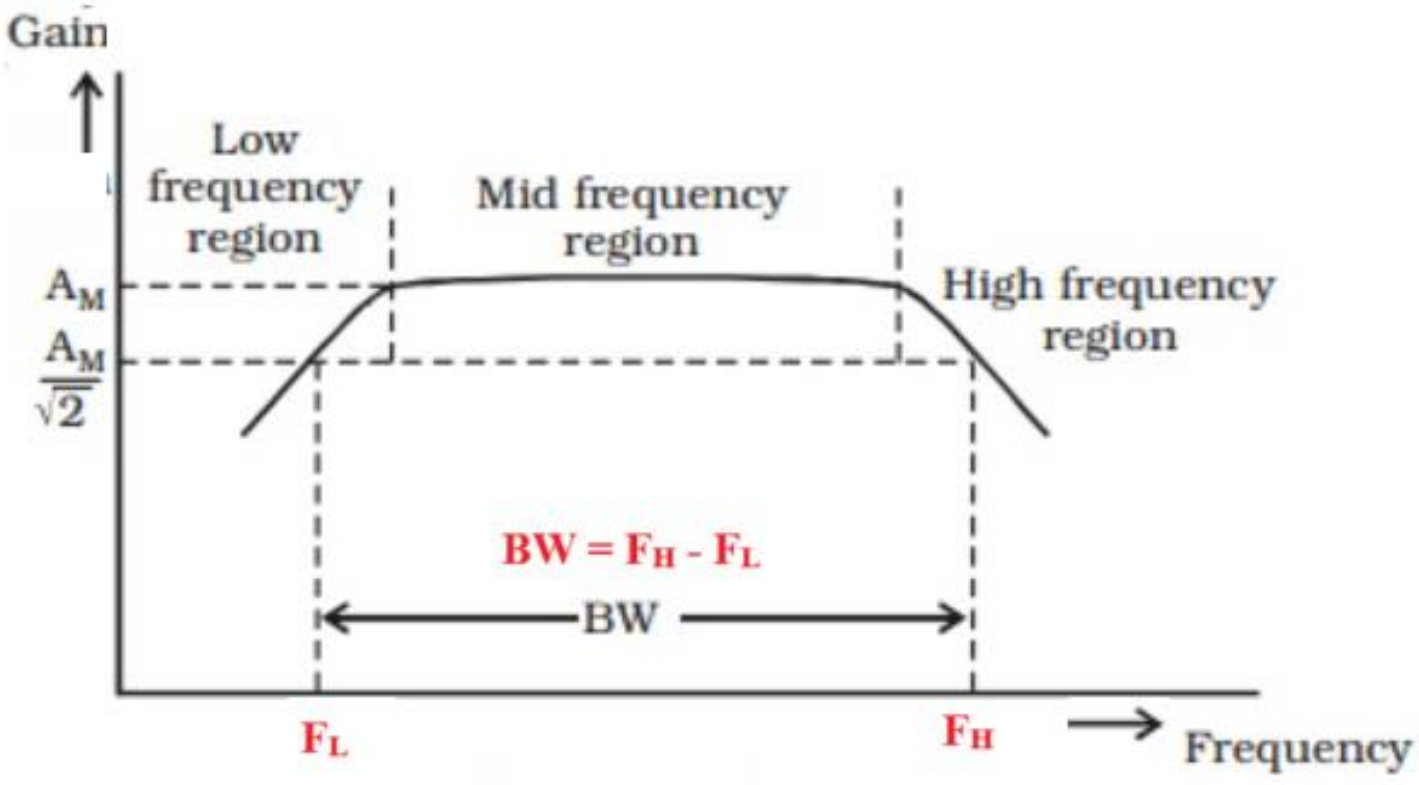
This is used to couple the amplified signal to the output device. This capacitor C allows only a.c. signal to flow.

(v) Working

- When a weak input a.c. signal is applied to the base of the transistor, a small base current flows**.**
- Due to transistor action, a much larger a.c. current flows through collector load R_C, a large voltage appears across R_C and hence at the output.
- Therefore, a weak signal applied to the base appears in amplified form at the collector of circuit.
- Voltage gain (A_v) of the amplifier is the ratio of the amplified output voltage to the input voltage.

Single stage CE Amplifier

(vi) ***Frequency response and bandwidth***



Frequency response curve

THANK YOU

Department of Electronics and Communication

ELECTRONIC PRINCIPLES AND DEVICES

Course Content

Department of Electronics and Communication.

ELECTRONIC PRINCIPLES AND DEVICES

Unit 3 –Transistors and Operational Amplifiers

Operational Amplifier - Introduction

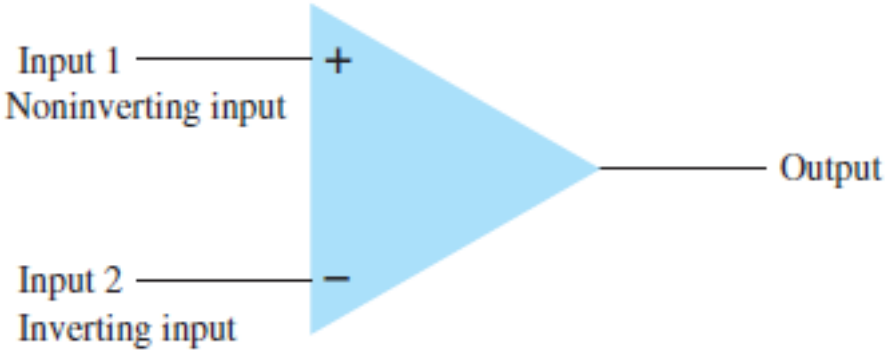


FIG. 10.1
Basic op-amp.

- Operational Amplifier or op-amp is a very high gain differential amplifier.
- It has very high input impedance. Ideally its value is infinity
- It has a low output impedance. Ideally its value is zero
- It finds applications in filters and oscillators

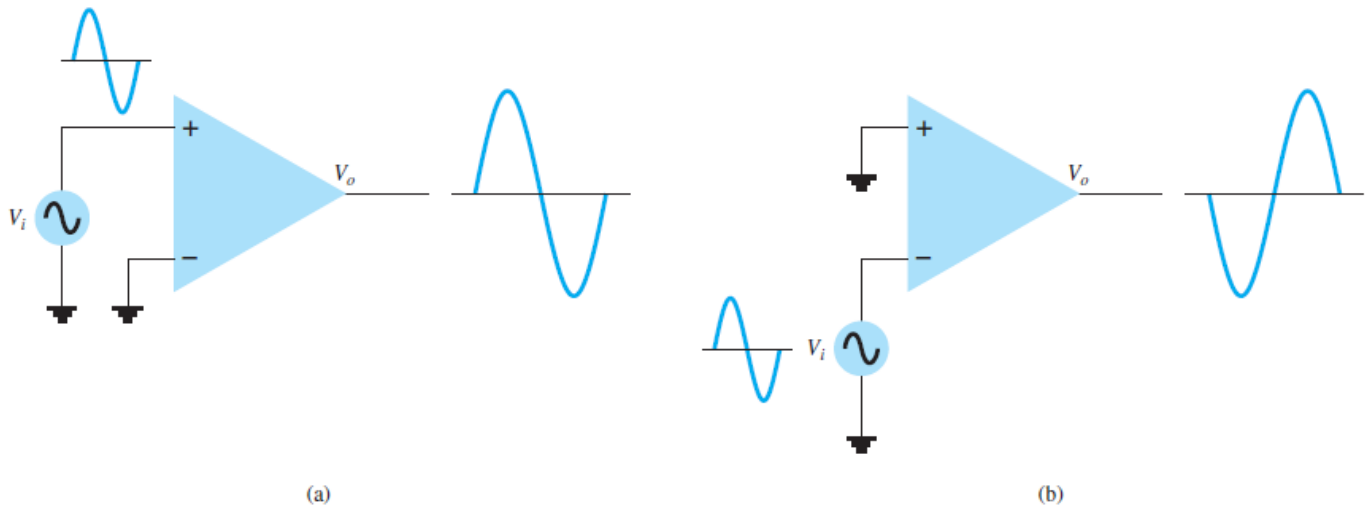


FIG. 10.2
Single-ended operation.

- **Single-ended input operation** results when the input signal is connected to one input with the other input connected to the ground.

- When the input signal is applied to the inverting input, the output is phase-shifted by 180^0

ELECTRONIC PRINCIPLES AND DEVICES

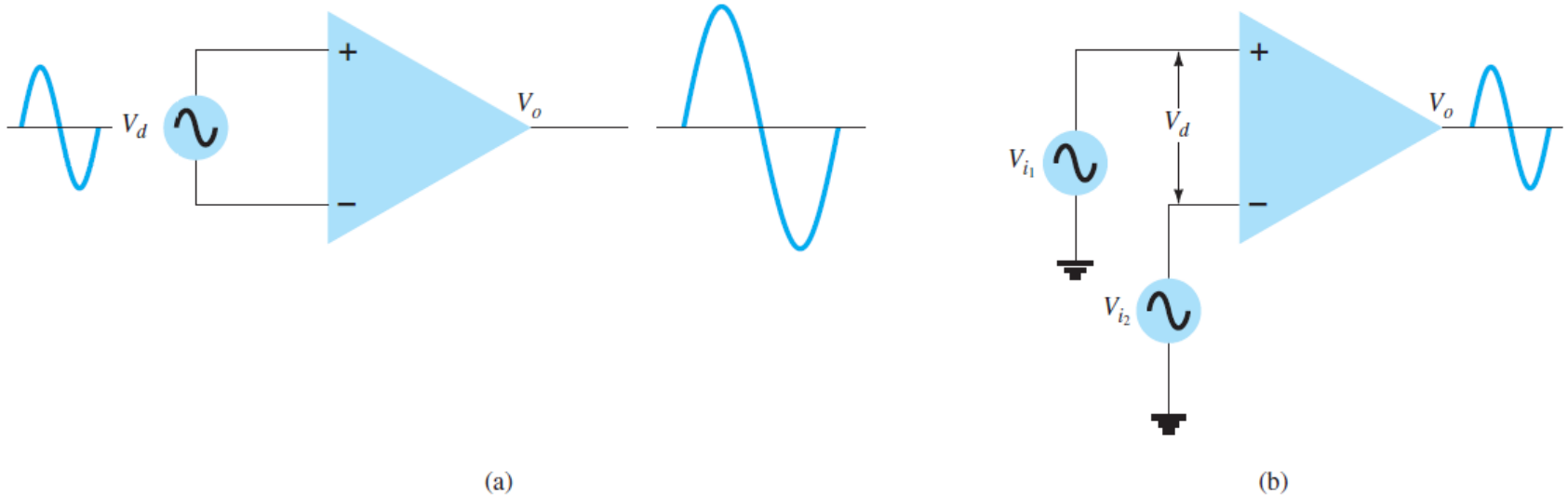


FIG. 10.3
Double-ended (differential) operation.

- Double-ended operation is one where an input, V_d is applied between the two input terminals (recall that neither input is at ground), with the resulting amplified output in phase with that applied between the inputs.
- Figure (b) shows the same action resulting when two separate signals are applied to the inputs, the difference signal being $V_{i1} - V_{i2}$

ELECTRONIC PRINCIPLES AND DEVICES

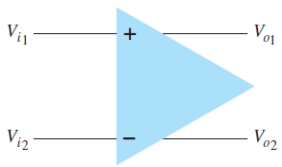


FIG. 10.4
Double-ended input with double-ended output.

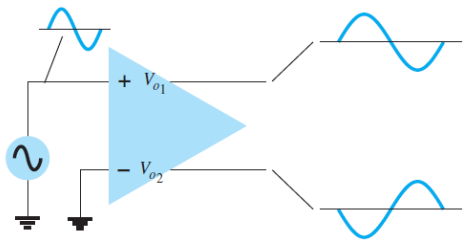


FIG. 10.5
Single-ended input with double-ended output.

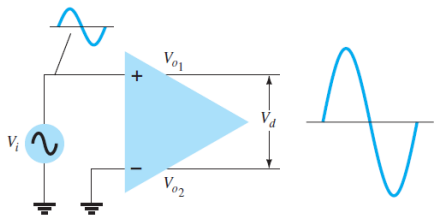


FIG. 10.6
Differential-output.

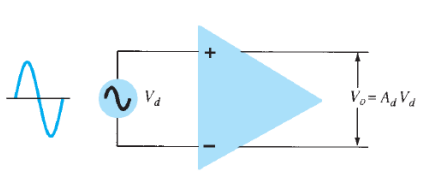


FIG. 10.7
Differential-input, differential-output operation.

- **Double Ended Output:** An input applied to either input will result in outputs from both output terminals, these outputs always being opposite in polarity.

- Figure 10.5 shows a single-ended input with a double-ended output. As shown, the signal applied to the plus input results in two amplified outputs of opposite polarity.

- Figure10.6 shows the same operation with a single output measured between output terminals This difference output signal is V_{o1}-V_{o2}. The difference output is also referred to as a *floating signal* since neither output terminal is the ground (reference) terminal.

- Figure 10.7 shows a differential input, differential output operation. The input is applied between the two input terminals, and the output is taken from between the two output terminals. This is a fully differential operation.

Common Mode Operation

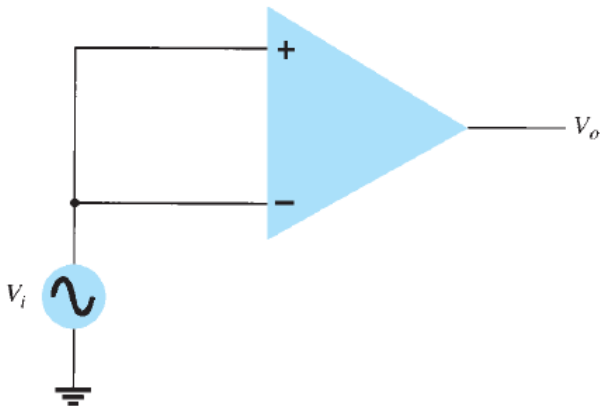


FIG. 10.8
Common-mode operation.

When the same input signal is applied to both inputs, common-mode operation results, as shown in Fig. Ideally, the two inputs are equally amplified, and since they result in opposite-polarity signals at the output, these signals cancel, resulting in 0-V output. Practically, a small output signal will result.

Basic Op-Amp

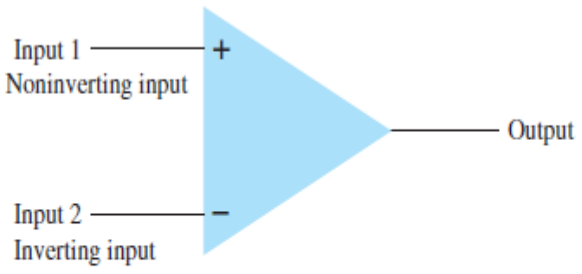
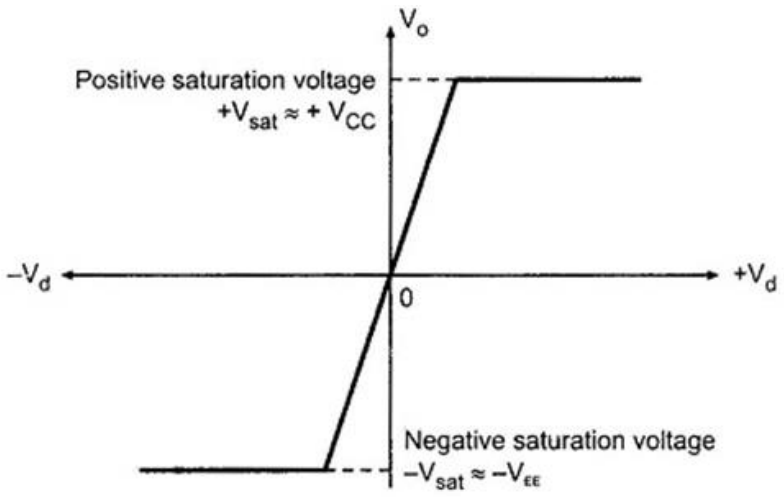


FIG. 10.1
Basic op-amp.

- **Op-Amp has two inputs as shown in the figure**
- **Input1=Noninverting input**
- **Input2= Inverting input**

Ideal Voltage Transfer Curve



Ideal voltage transfer curve

- V_d= Differential Voltage
- $+V_{sat}$ = +Ve Saturation Voltage
- $-V_{sat}$ = - Ve Saturation Voltage
- It rises linearly between $+V_{sat}$ and $-V_{sat}$

Op-Amp Parameters

Input Offset Voltage: It is the differential DC voltage that must be applied between the input terminals (inverting and non-inverting) of the op-amp to make the output offset voltage zero. Ideally its value is 0v. Its value is 1 mv to 6mv for IC 741.

Output offset voltage: This refers to the small DC voltage that appears at its output even when the input terminals are shorted together and no input signal is applied. This offset is caused by internal mismatches in the op-amp, such as differences in the transistor parameters or imbalances in the internal circuitry. Ideally its value is 0v.

Input Resistance: The **input resistance** of an op-amp refers to the effective resistance seen at its input terminals. It is generally measured in open-loop condition. Ideally its value is infinity. Its value is 2MΩ for IC 741 under open loop condition.

Output resistance: The **output resistance** of the op-amp is the resistance seen at the output terminal when the op-amp is configured in an open-loop condition. Ideally, its value is 0. Its value is 75Ω for IC 741.

Op-Amp Parameters

Gain Bandwidth: The frequency at which the gain drops by 3 dB is known as the cutoff frequency f_c of the Op-Amp. The unity-gain frequency f_1 and cutoff frequency are related by

$$f_1 = A_{VD} f_c$$

Unity-gain frequency may also be called the gain–bandwidth product of the op-amp. Ideally its value is infinity. Its value is 1MHz for IC741

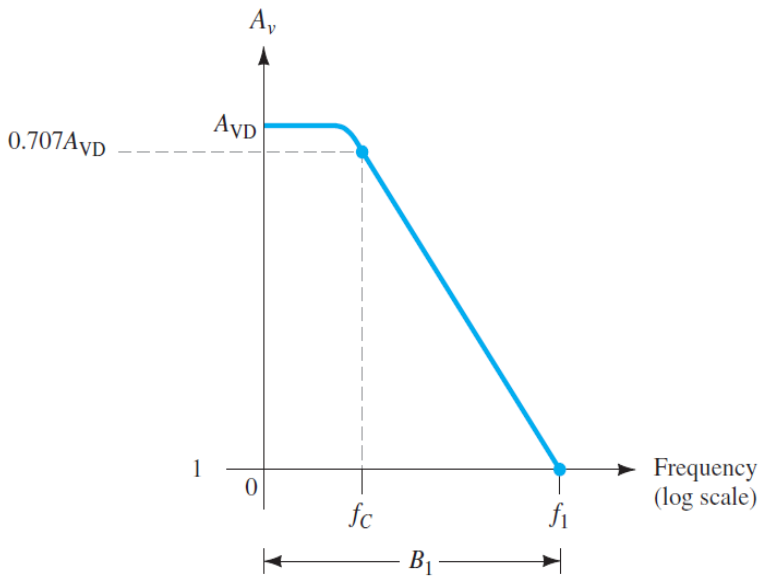


FIG. 10.47
Gain versus frequency plot.

Op-Amp Parameters

Slew rate: The maximum rate at which amplifier output can change in volts per microsecond is known as **Slew rate**. The slew rate provides a parameter specifying the maximum rate of change of the output voltage when driven by a large step-input signal. Ideal value of slew rate is infinity. It is 0.5 V/µs for IC741

$$\boxed{\mathrm{SR} = \frac{\Delta V_o}{\Delta t}\ \mathrm{V}/\mu\mathrm{s}} \quad \text{with } t \text{ in } \mu\mathrm{s}$$

Op-Amp Parameters

Common Mode Rejection Ratio: It is the ratio of differential gain to the common mode gain of the amplifier. Ideally, CMRR is infinity. Typically, its value is 90 dB for IC741.

$$CMRR = \frac{A_d}{A_c}$$

$$A_d = Differential\ gain\ of\ the\ amplifier$$

$$A_c = Common\ mode\ gain\ of\ the\ amplifier$$

The value of CMRR can also be expressed in logarithmic terms

$$CMRR(log) = 20log_{10}\left\{\frac{A_d}{A_c}\right\}\ dB$$

Negative feedback in Op-amp:

Op-amps are normally used with negative feedback for the following reasons:

1. The open-loop gain of the op-amp is very high. It is typically 2 x10^5 for IC 741. Such large gain is unsuitable for linear applications. Negative feedback decreases the gain and makes it suitable for linear applications such as an amplifier.
2. The open-loop gain is not stable and varies with temperature, supply voltage and frequency whereas the gain with feedback is stable.
3. The open-loop BW is very small making it unsuitable for any practical application. With negative BW increases.

Virtual Ground Concept

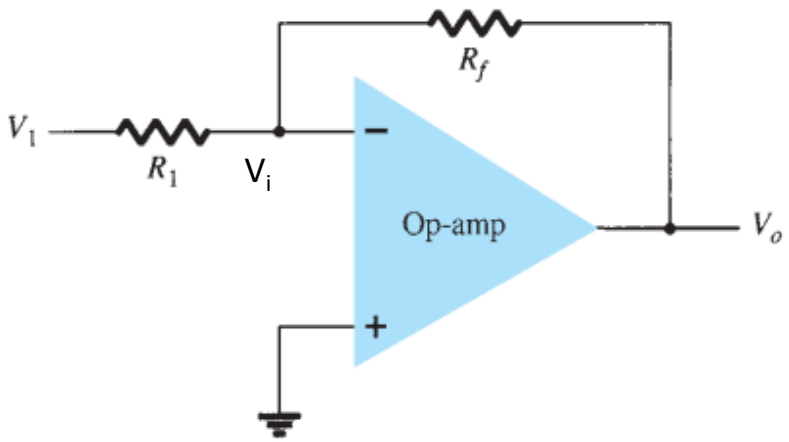


Fig. Basic Op-amp Connection

- The output voltage of an Op-amp is limited by the supply voltage V_1 as shown in the figure and the voltage gains are very high.
- For example, if V_o = -10 V and gain Av = 20,000, then the input voltage $V_i = -\frac{V0}{Av} = -\frac{10}{20{,}000}$ = 0.5 mV.
- If the circuit has an overall gain of 1, then value of V_1 is 10V.
- Compared to all other input and output voltages, the value of Vi is very small and can be considered as 0V.
- The fact that Vi ≈ 0V leads to the concept that at the amplifier input there exists a virtual short-circuit or virtual ground.

Virtual Ground Concept

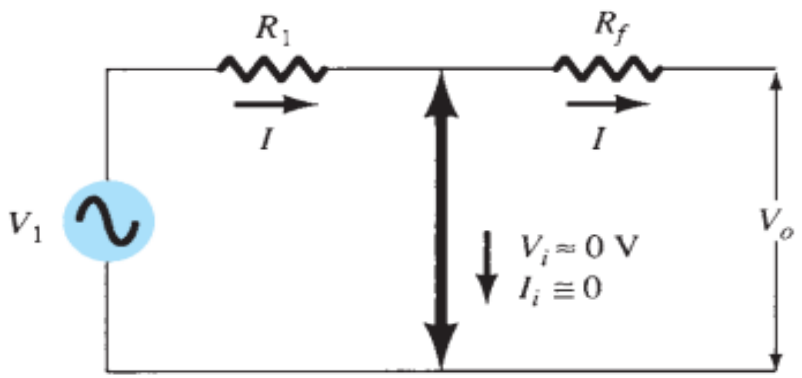
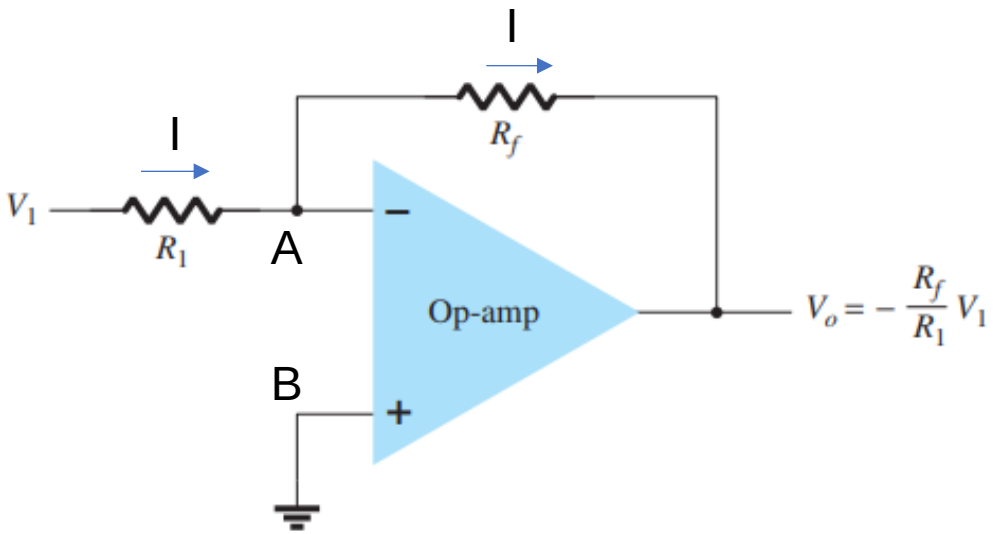


Fig. Virtual ground in Op-amp

- From above figure, Virtual short or Virtual ground implies that although the input voltage Vi is nearly 0V, there is no current through the amplifier input to ground.
- The heavy line in the figure is used to indicate that a short exists with Vi ≈ 0V.
- current will not flow through short and ground and flows only through resistors R1 and Rf as shown.
- Using the virtual ground concept, we can write equations for the current I as follows:
- $I = \frac{V1}{R1} = -\frac{V0}{Rf}$

Therefore, $\frac{V0}{V1} = -\frac{Rf}{R1}$

1. INVERTING AMPLIFIER:



$V_A = V_B = 0$(Virtual ground)

At Input, $I = (V_1 - V_A)/R_1 = V_1/R_1$----(1)

At Output, $I = (V_A - V_O)/R_f = -(V_O/R_f)$—(2)

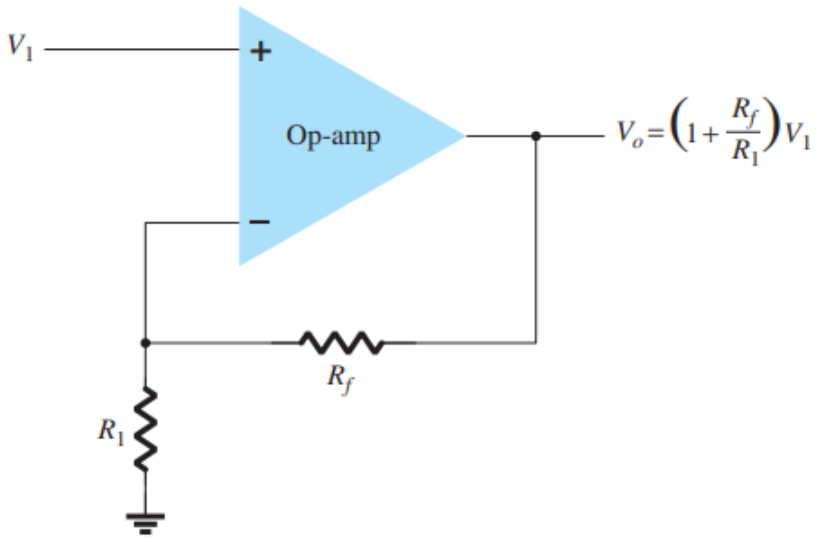
Equating 1 and 2

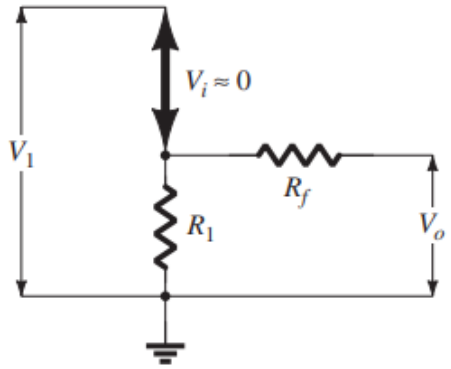
Output Voltage $V_O = -(R_f/R_1)*V_1$

Where Gain is $-(R_f/R_1)$

- Input is given to inverting terminal of the amplifier.
- Inverting amplifier is the most widely used constant-gain amplifier circuit.
- The output is obtained by multiplying the input by a fixed or constant gain, set by the input resistor R1and feedback resistor Rf and output is being inverted from the input.
- Output Voltage of Inverting amplifier is $V_0 = -\frac{Rf}{R1} * V_1$ (from virtual ground concept)

2. NONINVERTING AMPLIFIER:





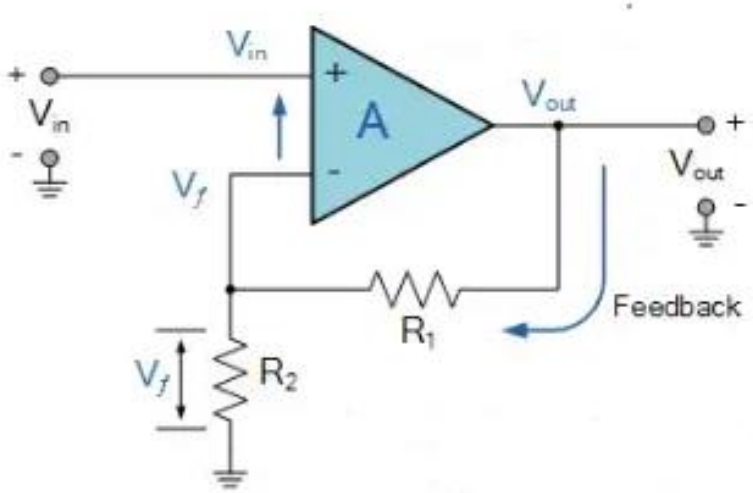
- Input is given to noninverting terminal of the op-amp.
- voltage across R_1 is V_1 (since V_i = 0V) and is equal to the output voltage, through a voltage divider of R1 and Rf and is given by

$$V_1 = \frac{R_1}{R_1 + R_f} V_o$$

or

$$\boxed{\frac{V_o}{V_1} = \frac{R_1 + R_f}{R_1} = 1 + \frac{R_f}{R_1}}$$

Ideal OP-Amp Negative Feedback



$$Closed\ loop\ Gain = \frac{V_{out}}{V_{in}} = 1 + \frac{R_1}{R_2}$$

$$Feed\ back\ \beta = \frac{V_f}{V_{out}} = \frac{R_2}{R_2 + R_2}$$

3. UNITY FOLLOWER OR VOLTAGE FOLLOWER:

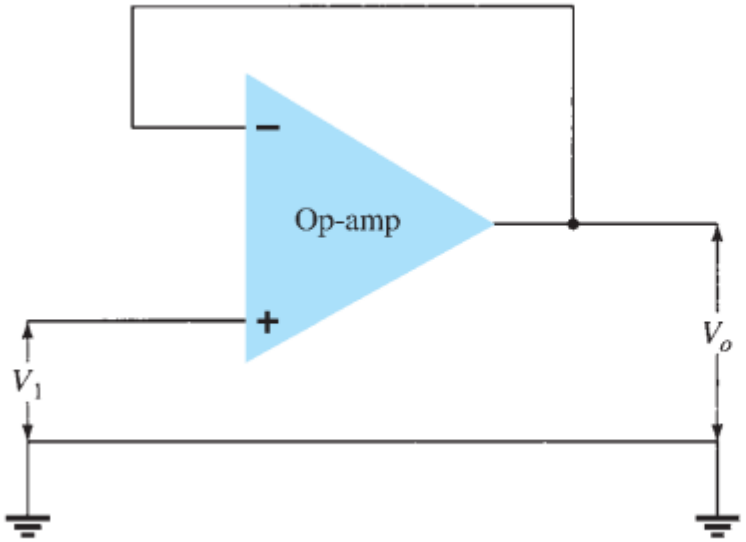


Fig a

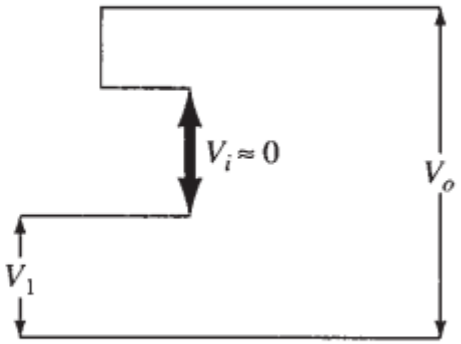


Fig b

- The unity-follower circuit provides a gain of unity with no polarity or phase reversal as shown in fig a.
- From the equivalent circuit as in fig b, $V_o = V_1$.
- It has a very high input resistance and a very low output resistance. It is used as a buffer circuit for impedance matching purposes.

4. SUMMING AMPLIFIER:

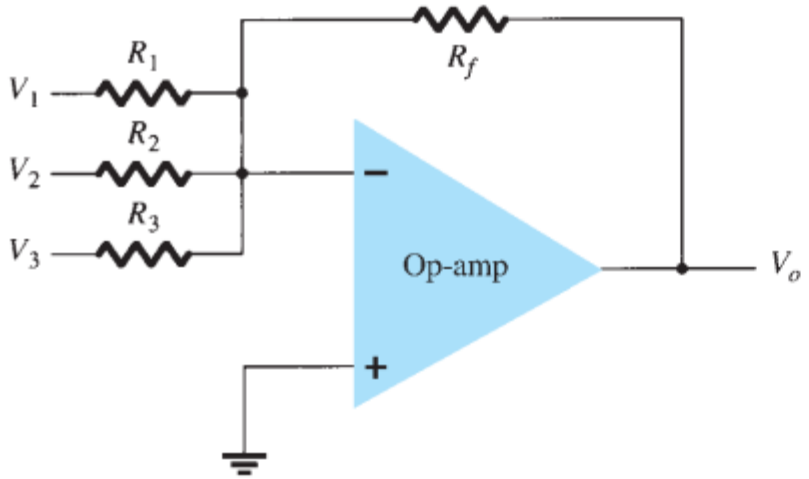


Fig a

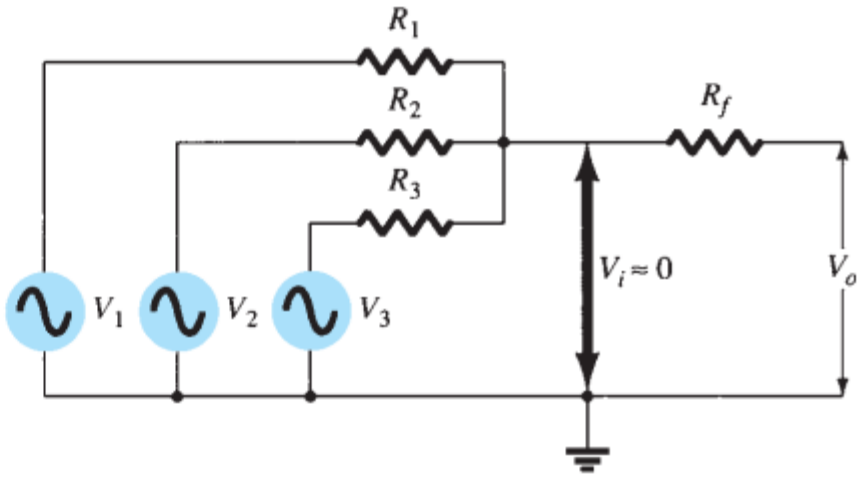
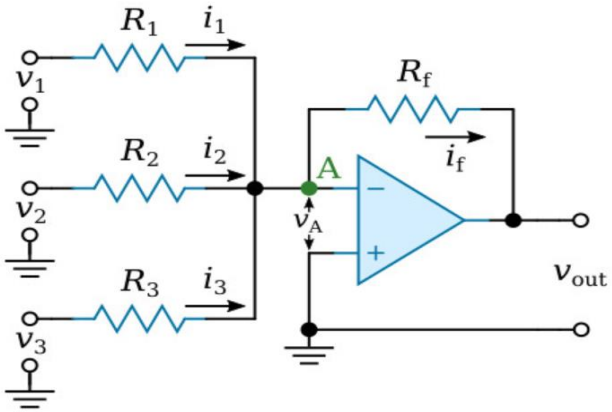


Fig b

- Above figure shows a three-input inverting summing amplifier circuit, which algebraically sums(adds) three voltages, each multiplied by a constant-gain(through resistors).
- If more inputs are used, they each add an additional component to the output.

OUTPUT OF A SUMMING AMPLIFIER:



Applying KCL at node A,

$$i_1 + i_2 + i_3 = i_f \qquad \text{---(1)}$$

Where,

$$i_1 = \frac{v_1 - v_A}{R_1} \qquad i_3 = \frac{v_3 - v_A}{R_3}$$

$$i_2 = \frac{v_2 - v_A}{R_2} \qquad i_f = \frac{v_A - v_{out}}{R_f} \qquad \text{----(2)}$$

Substituting eq (2) in (1) and considering $V_A = 0$(Virtual ground),

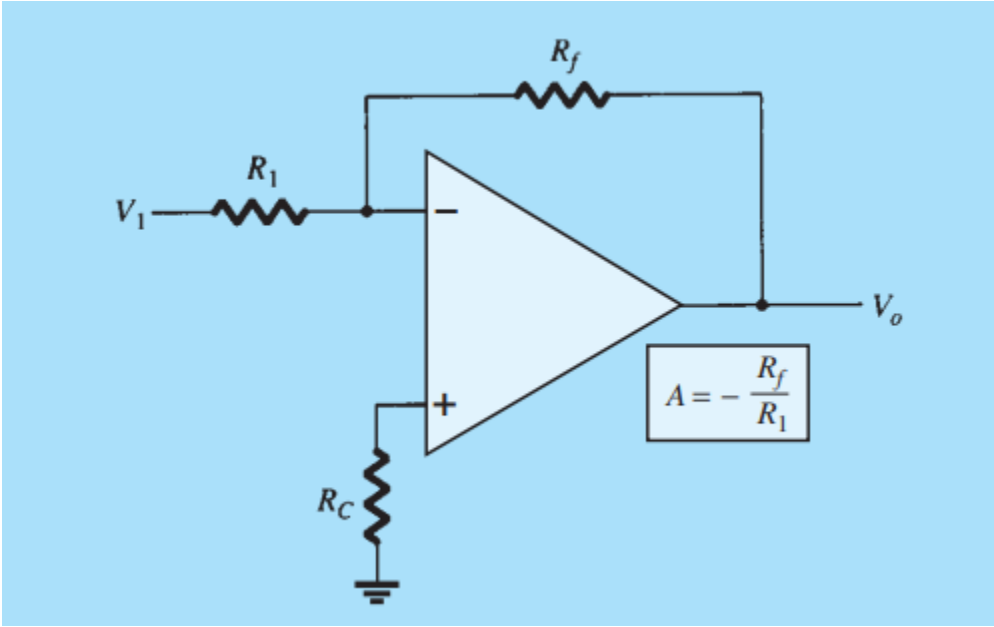
$$\frac{v_1}{R_1} + \frac{v_2}{R_2} + \frac{v_3}{R_3} = \frac{-v_{out}}{R_f}$$

or

$$v_{out} = -R_f\left(\frac{v_1}{R_1} + \frac{v_2}{R_2} + \frac{v_3}{R_3}\right)$$

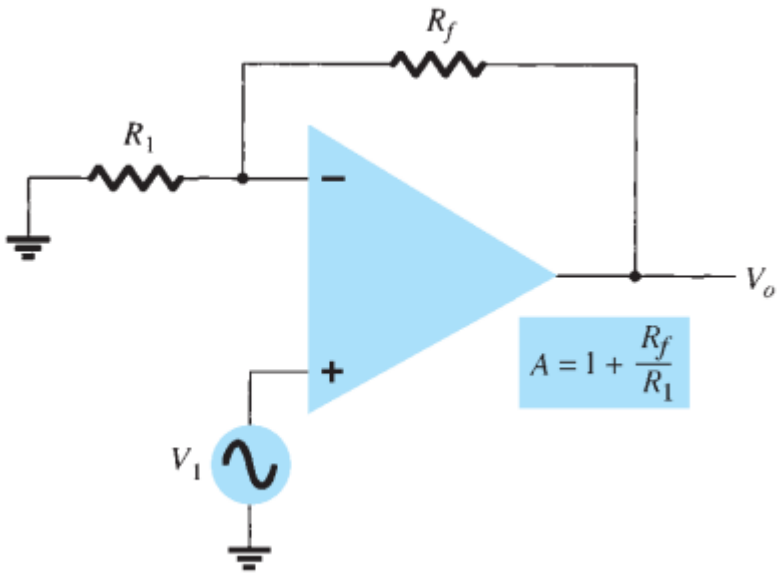
5. CONSTANT GAIN/FIXED GAIN AMPLIFIER:

a. Inverting Constant gain Multiplier: Provides a precise gain of $A = -\frac{R_f}{R_1}$

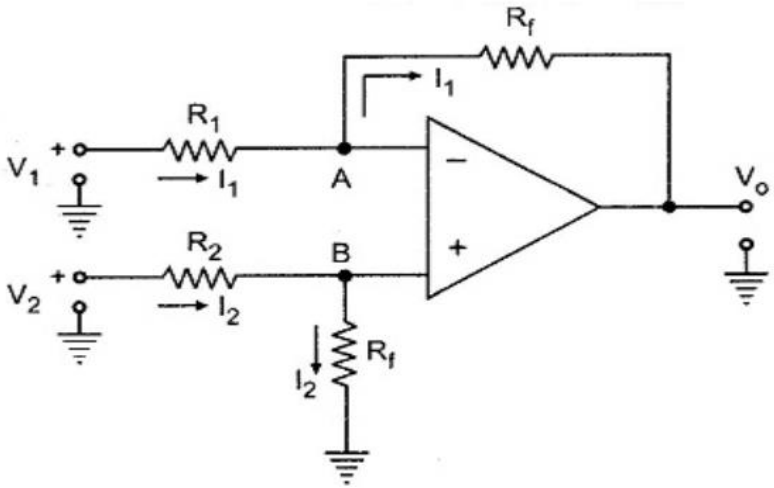


5. CONSTANT GAIN/FIXED AMPLIFIER:

b. Non-Inverting Constant gain Multiplier: Provides a precise gain of $A = 1 + \frac{R_f}{R_1}$



6. VOLTAGE SUBTRACTION:



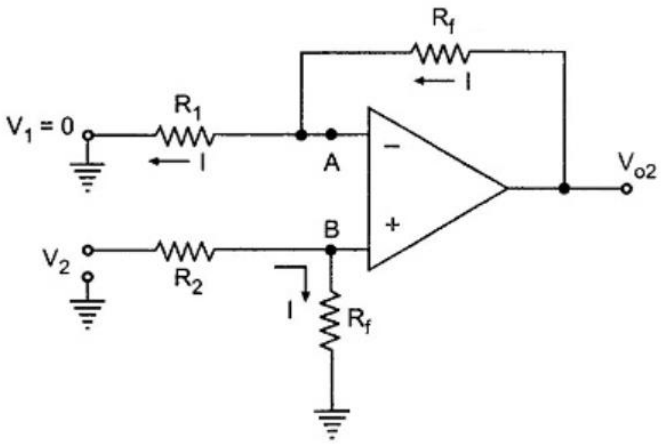
- Superposition principle is used to find the relation between output and input.
- Let V_{o1} be the output, with input V_1, assuming V_2 to be zero. And V_{o2} be the output, with input V_2 , assuming V_1 to be zero.

- With V_2 zero, the circuit acts as an inverting amplifier and the output equation is

$$V_{o1} = -\frac{R_f}{R_1} V_1 \quad \text{------(1)}$$

Practical Op-amp Circuits

While with V_1 as zero, the circuit reduces to as shown.



Let potential of node B be V_B. The potential of node A is same as B i.e. $V_A = V_B$ (Virtual short). Applying voltage divider rule to the input V_2 loop,

$$V_B = \frac{R_f}{R_2 + R_f} V_2 \quad \text{-----(2)}$$

$$I = \frac{V_A}{R_1} = \frac{V_B}{R_1} \quad \text{------(3)}$$

$$I = \frac{V_{o2} - V_A}{R_f} = \frac{V_{o2} - V_B}{R_f} \quad \text{------(4)}$$

Equating the equations (3) and (4),

Practical Op-amp Circuits

$$\frac{V_B}{R_1} = \frac{V_{o2} - V_B}{R_f}$$

$$V_{o2} = \frac{R_1 + R_f}{R_1} V_B$$

$$V_{o2} = \left[1 + \frac{R_f}{R_1}\right] V_B \qquad \text{-----(5)}$$

Substituting V_B from (2) in (5) we get,

$$V_{o2} = \left[1 + \frac{R_f}{R_1}\right]\left[\frac{R_f}{R_2 + R_f}\right] V_2$$

Hence using Superposition principle,

$$V_o = V_{o1} + V_{o2}$$

$$= -\frac{R_f}{R_1} V_1 + \left[1 + \frac{R_f}{R_1}\right]\left[\frac{R_f}{R_2 + R_f}\right] V_2$$

Practical Op-amp Circuits

If $R_1 = R_2$,

$$V_o = -\frac{R_f}{R_1} V_1 + \left[1 + \frac{R_f}{R_1}\right]\left[\frac{R_f}{R_1 + R_f}\right] V_2$$

$$= -\frac{R_f}{R_1} V_1 + \frac{R_f}{R_1} V_2$$

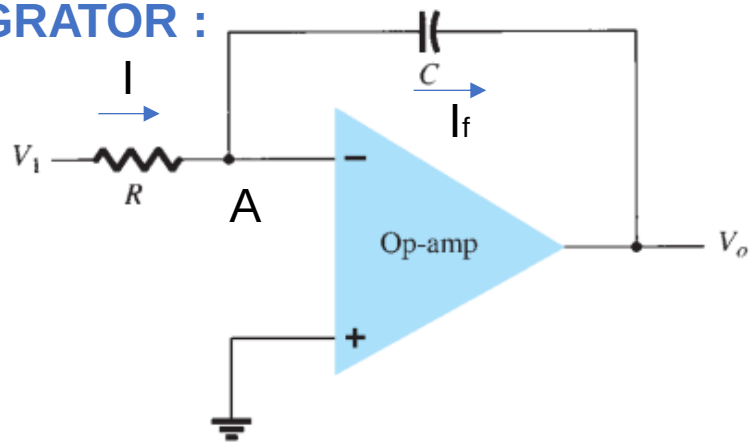
$$V_o = +\frac{R_f}{R_1}(V_2 - V_1)$$

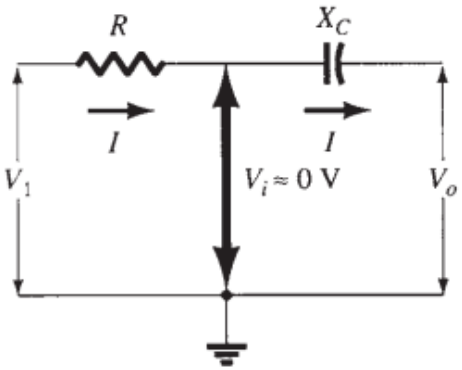
- The output voltage is proportional to the difference between the two input voltages. Thus it acts as a Subtractor using Op Amp circuit or difference amplifier.

If $R_1 = R_2 = R_f$ is selected, then $V_o = V_2 - V_1$

Practical Op-amp Circuits

7. INTEGRATOR :





Applying KCL at node A, $I=I_f$ ----(1)

Where $I= (V_1-V_A)/R$ and $I_f = C*d(V_A-V_0)/dt$ ----(2)

($V_A=0$ due to virtual ground property)

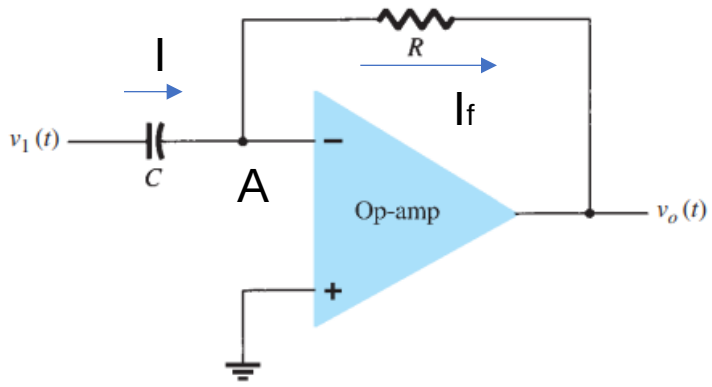
Substituting 2 in 1,

$$\frac{V_1 - 0}{R} = C\frac{d(0 - V_o)}{dt}$$ or $$\frac{dV_o}{dt} = -\frac{1}{RC}V_1$$

$$V_{out}(t) = -\frac{1}{RC}\int_0^t V_{in}(t)\,dt$$ Where Scale factor is $1/RC$

- Integrator has capacitor as a feedback element.
- Integration is summing the area under a waveform or a curve over a period of time.
- If a fixed voltage is applied in the form of a square wave as an input to an integrator circuit, the output voltage grows over a period of time, resulting in a ramp voltage.

8. DIFFERENTIATOR :



- A differentiator op amp circuit produces an output signal proportional to the input signal's rate of change.
- Involves an inverting amplifier with a capacitor at the input terminal.

Applying KCL at node A, $I=I_f$ ----(1)

Where $I= C*d(V_i-V_A)/dt$ and $I_f = (V_A—V_0)/R$----(2)

($V_A=0$ due to virtual ground property)

Substituting 2 in 1,

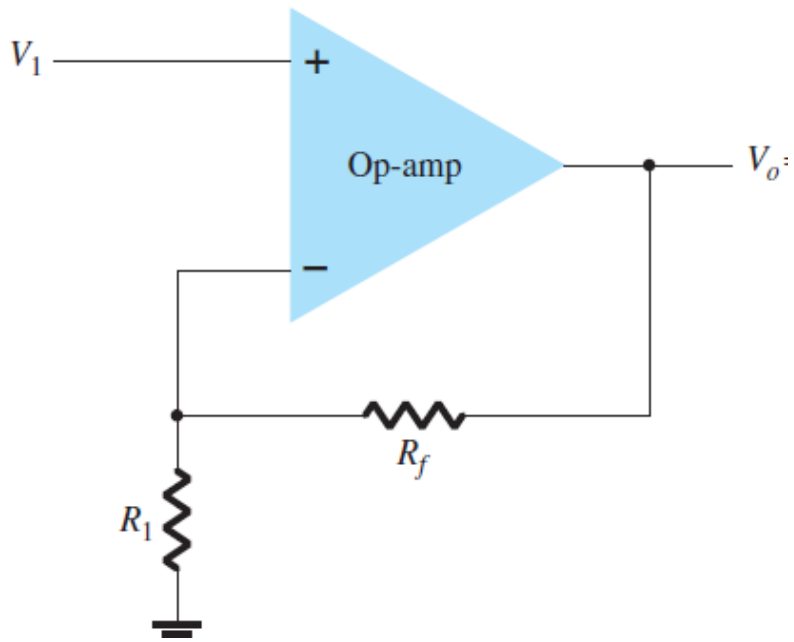
$$C\frac{dv_i}{dt} = -\frac{v_0}{R}$$

$$v_0 = -RC\frac{dv_i}{dt}$$

Where the scale factor is -RC

Numerical-1

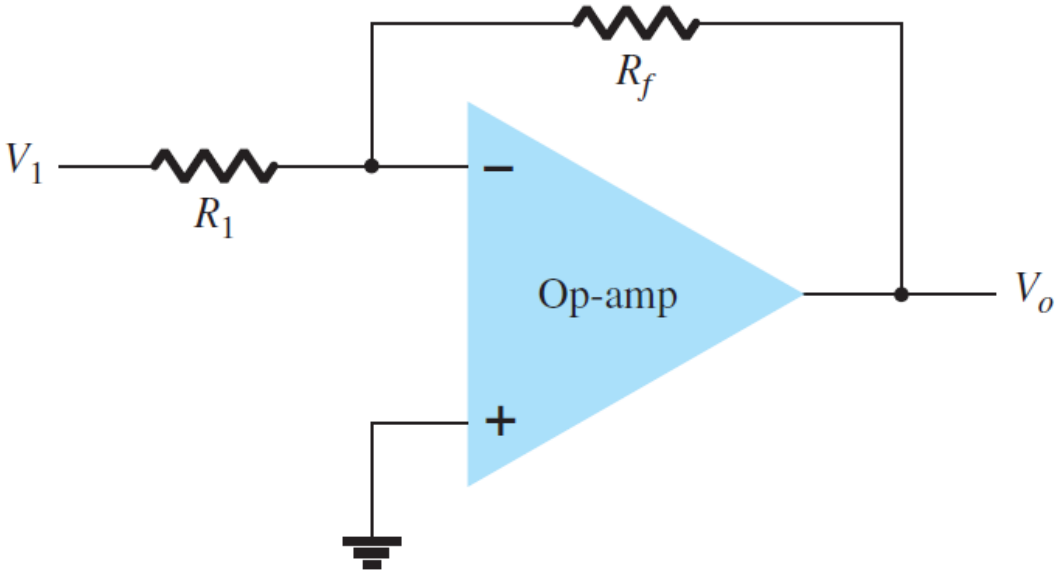
Calculate the output voltage of a noninverting amplifier shown in figure



$$V_o = \left(1 + \frac{R_f}{R_1}\right)V_1 = \left(1 + \frac{500\ \text{k}\Omega}{100\ \text{k}\Omega}\right)(2\ \text{V}) = 6(2\ \text{V}) = \mathbf{+12\ V}$$

Numerical-2

If the circuit of the figure has R_1=100K Ohms and R_f=500K Ohms, What is the output voltage if V_1= 2V?



$$V_o = -\frac{R_f}{R_1}V_1 = -\frac{500\ \text{k}\Omega}{100\ \text{k}\Omega}(2\ \text{V}) = \mathbf{-10\ V}$$

Numerical-3

3. What is the Output voltage in the Circuit shown in Figure

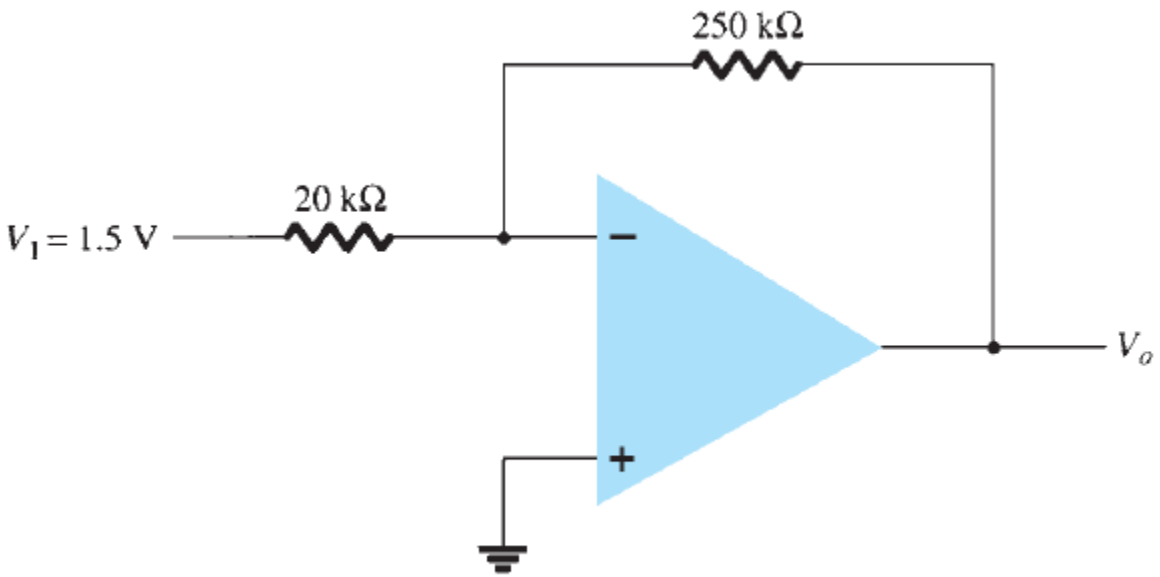


FIG. 10.62

$$V_o = -\frac{R_F}{R_1}V_1 = -\frac{250\ \text{k}\Omega}{20\ \text{k}\Omega}(1.5\ \text{V}) = \mathbf{-18.75\ V}$$

Numerical-4

What is the range of voltage gain adjustment in the circuit of the figure shown

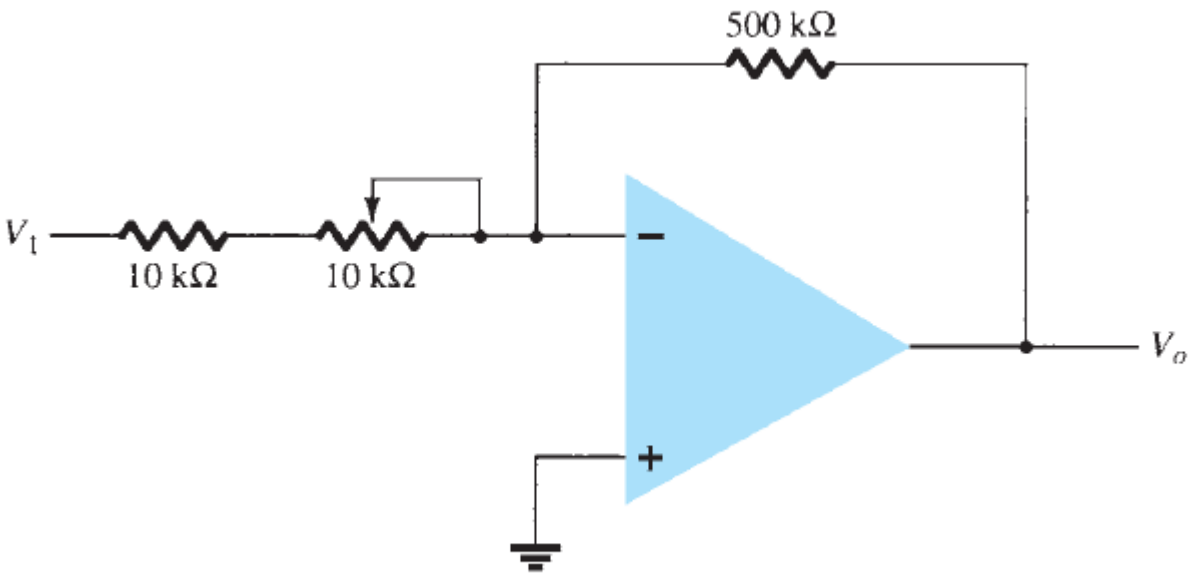


FIG. 10.63

$$A_v = \frac{V_o}{V_i} = -\frac{R_F}{R_1}$$

For $R_1 = 10\ \text{k}\Omega$:

$$A_v = -\frac{500\ \text{k}\Omega}{10\ \text{k}\Omega} = \mathbf{-50}$$

For $R_1 = 20\ \text{k}\Omega$:

$$A_v = -\frac{500\ \text{k}\Omega}{20\ \text{k}\Omega} = \mathbf{-25}$$

Numerical-5

What is the input voltage that results in an output of 2V in circuit shown in Figure

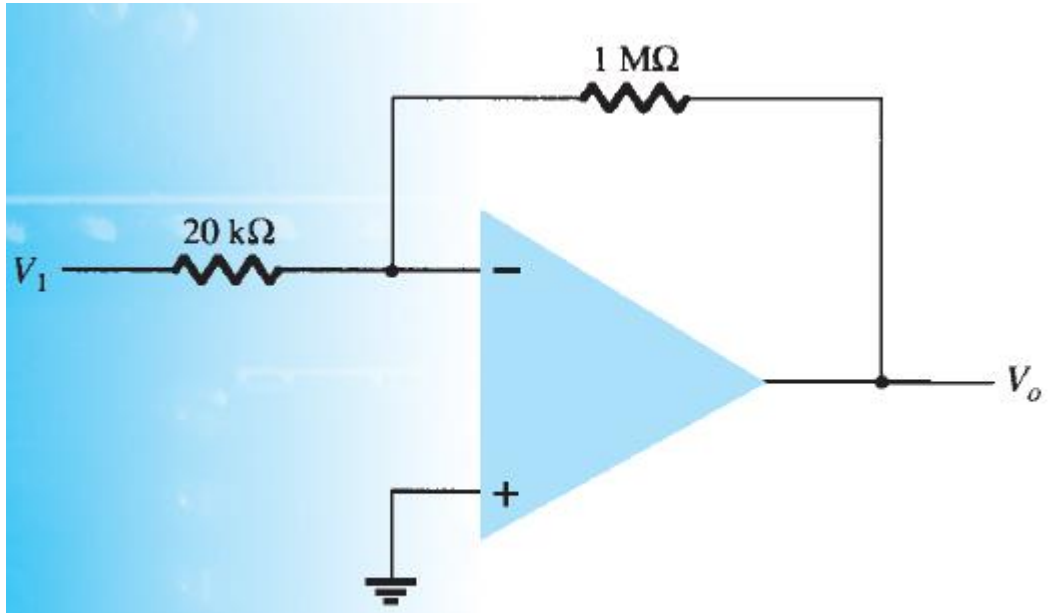


FIG. 10.64

$$V_o = -\frac{R_f}{R_1}V_1 = -\left(\frac{1\ \text{M}\Omega}{20\ \text{k}\Omega}\right)V_1 = 2\ \text{V}$$

$$V_1 = \frac{2\ \text{V}}{-50} = \mathbf{-40\ mV}$$

Numerical-6

What is the range of output voltage in the circuit shown in the figure if the input can vary from 0.1 to 0.5 V?

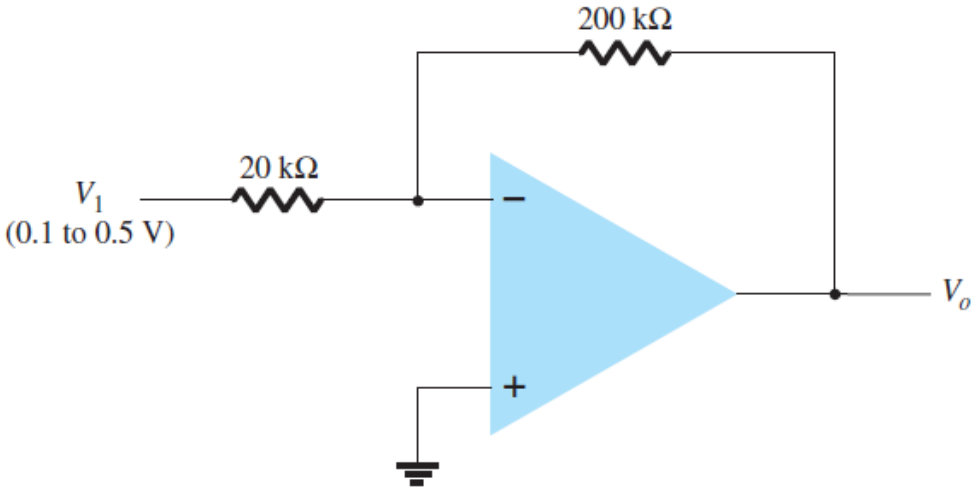


FIG. 10.65

$$V_o = -\frac{R_F}{R_1}V_1 = -\frac{200\ \text{k}\Omega}{20\ \text{k}\Omega}V_1 = -10\ V_1$$

For $V_1 = 0.1$ V:

$V_o = -10(0.1\ \text{V}) = \mathbf{-1\ V}$

For $V_1 = 0.5$ V:

$V_o = -10(0.5\ \text{V}) = \mathbf{-5\ V}$

V_o ranges from **−1 V to −5 V**

Numerical-7

What is the range of output voltage developed in the circuit shown in the figure

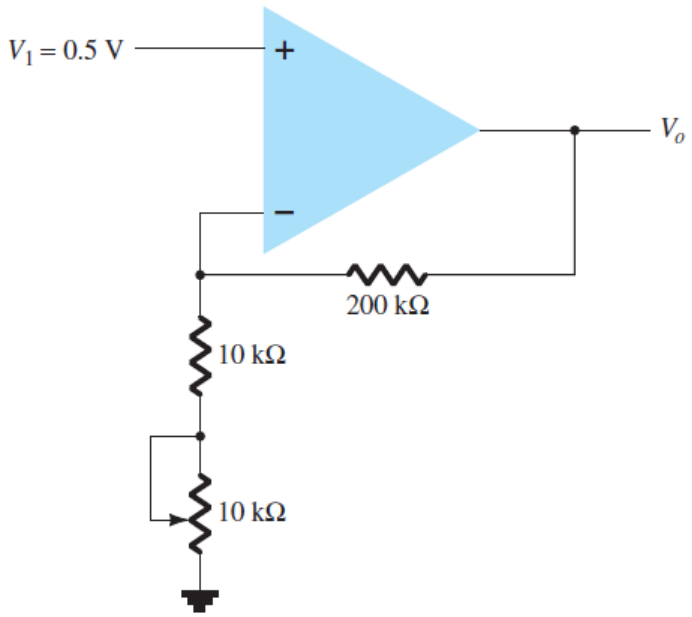


FIG. 10.67
Problem 7.

$$V_o = \left(1 + \frac{R_F}{R_1}\right)V_1$$

For $R_1 = 10$ kΩ:

$$V_o = \left(1 + \frac{200\text{ k}\Omega}{10\text{ k}\Omega}\right)(0.5\text{ V}) = 21(0.5\text{ V}) = \mathbf{10.5\ V}$$

For $R_1 = 20$ kΩ:

$$V_o = \left(1 + \frac{200\text{ k}\Omega}{20\text{ k}\Omega}\right)(0.5\text{ V}) = 11(0.5\text{ V}) = \mathbf{5.5\ V}$$

V_o ranges from 5.5 V to 10.5 V.

Numerical-8

What is the results in the circuit shown if the input for an input of V_1= - 0.3 V?

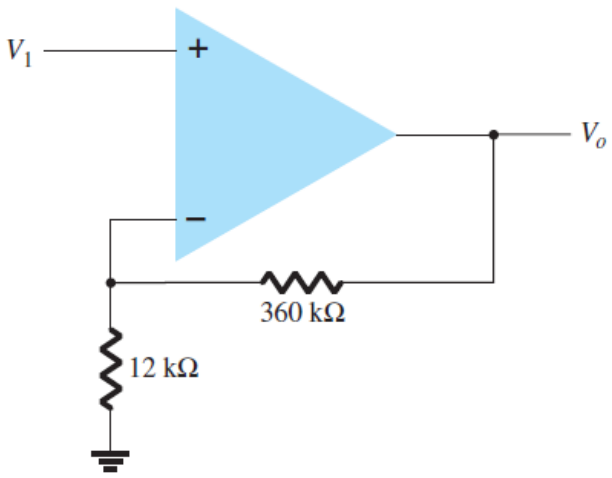


FIG. 10.66

$$V_o = \left(1 + \frac{R_F}{R_1}\right)V_1 = \left(1 + \frac{360\ \text{k}\Omega}{12\ \text{k}\Omega}\right)(-0.3\ \text{V})$$

$$= 31(-0.3\ \text{V}) = \mathbf{-9.3\ V}$$

Numerical-9

What input must be applied to the input of the circuit shown in the figure to result in an output of 2.4 V?

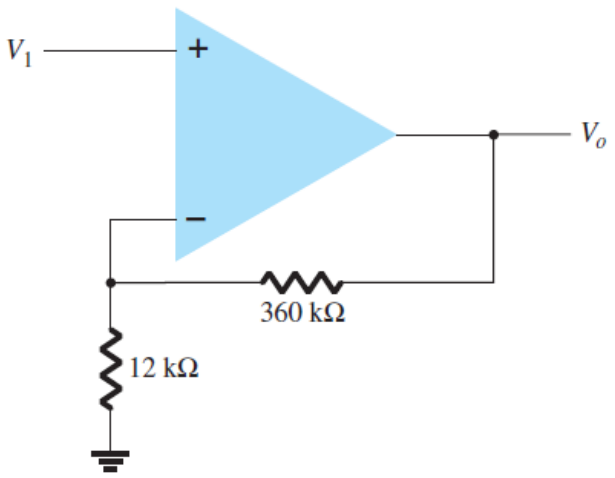


FIG. 10.66

$$V_o = \left(1 + \frac{R_F}{R_1}\right)V_1 = \left(1 + \frac{360\ \text{k}\Omega}{12\ \text{k}\Omega}\right)V_1 = 2.4\ \text{V}$$

$$V_1 = \frac{2.4\ \text{V}}{31} = \mathbf{77.42\ mV}$$

Numerical-10

What output voltage results in the circuit shown in the figure for V_1= + 0.5V?

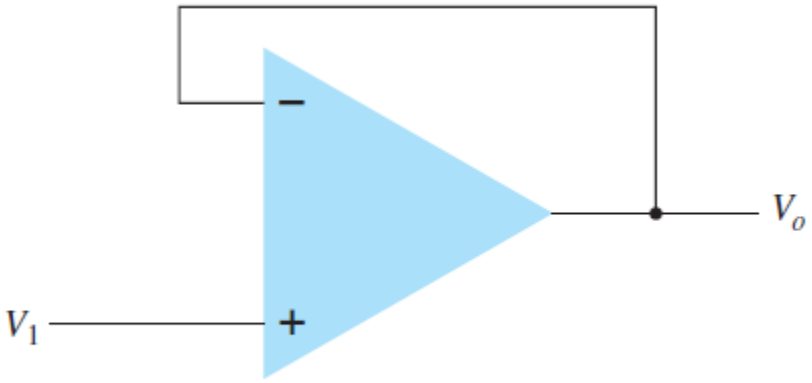


FIG. 10.70

$$V_o = V_1 = +0.5 \text{ V}$$

Numerical-11

Calculate the output voltage of a noninverting amplifier for values of V1 = 2V, Rf = 500 k, and R1 = 100k.

Soln: $$V_o = \left(1 + \frac{R_f}{R_1}\right)V_1 = \left(1 + \frac{500\ \text{k}\Omega}{100\ \text{k}\Omega}\right)(2\ \text{V}) = 6(2\ \text{V}) = \mathbf{+12\ V}$$

Numerical-12

Calculate the output voltage of an op-amp summing amplifier for the following sets of voltages and resistors. Use Rf = 1 M in all cases.

a. V1 = +1 V, V2 = +2 V, V3 = +3 V, R1 = 500 k, R2 = 1 M, R3 = 1 M.

b. V1 = -2 V, V2 = +3 V, V3 = +1 V, R1 = 200 k, R2 = 500 k, R3 = 1 M.

Soln: Using Summing Amplifier Equation,

$$\text{a. } V_o = -\left[\frac{1000\,\text{k}\Omega}{500\,\text{k}\Omega}(+1\text{ V}) + \frac{1000\,\text{k}\Omega}{1000\,\text{k}\Omega}(+2\text{ V}) + \frac{1000\,\text{k}\Omega}{1000\,\text{k}\Omega}(+3\text{ V})\right]$$

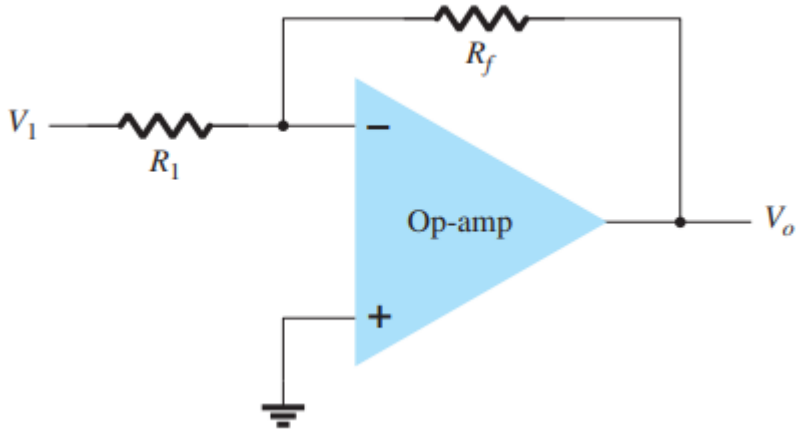
$$= -[2(1\text{ V}) + 1(2\text{ V}) + 1(3\text{ V})] = \mathbf{-7\text{ V}}$$

$$\text{b. } V_o = -\left[\frac{1000\,\text{k}\Omega}{200\,\text{k}\Omega}(-2\text{ V}) + \frac{1000\,\text{k}\Omega}{500\,\text{k}\Omega}(+3\text{ V}) + \frac{1000\,\text{k}\Omega}{1000\,\text{k}\Omega}(+1\text{ V})\right]$$

$$= -[5(-2\text{ V}) + 2(3\text{ V}) + 1(1\text{ V})] = \mathbf{+3\text{ V}}$$

Numerical-13

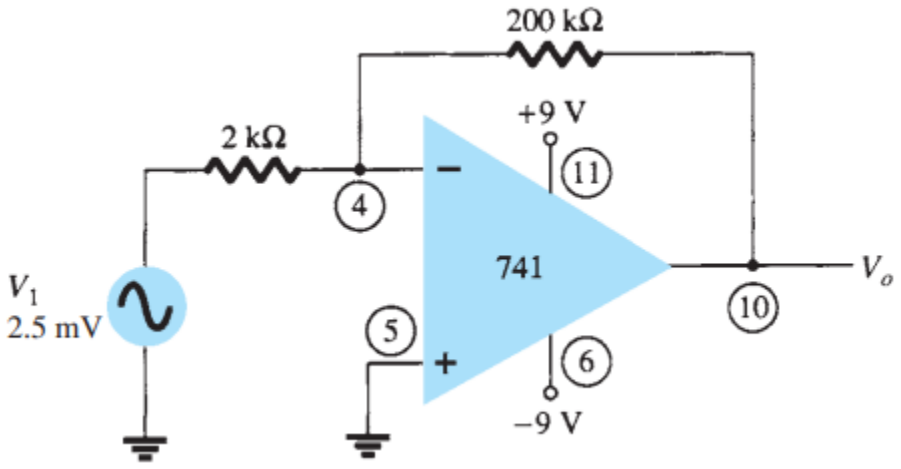
For the circuit shown, R1 = 100 k and R f 500 k, what output voltage results for an input of V1 = 2 V?



Soln: $$V_o = -\frac{R_f}{R_1}V_1 = -\frac{500\ \text{k}\Omega}{100\ \text{k}\Omega}(2\ \text{V}) = \mathbf{-10\ V}$$

Numerical-14

Determine the output voltage for the circuit of Fig with a sinusoidal input of 2.5 mV.



Soln:

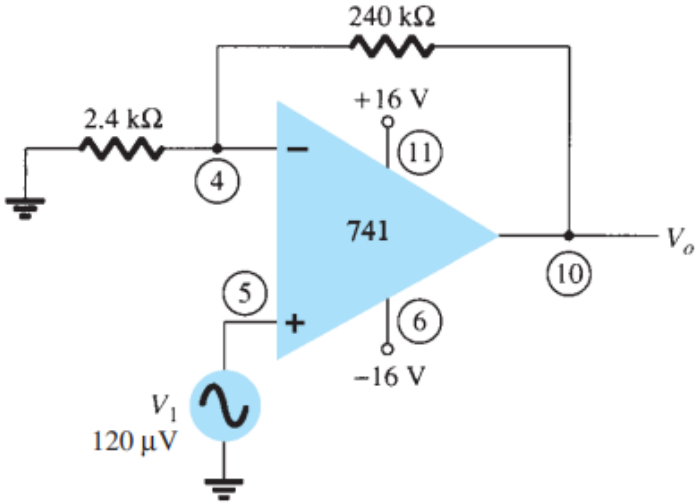
Gain $A = -\frac{R_f}{R_1} = -\frac{200\ \text{k}\Omega}{2\ \text{k}\Omega} = -100$

The output voltage is then

$$V_o = AV_i = -100(2.5\ \text{mV}) = -250\ \text{mV} = \mathbf{-0.25\ V}$$

Numerical-15

Calculate the output voltage from the circuit of Fig for an input of 120 mV.



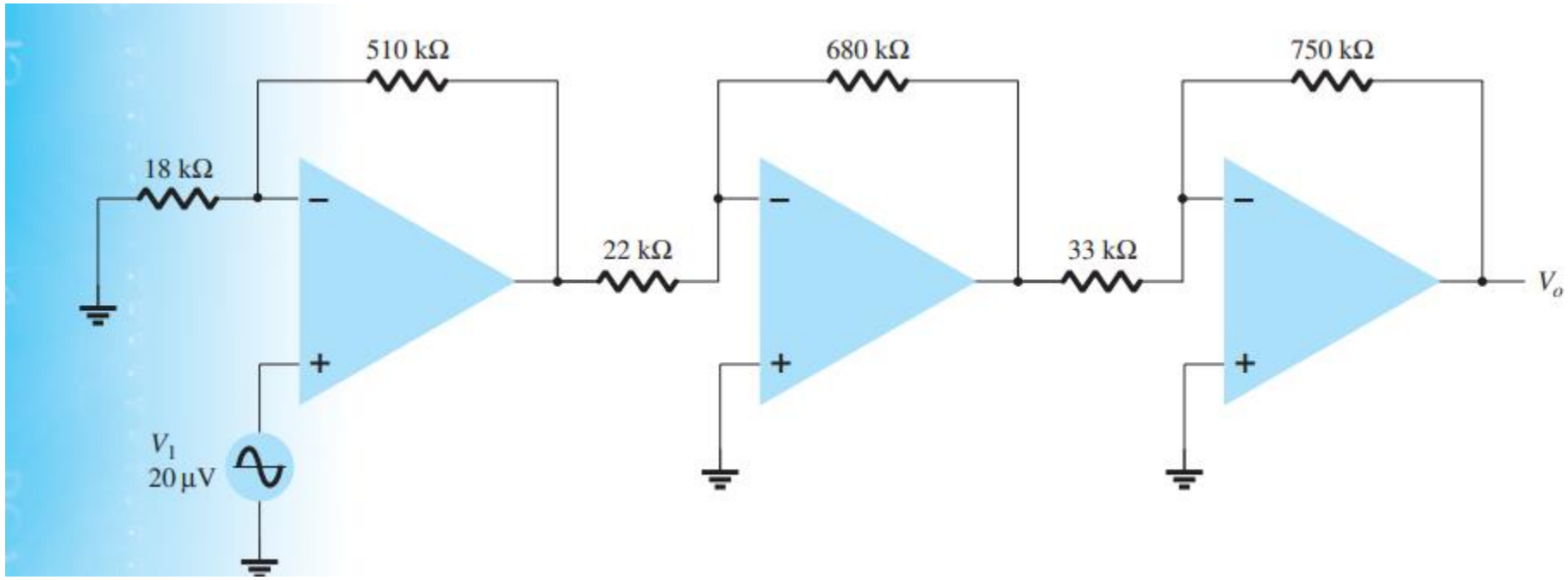
Soln: Gain $A = 1 + \frac{R_f}{R_1} = 1 + \frac{240\ \text{k}\Omega}{2.4\ \text{k}\Omega} = 1 + 100 = 101$

The output voltage is then

$$V_o = AV_i = 101(120\ \mu\text{V}) = \mathbf{12.12\ mV}$$

Numerical-16

Calculate the output voltage in the circuit.



Soln:

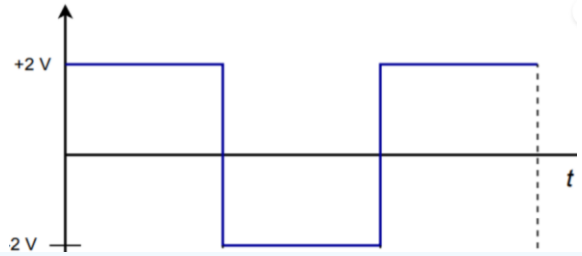
$$V_o = \left(1 + \frac{510\ \text{k}\Omega}{18\ \text{k}\Omega}\right)(20\ \mu\text{V})\left[-\frac{680\ \text{k}\Omega}{22\ \text{k}\Omega}\right]\left[-\frac{750\ \text{k}\Omega}{33\ \text{k}\Omega}\right]$$

$$= (29.33)(-30.91)(-22.73)(20\ \mu\text{V})$$

$$= \mathbf{412\ mV}$$

Numerical-17

Sketch the output of the integrator circuit if the input signal is a 10 kHz, 2 V peak square wave. Assume R=10KΩ and C=10nF.



Soln:

$$V_{in}(t) = 2 \text{ from } t = 0, \text{ to } t = 50\mu s$$

$$V_{in}(t) = -2 \text{ from } t = 50\mu s, \text{ to } t = 100\mu s$$

$$V_{out}(t) = -\frac{1}{R_i C}\int V_{in}(t)dt$$

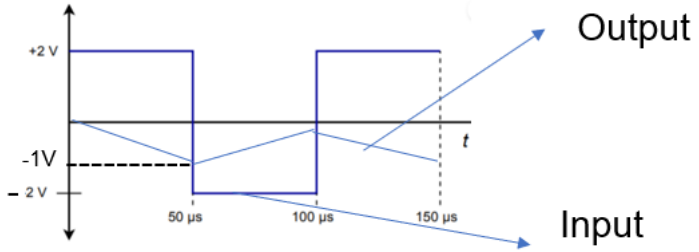
$$V_{out}(t) = -\frac{1}{10\text{ k} \times 10\text{ nF}}\int_0^{50\mu s} 2dt$$

$$V_{out}(t) = -10^4 \times 2 \times t|_{t=0}^{t=50\mu s}$$

$$V_{out} = -20000 \times 50\mu s$$

$$V_{out} = -1V$$

Vout represents total change over the 50 µs half-cycle interval with peak to peak output voltage of -1V. Where minus represents 180 degree phase shift output The resulting waveform is a ramp signal.



Numerical-18

Sketch the output waveform for the differentiator circuit if the input is 3 volt peak triangle wave at 4 kHz. Assume Rf=5KΩ and C=10nF

Soln:

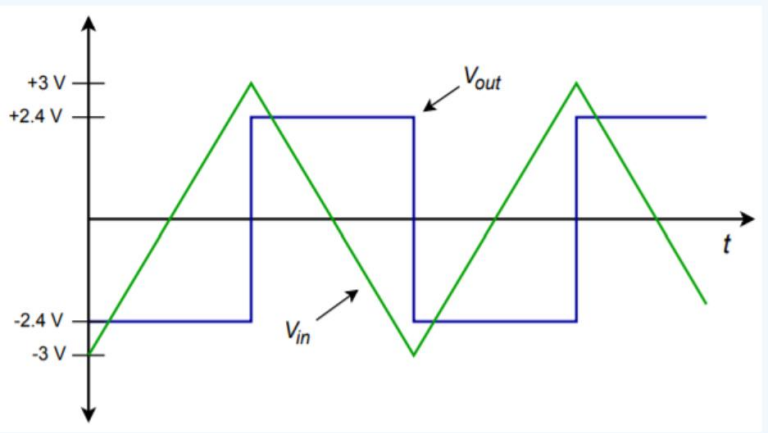
$$T = \frac{1}{4kHz}$$
$$T = 250\mu s$$

The slope (considering p-p) is

$$Slope = \frac{6V}{125\mu s}$$
$$Slope = 48000V/s$$

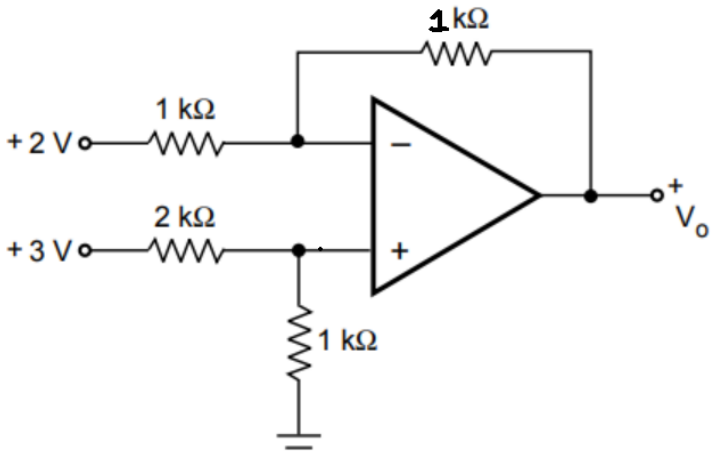
$$V_{in}(t) = 48000t$$

$$V_{out}(t) = -R_f C \frac{dV_{in}(t)}{dt}$$
$$V_{out}(t) = -5k \times 10nF \frac{d48000t}{dt}$$
$$V_{out}(t) = -2.4V \text{ Peak}$$



• Numerical-19

Determine the output voltage of the subtractor circuit shown.



Soln: From Superposition theorem,

$$V_o = V_{o1} + V_{o2}$$

$$= -\frac{R_f}{R_1} V_1 + \left[1+\frac{R_f}{R_1}\right]\left[\frac{R_f}{R_2+R_f}\right] V_2$$

Where R_1=1k,R_2=2K, R_f=1K

=-2+(2/3)*3
=0V

THANK YOU

Department of Electronics and Communication

ELECTRONIC PRINCIPLES AND DEVICES

Course Content

Department of Electronics and Communication.

ELECTRONIC PRINCIPLES AND DEVICES

Unit 4 –DIGITAL ELECTRONICS

ELECTRONIC PRINCIPLES AND DEVICES

Introduction

Digital electronics is a branch that deals with circuits and systems using digital signals.

Works with discrete signals represented by binary values— 0 and 1.

These binary values correspond to two voltage levels, typically representing "low" (0) and "high" (1).

Number System

Each number system is characterized by its **base** or **radix**, which determines the number of symbols used.

Base (or **Radix**) refers to the number of unique digits or symbols used in a number system.

For example: The **decimal system** has a base of 10, using digits 0 to 9.
The **binary system** has a base of 2, using digits 0 and 1.
The **hexadecimal system** has a base of 16, using digits 0 to 9 and letters A to F.

Binary Number System

Key features

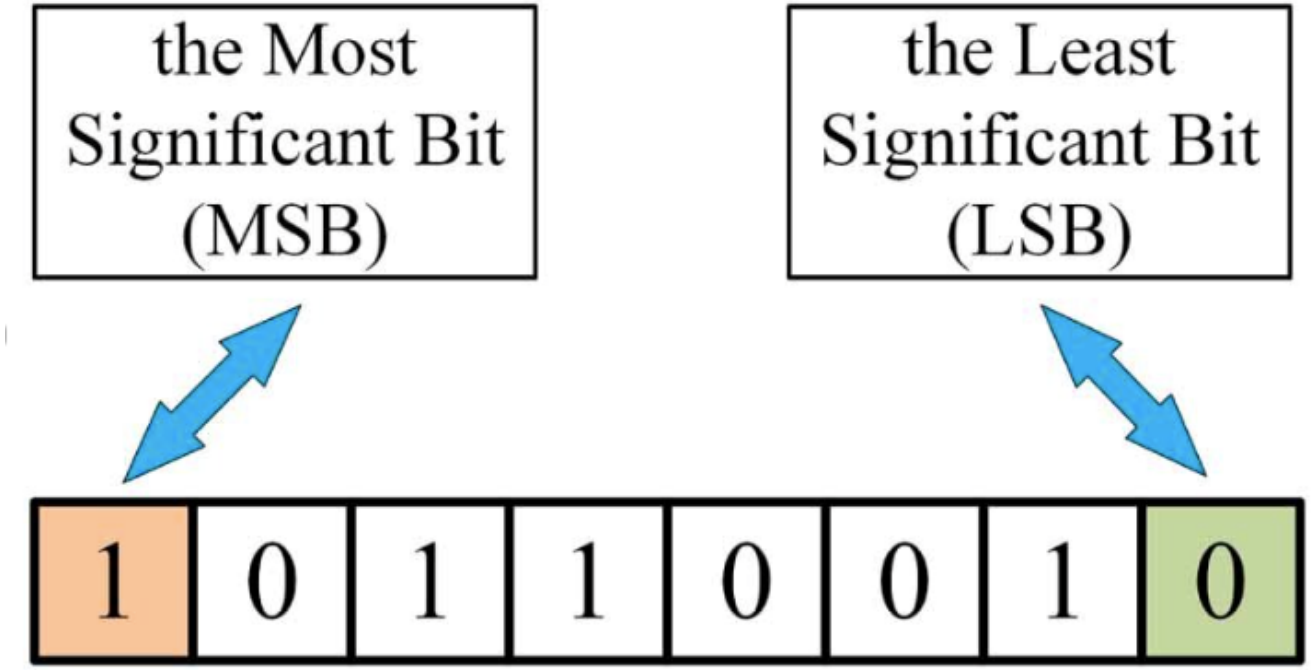
- The **binary number system** is a base-2 system that uses only two digits: **0** and **1**.
- Each digit in a binary number is called a **bit** (short for "binary digit").
- **Place Value:** Each bit in a binary number represents a specific power of 2, starting from 2^0 (rightmost bit) and increasing to 2^1 ,2^2,2^3, etc., as you move leftward.
- **Representation of Numbers:**
  Any numerical value can be represented in binary form using combinations of 0s and 1s.

The number of **bits** in a binary number determines the total number of unique combinations or values that can be represented.

If n is the number of bits, the maximum number values that can be represented using n bits equals 2^n

ELECTRONIC PRINCIPLES AND DEVICES

- In a binary number, the rightmost bit is called the **Least Significant Bit (LSB)** and the left most bit is the **Most Significant Bit (MSB).**



The place value of the LSB is 2^0 and the next digits to the left gets the place value in terms of increasing powers o
2.
In the above number, the place value of MSB is 2^7.

- Range of Values for Unsigned Binary Numbers
  In **unsigned binary**, all values are non-negative, starting from 0.

  Range= 0 to (2^n-1)

  For ex: With n=1 bit: no of values is 2^1=2 values (0,1)
  With n=2 bits: no of values is 2^2=4 values (00,01,10,11), 0 to 3 in decimal.
  With n= 3 bits: 2^3=8 values (000-111), 0 to 7 in decimal

- Range of Values for Signed Binary Numbers:
  In **signed binary**, one bit is reserved as the **sign bit** (0 for positive, 1 for negative).

  Range= -2^{n-1} to $(2^{n-1}-1)$

  For ex: With 2 bits: 2^2=4 values (−2 to 1), −2,−1,0,1,2
  With 3 bits: 2^3=8 values (−4 to 3), −4,−3,−2,−1,0,1,2,3

ELECTRONIC PRINCIPLES AND DEVICES

2 bit binary

Representation	Range
00	0
01	1
10	2
11	3

3 bit binary

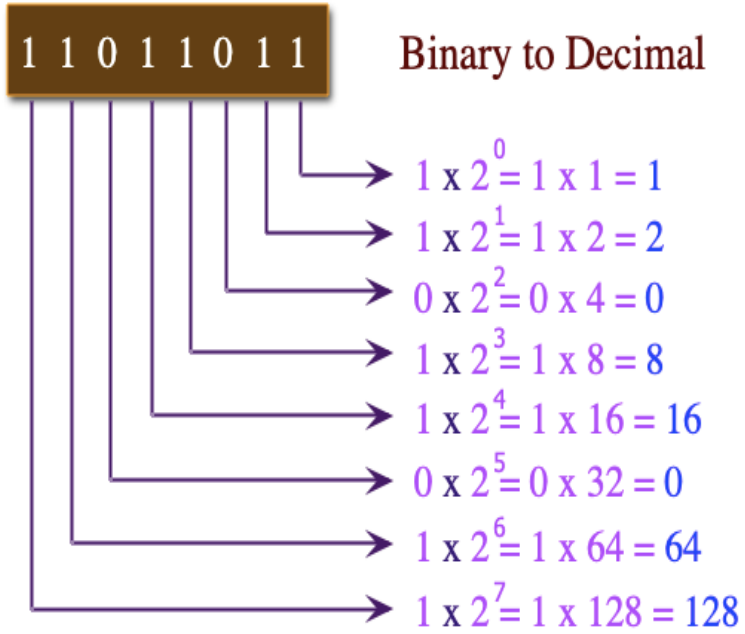
Representation	Range
000	0
001	1
010	2
011	3
100	4
101	5
110	6
111	7

4 bit binary

Representation	Range
0000	0
0001	1
0010	2
0011	3
0100	4
0101	5
0110	6
0111	7
1000	8
1001	9
1010	10
1011	11
1100	12
1101	13
1110	14
1111	15

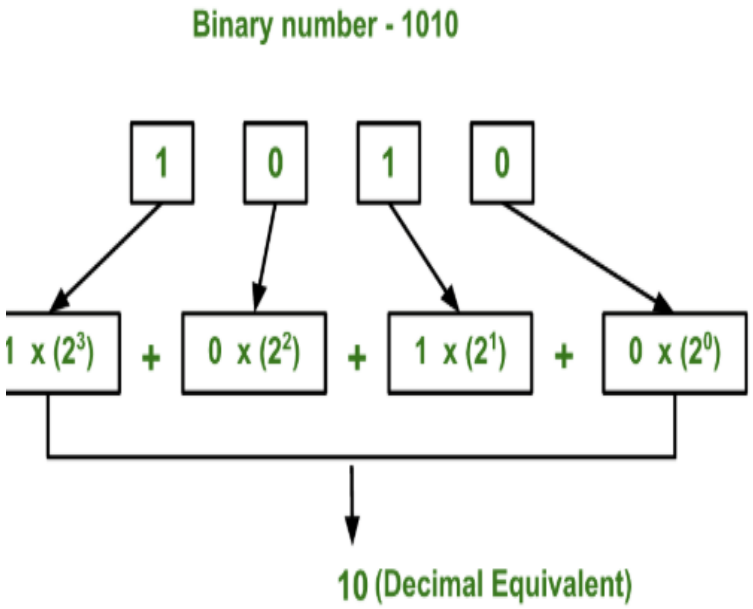
Binary to Decimal Conversion:

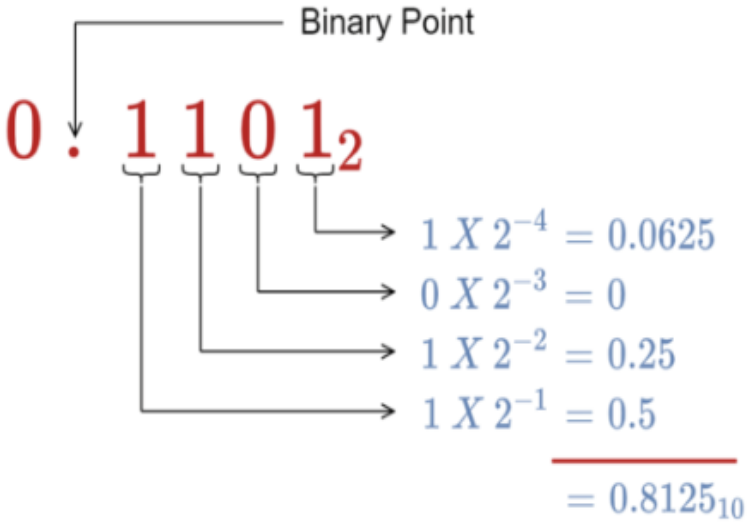
- Multiply each binary digit by the value of its position or place value (power of 2).
- Add all the products together to get the decimal equivalent



$$1 + 2 + 8 + 16 + 64 + 128 = 219$$

$$(11011011)_2 = (219)_{10}$$





ELECTRONIC PRINCIPLES AND DEVICES

Convert the following binary numbers to its decimal equivalent

a) 1011

Starting from LSB,

$$1\times 2^0 + 1\times 2^1 + 0\times 2^2 + 1\times 2^3$$

$$=1+2+0+8 = 11$$

$(1011)_2 = (11)_{10}$

b) 11010

$(11010)_2 = (26)_{10}$

c) 1111101

$(1111101)_2 = (127)_{10}$

d) 101.01011

$$101_2 = (1\times 2^2) + (0\times 2^1) + (1\times 2^0)$$

$$= (1\times 4) + (0\times 2) + (1\times 1)$$

$$= 4 + 0 + 1 = 5$$

$$.01011_2 = (0\times 2^{-1}) + (1\times 2^{-2}) + (0\times 2^{-3}) + (1\times 2^{-4}) + (1\times 2^{-5})$$

$$= 0 + \frac{1}{4} + 0 + \frac{1}{16} + \frac{1}{32}$$

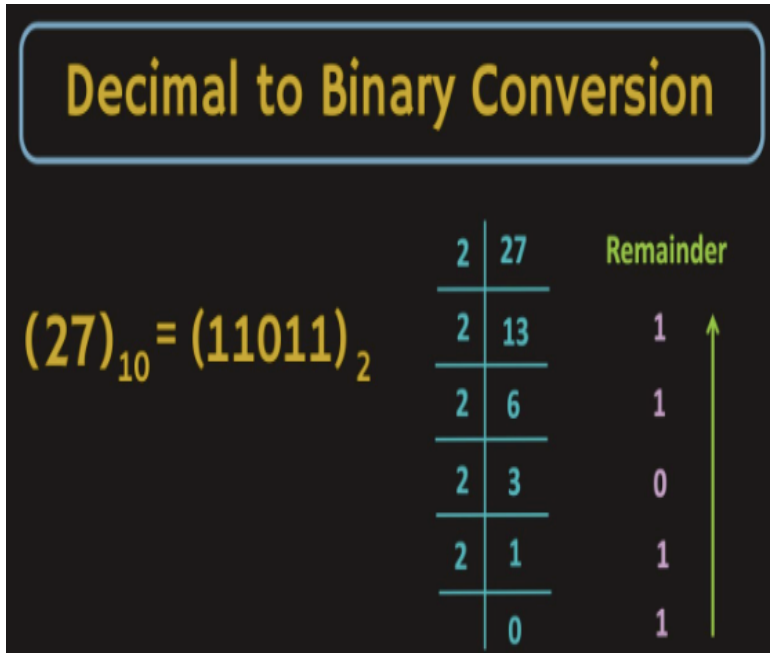
$$= 0 + 0.25 + 0 + 0.0625 + 0.03125 = 0.34375$$

$$101.01011_2 = 5.34375_{10}$$

Decimal to Binary Conversion

- Divide the Decimal Number by 2.
- Record the quotient and the remainder.
- Repeat the division by 2 until the quotient is 0.
- The last remainder represents the MSB and the first remainder represents the LSB. The remainders represent the equivalent binary number

2	4215		
2	2107	1	← LSB
2	1053	1	
2	526	1	
2	263	0	
2	131	1	
2	65	1	
2	32	1	
2	16	0	
2	8	0	
2	4	0	
2	2	0	
2	1	0	
	0	1	← MSB



Convert $(0.6875)_{10}$ to binary.

	Integer		Fraction
$0.6875 \times 2 =$	1	+	0.3750
$0.3750 \times 2 =$	0	+	0.7500
$0.7500 \times 2 =$	1	+	0.5000
$0.5000 \times 2 =$	1	+	0.0000

$(0.6875)_{10} = (0.1011)_2$

Convert the decimal number 41 to binary.

	Integer Quotient		Remainder	Coefficient
$41/2 =$	20	+	$\frac{1}{2}$	$a_0 = 1$
$20/2 =$	10	+	0	$a_1 = 0$
$10/2 =$	5	+	0	$a_2 = 0$
$5/2 =$	2	+	$\frac{1}{2}$	$a_3 = 1$
$2/2 =$	1	+	0	$a_4 = 0$
$1/2 =$	0	+	$\frac{1}{2}$	$a_5 = 1$

$(41)_{10} = (101001)_2$

Hexadecimal Number System

The **hexadecimal (base-16)** number system is a positional numeral system that uses **16 distinct symbols** to represent values.

Symbols Used:

- **Digits:** 0, 1, 2, 3, 4, 5, 6, 7, 8, 9

- **Letters:** A, B, C, D, E, F
  (where A = 10, B = 11, C = 12, D = 13, E = 14, F = 15 in decimal).

- **Place Values:**
Each digit in a hexadecimal number represents a power of 16, starting from 16^0 at the rightmost position

Ex: 1A316, 2AC

Hexadecimal	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
Decimal	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

Hexadecimal to Decimal Conversion

- Convert each hexadecimal bit into its decimal equivalent.
- Multiply each bit by the value of its position or place value (power of 16).
- Add all the products together to get the decimal equivalent

Hexadecimal	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
Decimal	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

2F36

$6\times 16^0 + 3\times 16^1 + 15\times 16^2 + 2\times 16^3$

= 8192+3840+48+6
=12086

$(B65F)_{16}$

$$(B65F)_{16} = 11 \times 16^3 + 6 \times 16^2 + 5 \times 16^1 + 15 \times 16^0 = (46{,}687)_{10}$$

Decimal to Hexadecimal Conversion

Divide the Decimal Number by 16

Divide the decimal number by 16. The quotient will be used for the next division, and the remainder will be one of the hexadecimal digits.

Record the Remainder

The remainder of each division corresponds to a hexadecimal digit. If the remainder is between 10 and 15, use the hexadecimal letters:

Hexadecimal	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
Decimal	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

Repeat the Division

Divide the quotient by 16 again, and continue recording the remainders until the quotient is 0.

Read the Remainders in Reverse Order

The remainders, when read from last to first, form the hexadecimal representation of the decimal number.

Example 1: Convert 255 (Decimal) to Hexadecimal
Step 1: Divide 255 by 16:

$$255 \div 16 = 15 \text{ (quotient)} \quad \text{remainder} = 15$$

Step 2: Divide the quotient (15) by 16:

$$15 \div 16 = 0 \text{ (quotient)} \quad \text{remainder} = 15$$

Step 3: The quotient is now 0, so stop dividing.

Step 4: Read the remainders in reverse order: The remainders, from last to first, are F and F.
Thus, **255 (decimal) = FF (hexadecimal)**.

ELECTRONIC PRINCIPLES AND DEVICES
1's Complement

One's Complement

If all bits in a byte are inverted by changing each 1 to 0 and each 0 to 1, we have formed the one's complement of the number.

```
Original      One's Complement
-------------------------------
10011001  -->  01100110
10000001  -->  01111110
11110000  -->  00001111
11111111  -->  00000000
00000000  -->  11111111
```

1's Complement Representation in Signed Magnitude :

In sign-magnitude, 6 is a positive number, its binary representation is 0000 0110, and it will be represented as it is, i.e. 0000 0110. Whereas a negative number suppose -6 will be represented as 1111 1001

ELECTRONIC PRINCIPLES AND DEVICES

2's Complement

To form the two's complement, add 1 to the one's complement.

Step 1: Begin with the original binary value

```
 10011001  Original byte
```

Step 2: Find the one's complement

```
 01100110  One's complement
```

Step 3: Add 1 to the one's complement

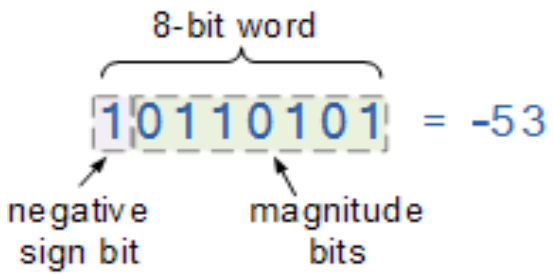
```
 01100110  One's complement
+       1  Add 1
  -----------
 01100111  <---  Two's complement
```

ELECTRONIC PRINCIPLES AND DEVICES
2's Complement

2's Complement Representation in Signed Magnitude :

For signed binary numbers the most significant bit (MSB) is used as the sign bit.
If the sign bit is "0", this means the number is positive in value.
If the sign bit is "1", then the number is negative in value.

Positive Signed Binary Number



Negative Signed Binary Number

Binary Addition using 2's Complement

(2) 8 + (-5) = ?
This example can also be read as 8 – 5 = ?

Binary equivalent of 8 = 00001000
2's complement representation of -5 = 11111011

```
                 0 0 0 0 1 0 0 0
              +  1 1 1 1 1 0 1 1
              ------------------
Discard Carry  1 0 0 0 0 0 0 1 1

Sum: 0 0 0 0 0 0 1 1
```

Sign bit is zero, so the result is a positive number

```
   8
+ -5
-----
   3
```

www.vlsifacts.com

3 => 00000011

Binary Subtraction using 2's Complement

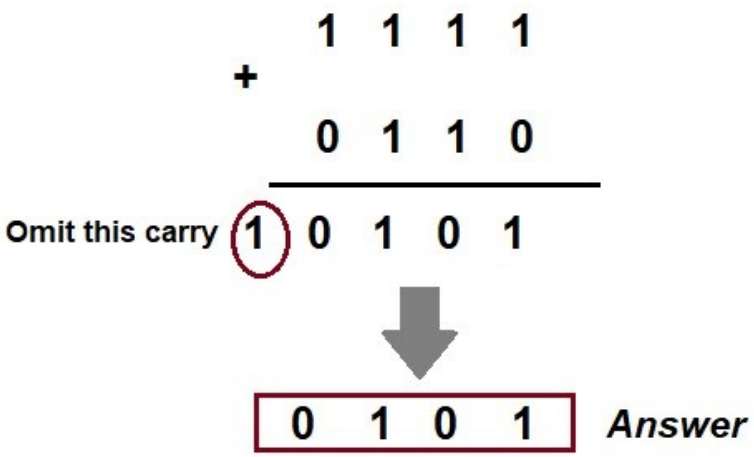
(1) Subtract (1010)2 from (1111)2 using 2's complement method.

Solution:

Step-1: 2's complement of (1010)2 is (0110)2.

Step-2: Add (0110)2 to (1111)2. This is shown below.

method of 2s complement subtraction of smaller number from a larger number



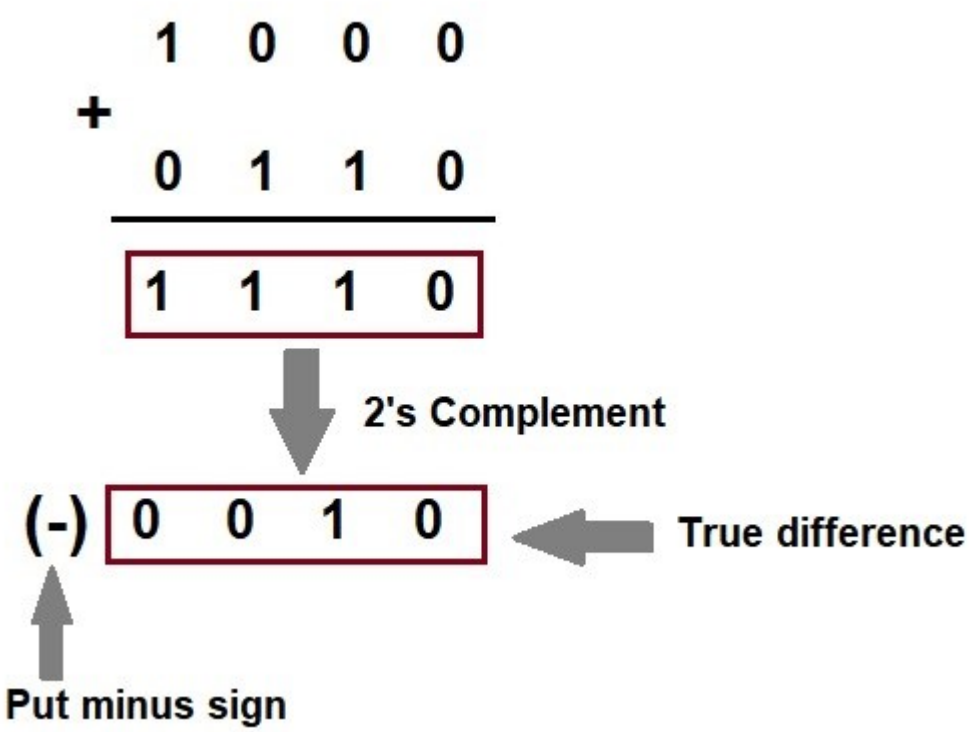
Binary Subtraction using 2's Complement

(1) ***Example-2:*** Subtract $(1010)_2$ from $(1000)_2$ using 2's complement.

Solution:

Step-1: Find the 2's complement of $(1010)_2$. It is $(0110)_2$.

Step-2: Add $(0110)_2$ to $(1000)_2$.



Boolean Algebra and Logic gates

- Digital Electronic circuits process data that contains **binary values 1's and 0's.**
- A **Logic "1"** is also referred as HIGH voltage or TRUE or ON state
- A **Logic "0"** is also referred as LOW voltage or FALSE or OFF state
- A binary digit "0" or "1" is called a **bit**
- Digital information is stored using a series of binary values 1's and 0's.
- Digital systems such as digital telephones, digital cameras, computers, handheld portable devices and other high technology systems **stores and process** these binary values (1's and 0's)

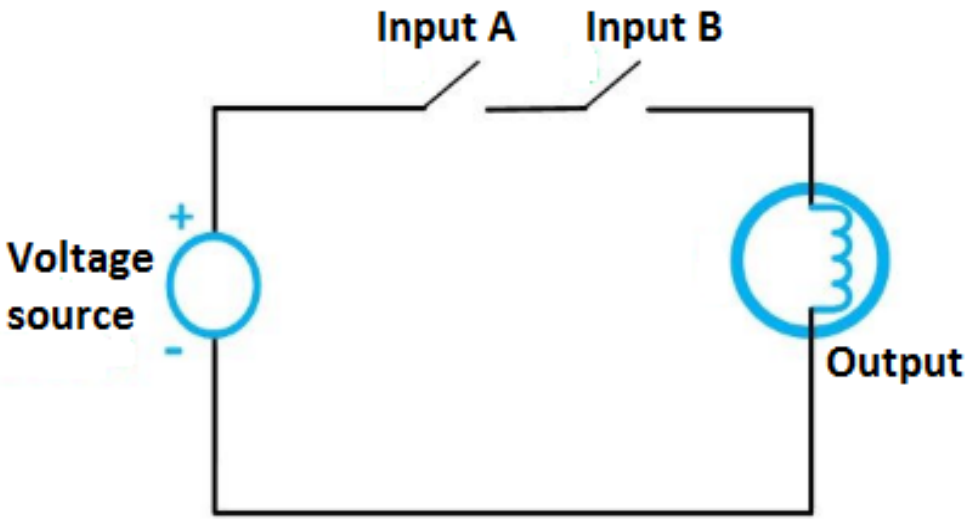
Boolean Algebra and Logic gates

- Boolean Algebra is the mathematics used to analyse and **simplify logic or digital circuits**.
- Digital circuits are constructed by using **logic gates**.
- Logic gates are the basic building blocks of digital systems, performs logical functions based on Boolean algebra.
- Logic gates have one or more inputs and only one output.
- Number of possible input states is **2^n**. Where n is Number of inputs
- Logic gates are implemented using diodes or transistors which acts as electronic switches
- logic gates **: (i) Basic Gates:** AND, OR, NOT,
  (ii) Derived Gates: NAND, NOR, EXOR and EXNOR gates

Boolean Algebra and Logic gates

- **AND Gate** is an electronic circuit that gives output as logic "1" (HIGH) only if all inputs are "1". Otherwise output is Logic "0" (LOW)
- Boolean algebra representation for AND gate is **Y = A.B**
- AND gate is represented as **series connection** of two switches

Symbol



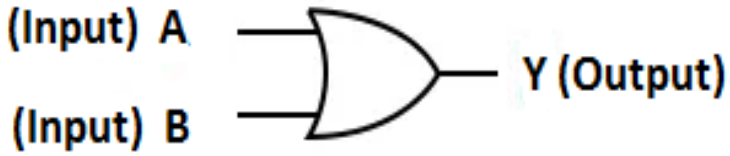
Truth Table

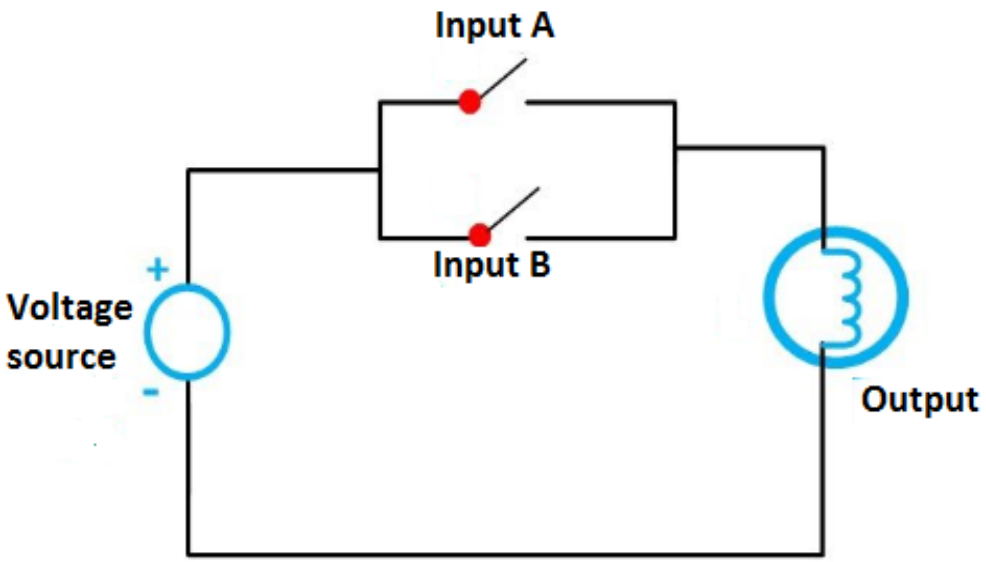
Inputs		Output
A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

Boolean Algebra and Logic gates

- **OR Gate** is an electronic circuit that gives as Logic “1” (HIGH) if any of the inputs are HIGH .Output of OR gate goes Logic “0” (LOW) only if all inputs are Logic “0” (LOW)
- Boolean algebra representation of OR gate is $Y = A + B$
- OR gate is represented as **parallel connection** of two switches

Symbol





Truth Table

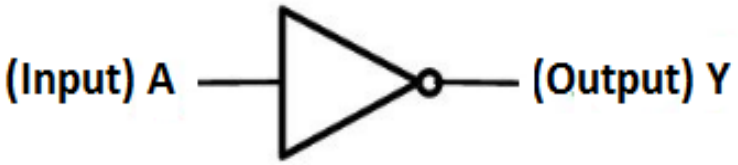
Inputs		Output
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

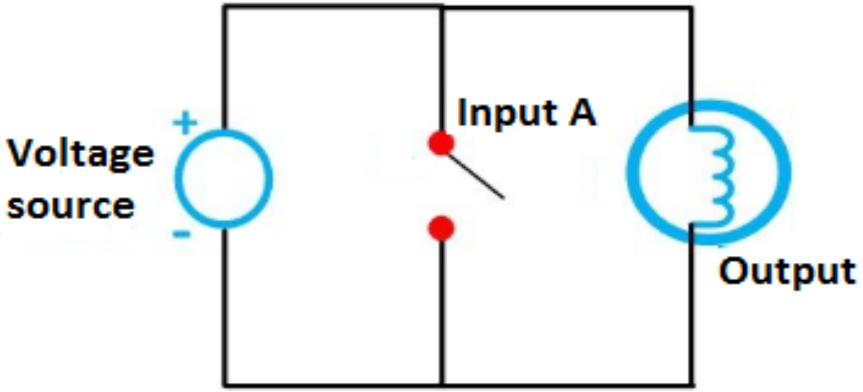
- **NOT Gate** is a single input and single output gate which performs the inversion of the applied binary input signal. Hence it is also called as Inverter Gate.

- Boolean expression for NOT gate is $Y = \overline{A}$

- NOT Gate can be represented by connecting a switch parallel to bulb

Symbol

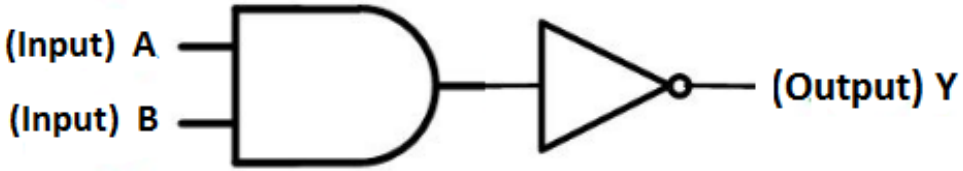




Truth Table

Input	Output
A	Y
0	1
1	0

NAND Gate

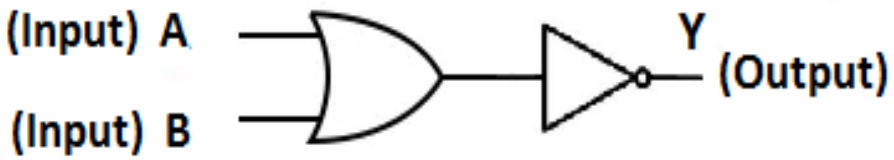


Symbol

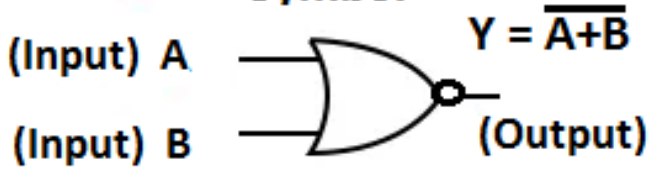
Truth Table

NAND		
Input		Output
A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

NOR Gate



Symbol



Truth Table

NOR		
Input		Output
A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

❖ Logical Boolean Laws:

❖ NOT / Inversion Law:

$$\overline{1} = 0$$
$$\overline{0} = 1$$

(i) If A = 1 then A’ = 0 and if A = 0 then A’ = 1

(ii) (A’)’ = A itself

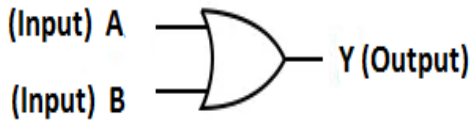
❖ AND Law:

Symbol

0.0 = 0	A.0 = 0
0.1 = 0	A.1 = A
1.0 = 0	A.A = A
1.1 = 1	A.A’ = 0

❖ OR Law:

Symbol



0+0 = 0	A+0 = A
0+1 = 1	A+1 = 1
1+0 = 1	A+A = A
1+1 = 1	A+A’ = 1

❖ Principle of duality in Boolean Algebra

❖ In Boolean Algebra , One type of expression can be converted into another type of expression by replacing "0 with 1 " , " 1 with 0" , "(+) sign with (.) sign " and vice versa.

AND (.)	OR (+)
0.0 = 0	1+1 = 1
0.1 = 0	1+0 = 1
1.0 = 0	0+1 = 1
1.1 = 1	0+0 =0

Example:

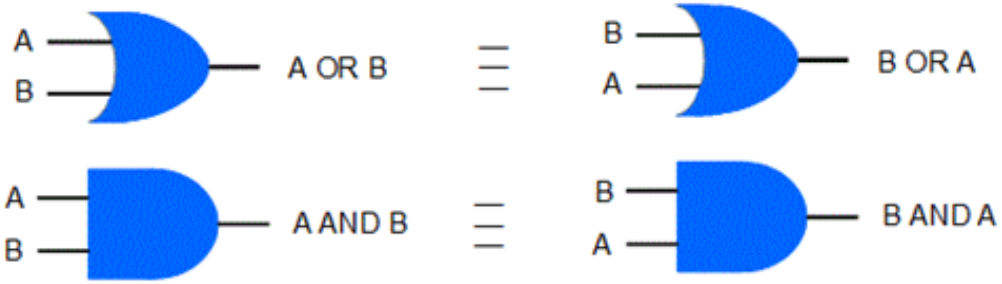
Expression	Dual Expression
$\overline{0} = 1$	$\overline{1} = 0$
$0.1 = 0$	$1 + 0 = 1$
$A.0 = 0$	$A + 1 = 1$
$A.B = B.A$	$A + B = B + A$
$A.\overline{A} = 0$	$A + \overline{A} = 1$

Basic Theorem and Properties of Boolean Algebra

❖ Boolean Laws and Theorems are used to simplify the Boolean expressions. Hence reduce the number of logic gates.

❖ **Commutative Laws:** (i) A+ B = B+ A

(ii) A.B = B.A



Proof: Logic circuits

A	B	(A+B)	(B+A)	(A.B)	(B.A)
0	0	0	0	0	0
0	1	1	1	0	0
1	0	1	1	0	0
1	1	1	1	1	1

Proof: Truth Table

Basic Theorems and Properties of Boolean Algebra

❖ Associative Law:

(A+B)+C = A+(B+C) Boolean addition

❖ Proof:

A	B	C	A + B	(A + B) + C	B + C	A + (B + C)
0	0	0	0	0	0	0
0	0	1	0	1	1	1
0	1	0	1	1	1	1
0	1	1	1	1	1	1
1	0	0	1	1	0	1
1	0	1	1	1	1	1
1	1	0	1	1	1	1
1	1	1	1	1	1	1

❖ From principle of duality: (A.B).C = A.(B.C) Boolean Multiplication

Basic Theorem and Properties of Boolean Algebra

❖ Distributive Law:

$A + B.C = (A+B) . (A+C)$

❖ Proof: Truth Table

A	B	C	BC	A+BC	(A+B)	(A+C)	(A+B)(A+C)
0	0	0	0	0	0	0	0
0	0	1	0	0	0	1	0
0	1	0	0	0	1	0	0
0	1	1	1	1	1	1	1
1	0	0	0	1	1	1	1
1	0	1	0	1	1	1	1
1	1	0	0	1	1	1	1
1	1	1	1	1	1	1	1

Dual of distributive law:

$A . (B+C) = A.B + A.C$

❖ Proof: Truth Table

A	B	C	B+C	A(B+C)	AB	AC	AB+AC
0	0	0	0	0	0	0	0
0	0	1	1	0	0	0	0
0	1	0	1	0	0	0	0
0	1	1	1	0	0	0	0
1	0	0	0	0	0	0	0
1	0	1	1	1	0	1	1
1	1	0	1	1	1	0	1
1	1	1	1	1	1	1	1

❖ De Morgan's Theorem :

(i) The complement of the sum of 2 variables is equal to the product of the complements of individual variables:

$$\overline{A+B} = \overline{A}\,.\,\overline{B}$$

(ii) The complement of the product of 2 variables is equal to the sum of the complements of individual variables:

$$\overline{A.B} = \overline{A} + \overline{B}$$

A	B	$\overline{A}$	$\overline{B}$	$A+B$	$A.B$	$\overline{A+B}$	$\overline{A}\,.\,\overline{B}$	$\overline{A\,.\,B}$	$\overline{A}+\overline{B}$
0	0	1	1	0	0	1	1	1	1
0	1	1	0	1	0	0	0	1	1
1	0	0	1	1	0	0	0	1	1
1	1	0	0	1	1	0	0	0	0

Basic Theorem and Properties of Boolean Algebra

❖ Absorption Theorem:

(i) A+AB = A

LHS: $= A + AB$

$= A.1 + AB \rightarrow$ since $A.1 = A$

$= A(1+B) \rightarrow$ since $1 + B = 1$

$= A.1$

$= A = RHS$

(ii) A(A+B) = A

LHS $= A (A + B)$

$= A.A + A.B$

$= A+AB \rightarrow$ since $A . A = A$

$= A (1 + B)$

$= A.1$

$= A = RHS$

(iii) $A+\bar{A}B = A+B$

LHS $= A + \bar{A}B$

$= (A + \bar{A}) (A + B) \rightarrow$ since $A+BC = (A+B)(A+C)$

$= (1) . (A + B) \rightarrow$ since $A + \bar{A} = 1$

$= A + B = RHS$

(iv) $A.(\bar{A}+B) = AB$

LHS $= A.(\bar{A} + B)$

$= A. \bar{A} + A.B \longrightarrow (A \bar{A} = 0)$

$= AB = RHS$

❖ Redundancy Laws

❖ Consensus Theorem:

$AB + \bar{A}C + BC = AB + \bar{A}C$

$LHS = AB + \bar{A}C + BC$

$= AB + \bar{A}C + BC.1$

$= AB + \bar{A}C + BC(A + \bar{A}) \rightarrow$ since $A + \bar{A} = 1$

$= AB + \bar{A}C + ABC + \bar{A}BC$

$= AB(1 + C) + \bar{A}C(1 + B)$

$1 + B = 1 + C = 1$

$= AB + \bar{A}C = RHS$

❖ **BC is redundant term**

❖ Dual of consensus theorem:

$(A+B)(\bar{A}+C)(B+C) = (A+B)(\bar{A}+C)$

$LHS = (A+B)(\bar{A}+C)(B+C)$

WKT $A+BC = (A+B)(A+C)$

$B + AC = (B+A)(B+C)$

$LHS = (B + AC)(\bar{A}+C)$

$= \bar{A}B + \bar{A}AC + BC + ACC$

$= \bar{A}B + BC + AC + A\bar{A}$

$= B(\bar{A} + c) + A(\bar{A} + c)$

$= (A+B)(\bar{A}+C) = RHS$

Boolean Functions, Canonical and Standard Form

- Boolean function described by an algebraic expression consists of **binary variables, the constants 0 and 1, and the logic operation symbols**.
- Boolean function is **evaluated to logic-1 or logic-0** for a given value of the binary variables.
- Boolean function can be represented in a **truth table**.
- A Boolean function can be implemented as **digital circuit**, Which is constructed by using logic gates.
- Example: $F = X + Y'Z$

  $F = 1$ if $X = 1$ or if $Y = 0$ and $Z = 1$

  $F = 0$ Otherwise

Boolean Functions, Canonical and Standard Form

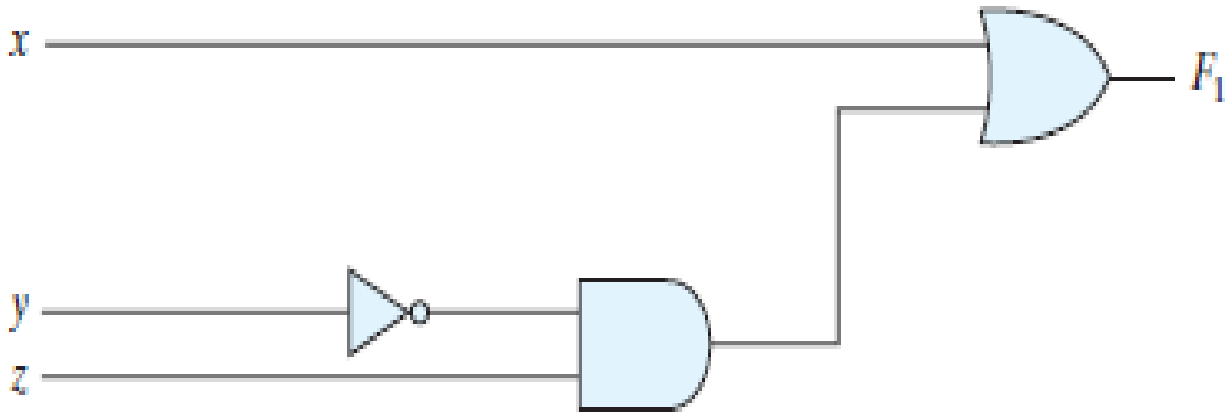
- Example: $F_1 = x + y'z$

- F_1 contains either 0 or 1 for each of these combinations. The table shows that the function is equal to 1 when x = 1 or when yz = 01 and is equal to 0 otherwise.

Truth Table:

x	y	z	F_1
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

Gate Level Implementation:



Reference: "Digital Design with an Introduction to Verilog HDL" M Morris Mano, Michale D Ciletti

Boolean Functions, Canonical and Standard Form

❖ Simplify and realize the given Boolean function using basic gates

$F_2 = x'y'z + x'yz + xy'$.....(1)

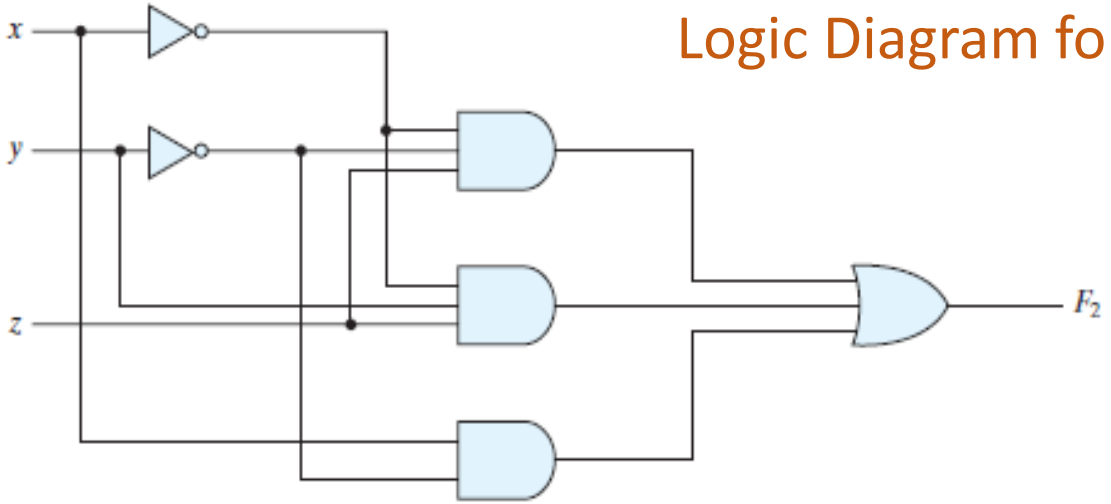
$F_2 = x'z(y' + y) + xy'$

$F_2 = x'z + xy'$.....(2)

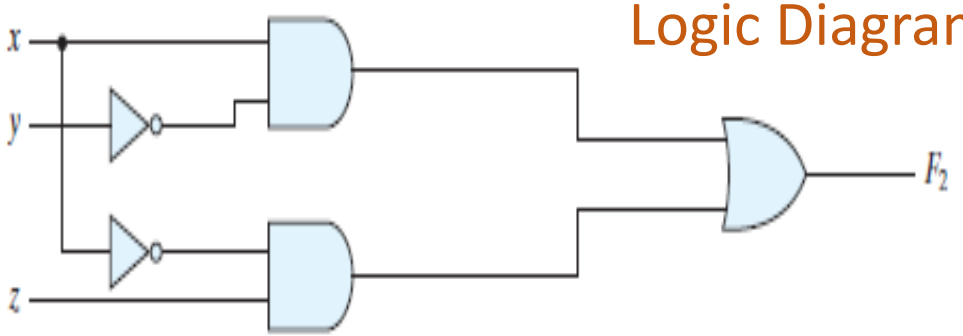
Truth Table

x	y	z	F_2
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	0

Logic Diagram for eq.1



Logic Diagram for eq.2

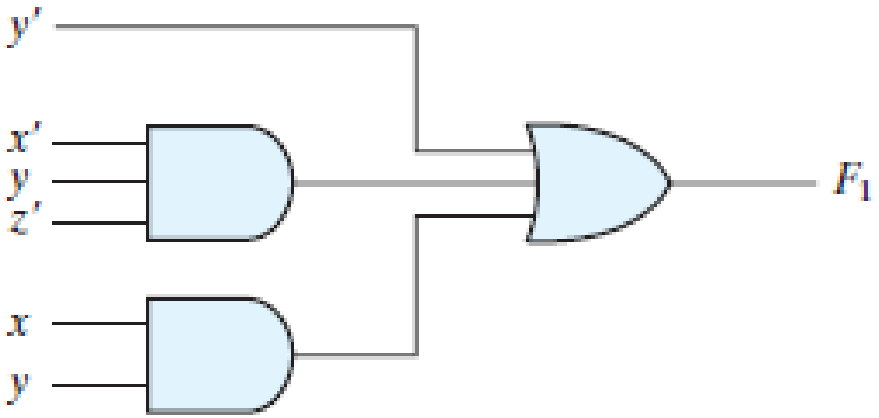


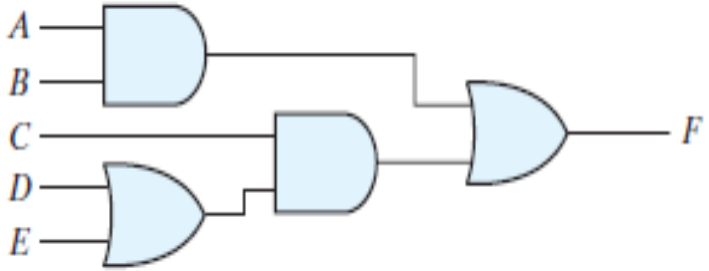
Reference: "Digital Design with an Introduction to Verilog HDL" M Morris Mano, Michale D Ciletti

❖ Sum of Products: (SOP)

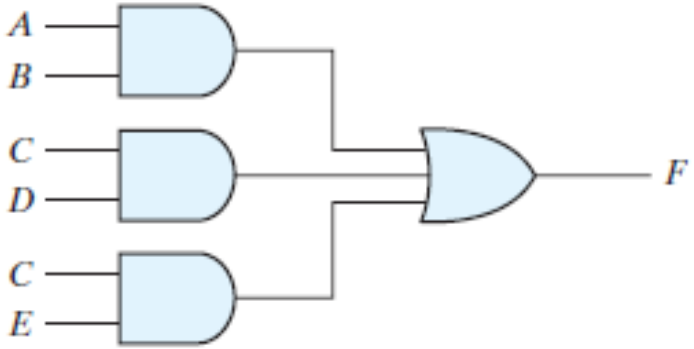
- The sum of products is a Boolean expression containing **AND** terms, called **product terms,** with one or more literals each. The **sum** denotes the **OR**ing of these terms.
- Two- Level Logic implementation of SOP

❖ Example 1 : $F_1 = y' + xy + x'yz'$





Example 2:
F = AB + C (D+E)



F = AB + CD + CE

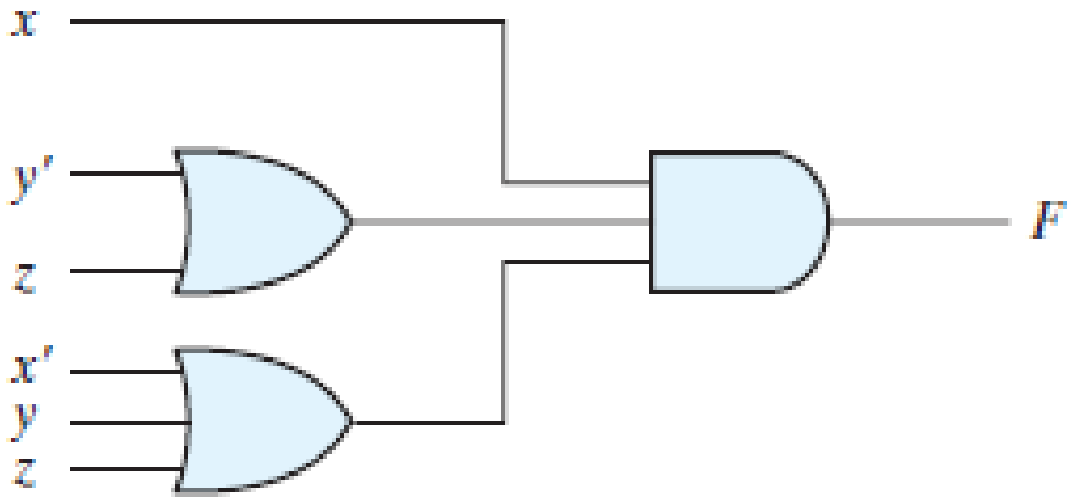
Reference: "Digital Design with an Introduction to Verilog HDL" M Morris Mano, Michale D Ciletti

❖ Product Of Sum: POS

- A product of sum (POS) is a Boolean expression containing OR terms, called sum terms. Each term may have any number of literals. The product denotes the ANDing of these terms

- Example 1 :

  F = x.(y’ + z).(x’ + y + z)



- Example 2: Y = (A+B). (C+D)

❖ Canonical SOP Form:

- Each product term contains all the literals of that function either in true or complement form
- **Example:** F(x,y,z) = xyz + x'y'z + x'yz' +x'y'z'
- Each product term is called as **minterm**
- For three variable function: Truth Table

			Minterms	
x	y	z	Term	Designation
0	0	0	$x'y'z'$	m_0
0	0	1	$x'y'z$	m_1
0	1	0	$x'yz'$	m_2
0	1	1	$x'yz$	m_3
1	0	0	$xy'z'$	m_4
1	0	1	$xy'z$	m_5
1	1	0	xyz'	m_6
1	1	1	xyz	m_7

Boolean Functions, Canonical and Standard Form

❖ Consider the function: f1 and f2 in the truth table

x	y	z	Function f_1	Function f_2
0	0	0	0	0
0	0	1	1	0
0	1	0	0	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

❖ Canonical SOP Form for f1

f1 = x’y’z + xy’z’ + xyz = m1 + m4 + m7

❖ Canonical SOP Form for f2

f2 = x’yz + xy’z + xyz’ + xyz = m3 + m5 + m6 + m7

❖ Canonical POS Form:

- Each sum term contains all the literals of that function either in true or complement form
- **Example:** F(x, y, z) = (x +y+z) (x'+y'+z) (x'+y+z')
- Each sum term is called as **Maxterm**
- For three variable function: Truth Table

			Maxterms	
x	y	z	Term	Designation
0	0	0	$x + y + z$	M_0
0	0	1	$x + y + z'$	M_1
0	1	0	$x + y' + z$	M_2
0	1	1	$x + y' + z'$	M_3
1	0	0	$x' + y + z$	M_4
1	0	1	$x' + y + z'$	M_5
1	1	0	$x' + y' + z$	M_6
1	1	1	$x' + y' + z'$	M_7

Boolean Functions, Canonical and Standard Form

❖ Consider the function: f1 and f2 in the truth table

x	y	z	Function f_1	Function f_2
0	0	0	0	0
0	0	1	1	0
0	1	0	0	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

❖ Canonical POS Form for f1

f1 = (x + y + z)(x + y’ + z)(x + y’ + z’)(x’ + y + z’)(x’ + y’ + z)

= M0. M2 .M3 . M5 . M6

❖ Canonical POS Form for f2

f2 = (x + y + z)(x + y + z’)(x + y’ + z)(x’ + y + z)

= M0. M1. M2. M4

❖ Find the Minterms for the given expression: (Convert into canonical SOP Form)

$F = A + BC$

$F = A.1.1 + BC.1$

$F = A.(B+B').(C+C'). + BC.(A+A')$

$F = A.(BC + BC' + B'C + B'C') + ABC + A'BC$

$F = ABC + ABC' + AB'C + AB'C' + ABC + A'BC$

$F = ABC + ABC' + AB'C + AB'C' + A'BC$

$F = m7 + m6 + m5 + m4 + m3$

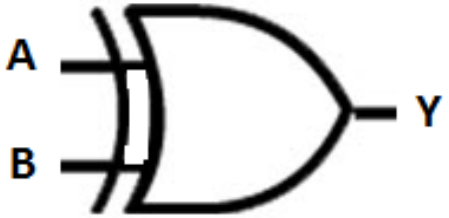
$F = \Sigma(3,4,5,6,7)$

Other Logical Operation, Digital Logic gates (XOR and XNOR)

- **XOR Gate** is a digital logic Gate which has two or more inputs and only one output that performs Exclusive OR operation. Hence it is also called as Ex-OR or XOR
- For two input XOR gate output is **logic-1** only when one of its input is logic-1 (unequal input i.e..A = 0 and B = 1 or A = 1 and B = 0).
- Output of XOR gate is **logic-0** if both inputs are same (i.e.., A = 0 and B = 0 or A = 1 and B = 1)
- Truth Table of XOR Gate:

Input A	Input B	Output Y
0	0	0
0	1	1
1	0	1
1	1	0

- Symbol



$A.B' + A'.B = A \oplus B$

Other Logical Operation, Digital Logic gates (XOR and XNOR)

❖ XOR gate performs modulo sum operation without including carry.
i.e.., 0+0 = 0 , 0+1 = 1, 1+0 = 1, 1+1 = 0 (carry 1)

❖ Truth Table

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

$Y = A'.B + A.B'$

$Y = A \text{ XOR } B$

$Y = A \oplus B$

$A.B' + A'.B = A \oplus B$

$LHS = A.B' + A'.B$

Case1: If A = 0 and B = 0
$0.0' + 0'.0 = 0.1 + 1.0 = 0$

Case2: If A = 0 and B = 1
$0.1' + 0'.1 = 0.0 + 1.1 = 1$

Case3: If A = 1 and B = 0
$1.0' + 1'.0 = 1.1 + 0.0 = 1$

Case4: If A = 1 and B = 1
$1.1' + 1'.1 = 1.0 + 0.1 = 0$

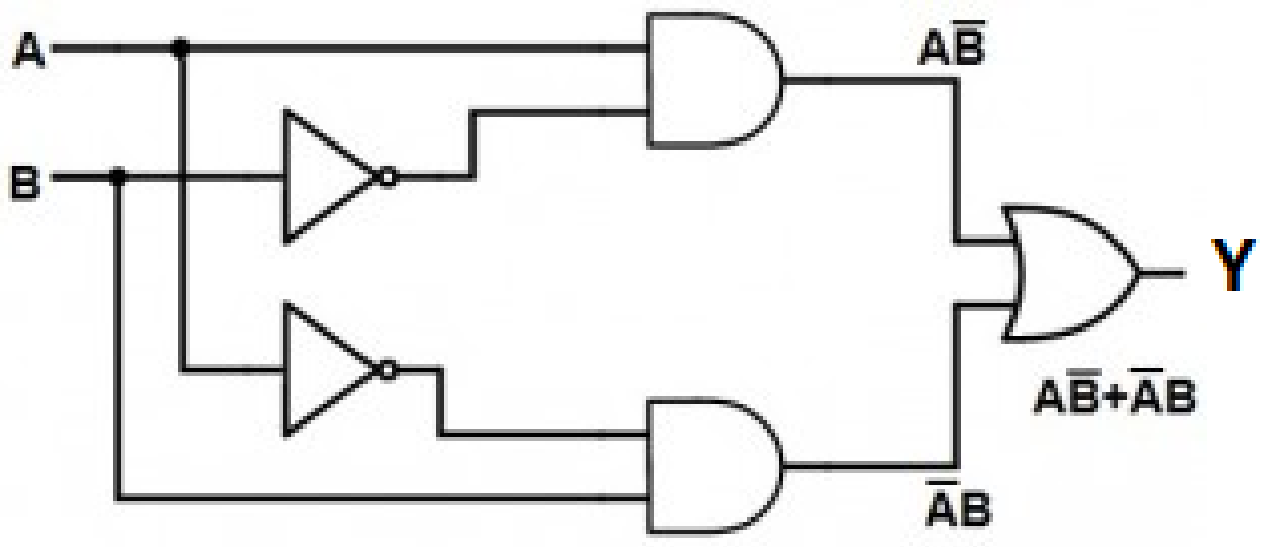
Hence $\mathbf{Y = A \oplus B = A.B' + A'.B}$

Other Logical Operation, Digital Logic gates (XOR and XNOR)

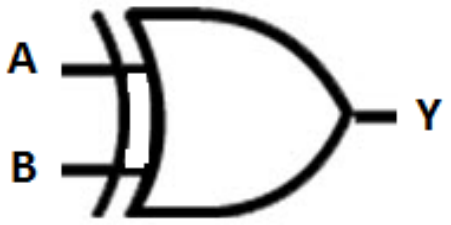
- Implementation of XOR Gate using basic gates:

  $Y = A \oplus B = A.B' + A'.B$

- Logic Diagram



- Symbol



Reference: "Digital Design with an Introduction to Verilog HDL" M Morris Mano, Michale D Ciletti

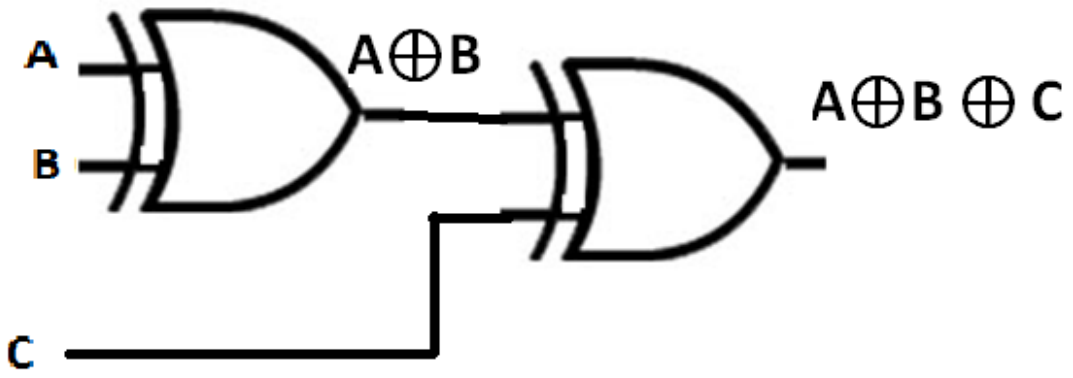
Other Logical Operation, Digital Logic gates (XOR and XNOR)

❖ **3 - Input XOR Gate:** $Y = A \oplus B \oplus C$

Truth Table

A	B	C	$A \oplus B$	$A \oplus B \oplus C$
0	0	0	0	0
0	0	1	0	1
0	1	0	1	1
0	1	1	1	0
1	0	0	1	1
1	0	1	1	0
1	1	0	0	0
1	1	1	0	1

Symbol



Associative Law:

$(A \oplus B) \oplus C = A \oplus (B \oplus C)$

❖ **Even or odd Parity Bits**

Other Logical Operation, Digital Logic gates (XOR and XNOR)

❖ **XNOR Gate**: Logical Complement of XOR Gate

❖ For two input XNOR Gate if both inputs are same i.e.., A = 0 and B = 0 or A = 1 and B = 1. Then output of logic gate is logic-1 (High). Output of XNOR is logic-0 if inputs are unequal.

❖ Equality detector

Truth Table

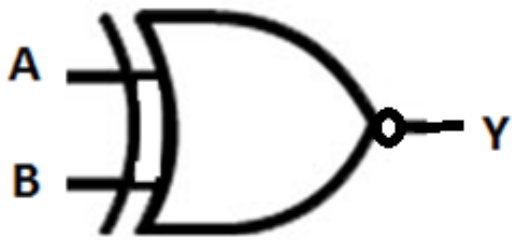
Input A	Input B	Output Y
0	0	1
0	1	0
1	0	0
1	1	1

❖ **Boolean Expression**

$$Y = A.B + A'.B'$$

$$Y = A \odot B$$

❖ **Symbol**



Other Logical Operation, Digital Logic gates (XOR and XNOR)

❖ XNOR Gate:

$Y = (A \oplus B)'$

$Y = (A.B' + A'.B)'$

De Morgan's Theorem

$Y = (A.B')' . (A'.B)'$

$Y = (A'+B) . (A + B')$

$Y = A'.A + A'.B' + A.B + B.B'$

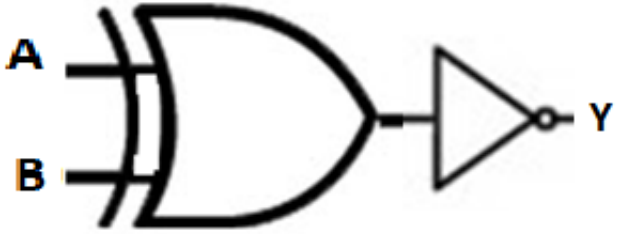
$Y = 0 + A'.B' + A.B + 0$

$Y = A'.B' + A.B$

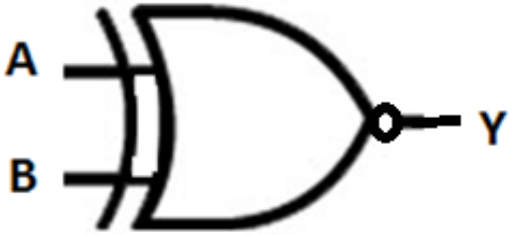
$Y = (A \oplus B)' = A \odot B$

$Y = (A \text{ XOR } B)' = (A \text{ XNOR } B)$

❖ Logic Diagram:



❖ Symbol:

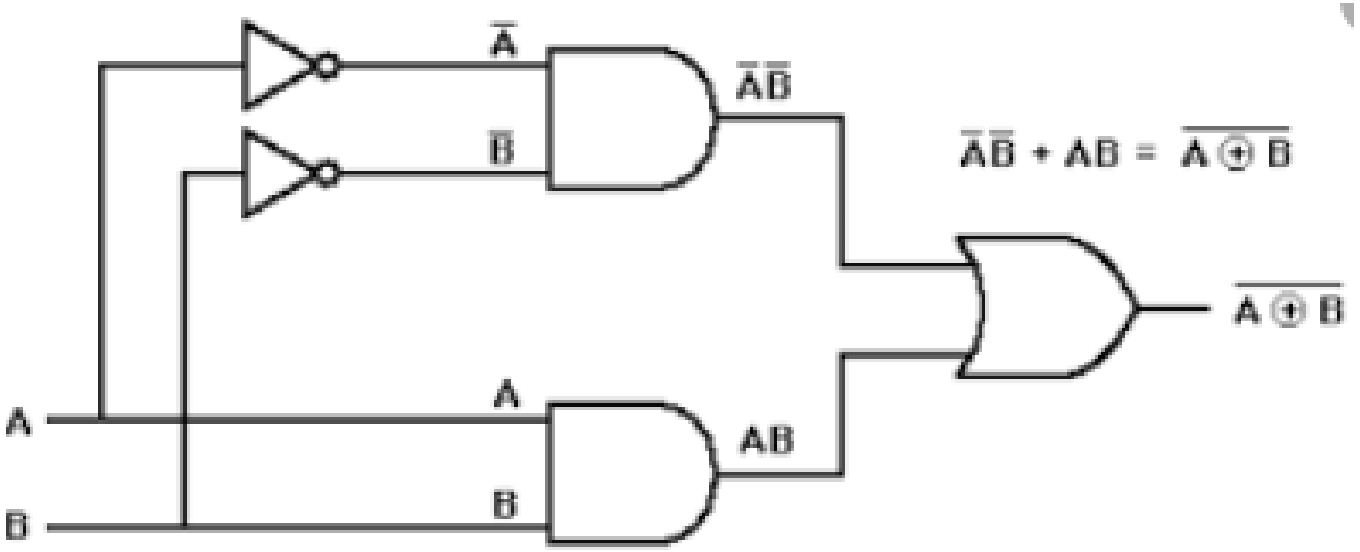


Other Logical Operation, Digital Logic gates (XOR and XNOR)

❖ Implement the XNOR Gate using basic gates:

$Y = A'.B' + A.\ B$

❖ Logic Diagram:



$Y = (A \oplus B\ )' = A \odot B$

Other Logical Operation, Digital Logic gates (XOR and XNOR)

❖ Properties of XOR Gate:

- Identity element: $A \oplus 0 = A$
- $A \oplus 1 = A'$
- $A \oplus A = 0$
- Commutative Law: $A \oplus B = B \oplus A$
- Associative Law : $A \oplus (B \oplus C) = (A \oplus B) \oplus C$

Input A	Input B	Output Y
0	0	0
0	1	1
1	0	1
1	1	0

❖ Applications of XOR and XNOR

- XOR gate is used in processor's Arithmetic Logic Unit (ALU) for binary addition.
- XOR logic gate is used to generate pseudorandom numbers in hardware.
- To generate parity bits and error detection
- Equality detector

Realization of Boolean expression using Universal Gates

- **Universal Gates** : (i) NAND Gate
  (ii) NOR Gate

- Any digital logic circuit can be implemented by using NAND or NOR logic gates.

- NAND and NOR gates are easier to fabricate with electronic components and are used in all Integrated Circuit (IC's) digital logic families.

Realization of Boolean expression using Universal Gates

❖ Realization of logic gates using NAND Gates:

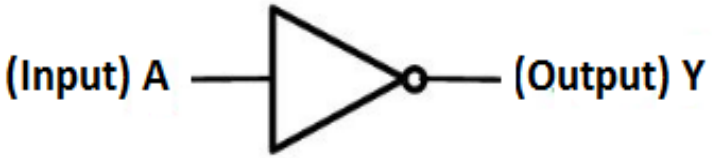
Symbol

Truth Table

NAND		
Input		Output
A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

❖ NOT Gate:

Symbol



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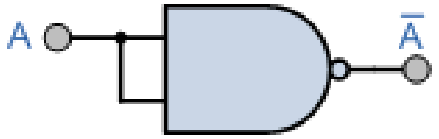
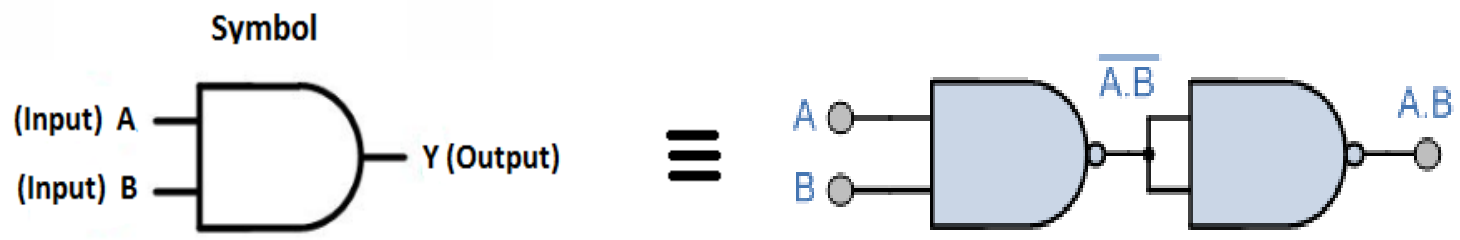


Y = (A.A)' = (A)' = A'

Reference: https://www.electronics-tutorials.ws/logic/universal-gates.html

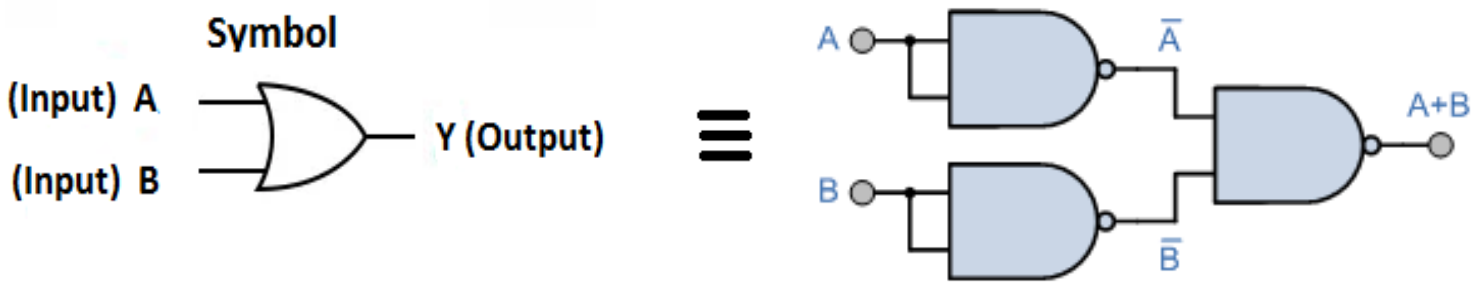
Realization of Boolean expression using Universal Gates

❖ AND Gate:



$Y = ((A.B)')' = A.B$

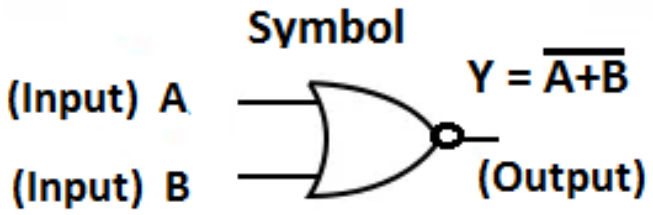
❖ OR Gate:



$Y = ((A+B)')' = (A' . B')' = A+B$

Realization of Boolean expression using Universal Gates

❖ NOR Gate:



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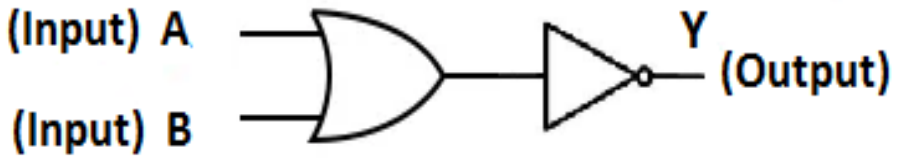

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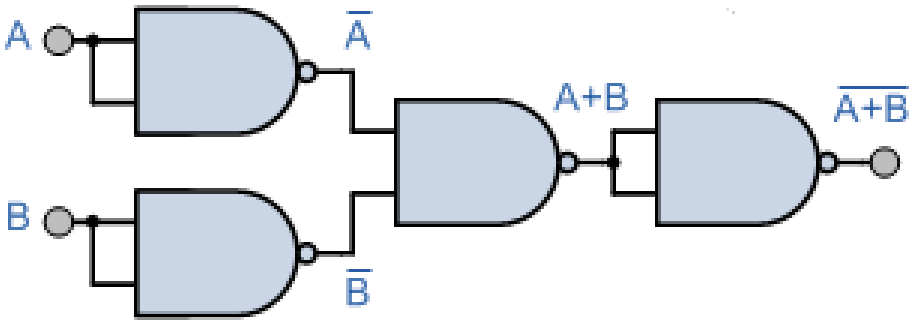
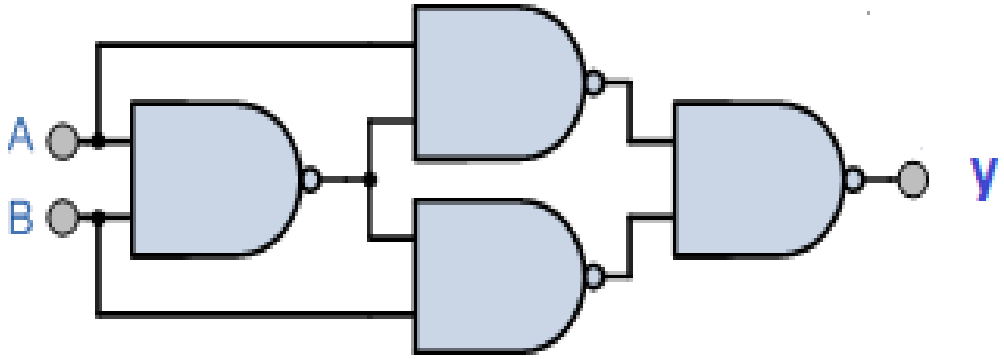


Realization of Boolean expression using Universal Gates

❖ XOR Gate:

≡



$Y = A \oplus B$

$Y = A.B' + A'B = A\,(A.B)' + B.\,(A.B)'$

$Y = ((A\,(A.B)' + B.\,(A.B)')')'$

$Y = ((\ (A.\,(A.B)')'\ .\ (B.(A.B)')'\ \ )))''$

$Y = A\,(A.B)' + B.\,(A.B)'$

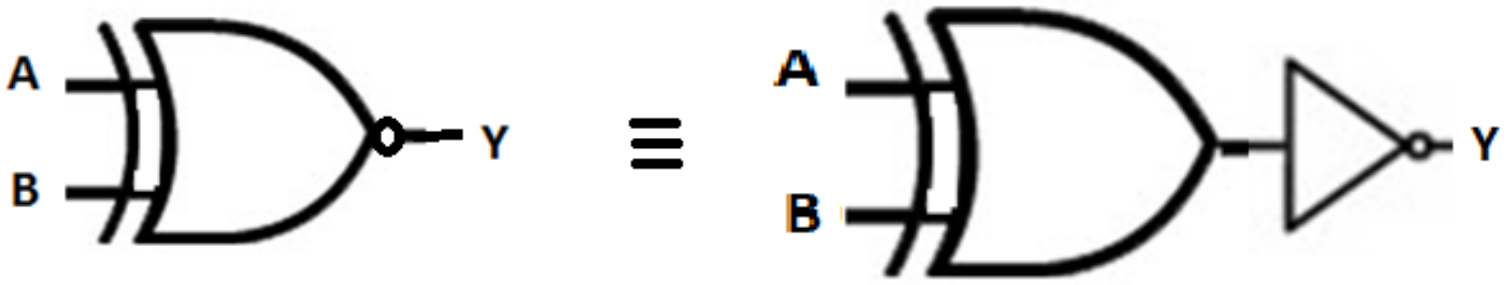
$Y = A\,(A' + B') + B.\,(A' + B')$

$Y = A.A' + A.B' + A'.B + B.B'$

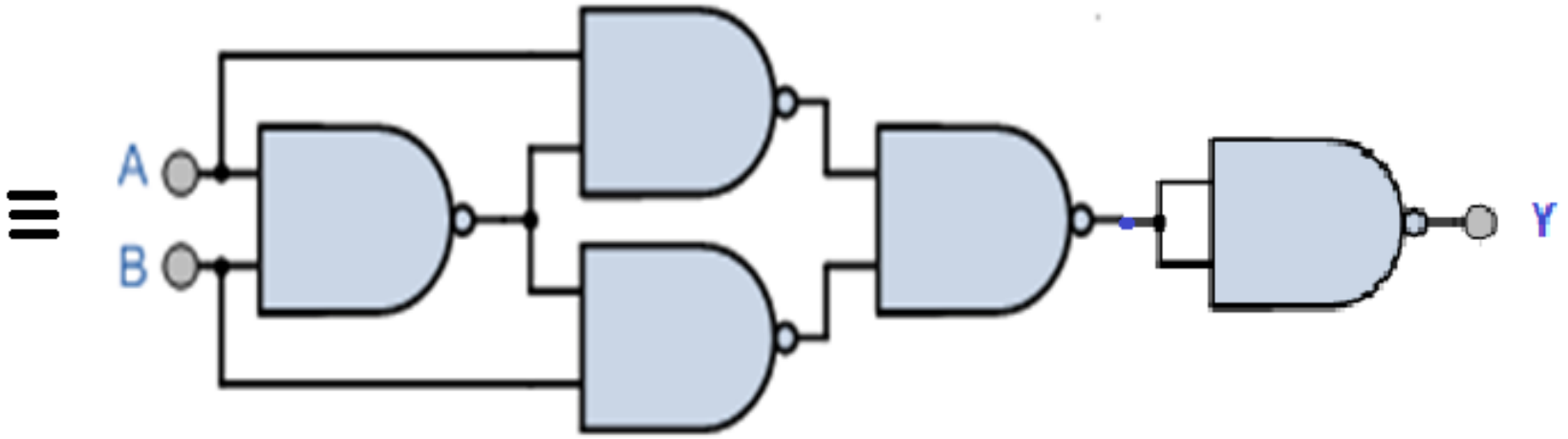
$Y = A.B' + A'.B$

Realization of Boolean expression using Universal Gates

❖ **XNOR Gate**:



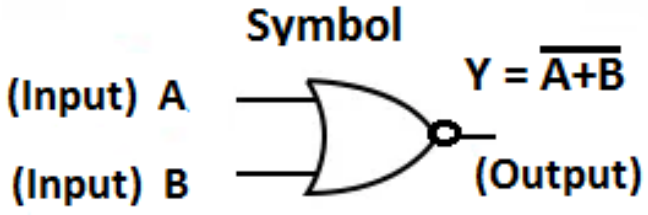
$Y = (A \oplus B)' = A \odot B$



Realization of Boolean expression using Universal Gates

❖ Realization of logic gates using NOR Gates:

Symbol

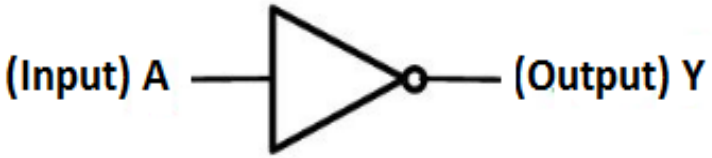


Truth Table

NOR		
Input		Output
A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

❖ NOT Gate:

Symbol



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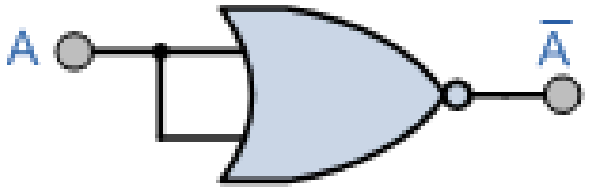
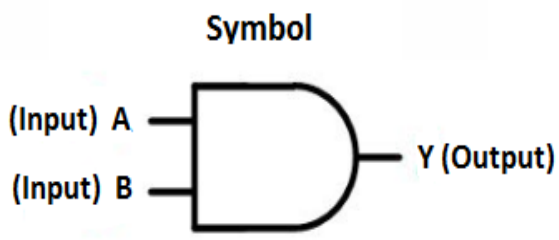


Y = (A + A)' = (A)' = A'

Realization of Boolean expression using Universal Gates

❖ AND Gate:



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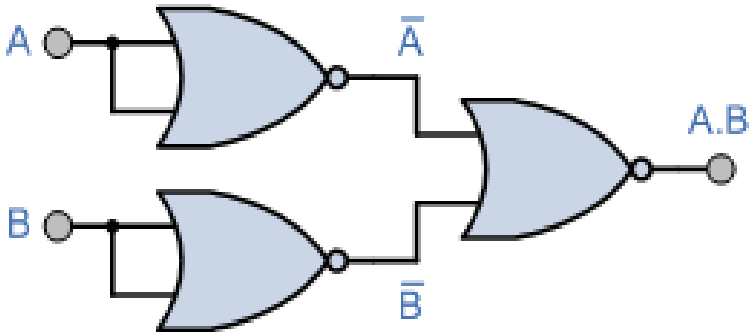
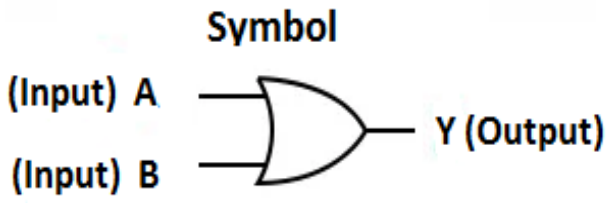


$$Y = ((A.B)')' = (A' + B')' = A.B$$

❖ OR Gate:



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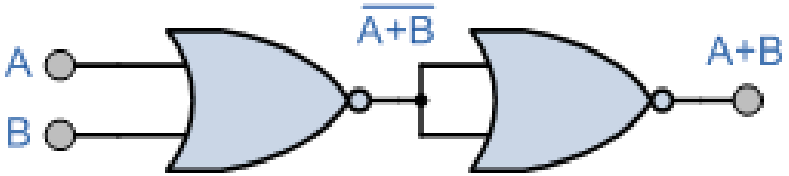


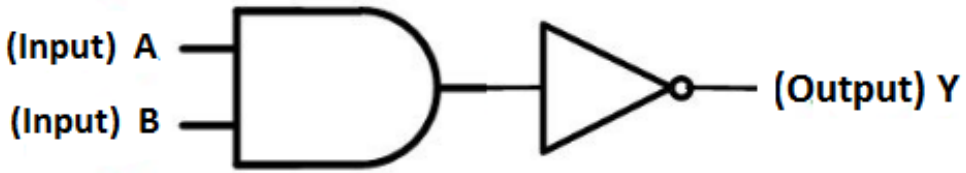
$$Y = ((A+B)')' = A + B$$

Realization of Boolean expression using Universal Gates

❖ NAND Gate:

Symbol

≡



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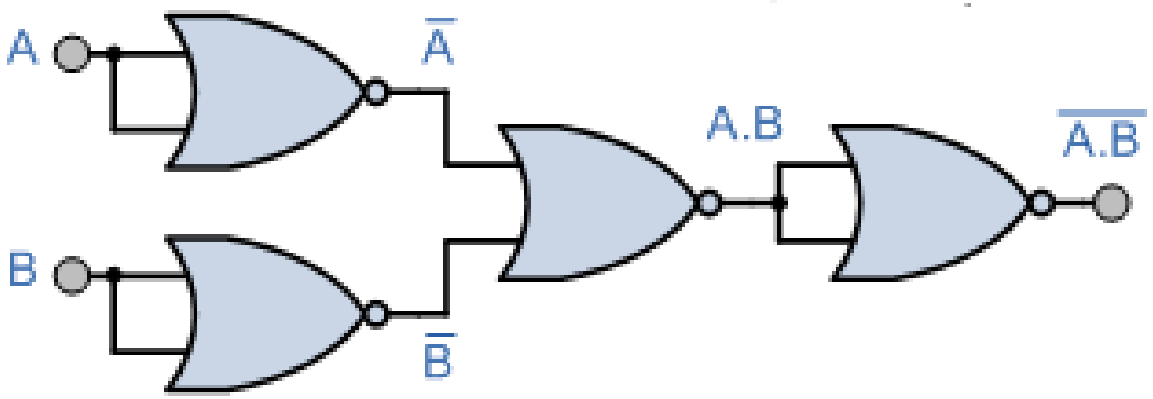
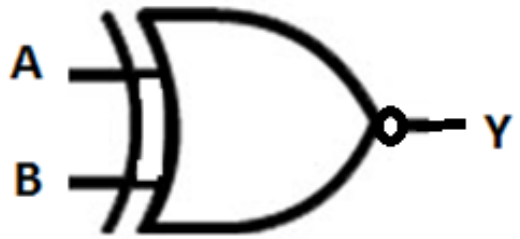


Realization of Boolean expression using Universal Gates

❖ **XNOR Gate**:



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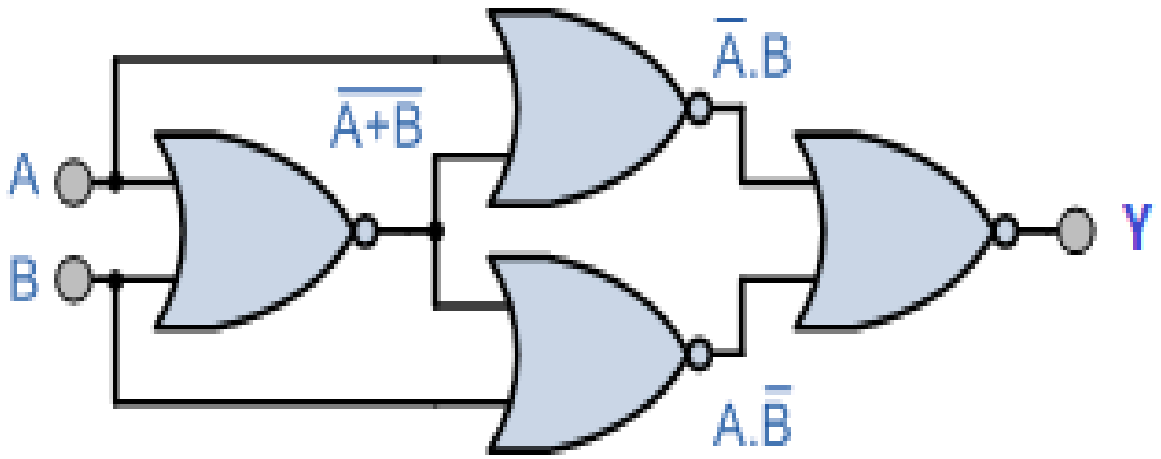


Y1 = ((A+B)’ + A)’ = (A+B). A’ = A’.B

Y2 = ((A+B)’ + B)’ = (A+B). B’ = A.B’

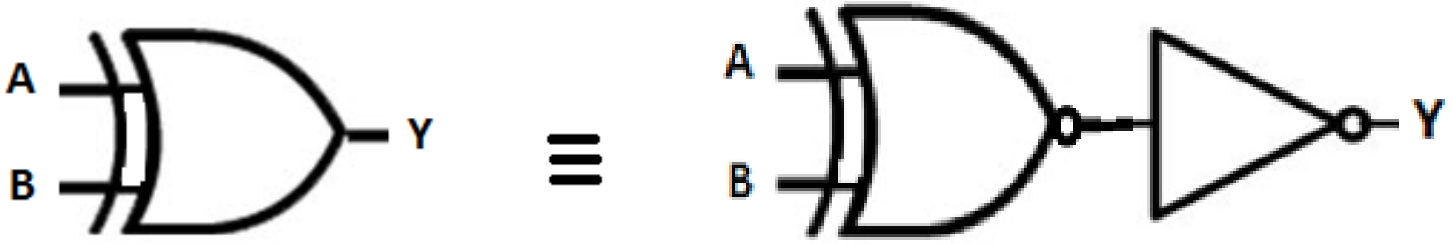
Y = (A’.B + A.B’)’ = (A’.B)’ . (A.B’)’ = (A + B’) . (A’ + B)

Y = A.B + A’.B’

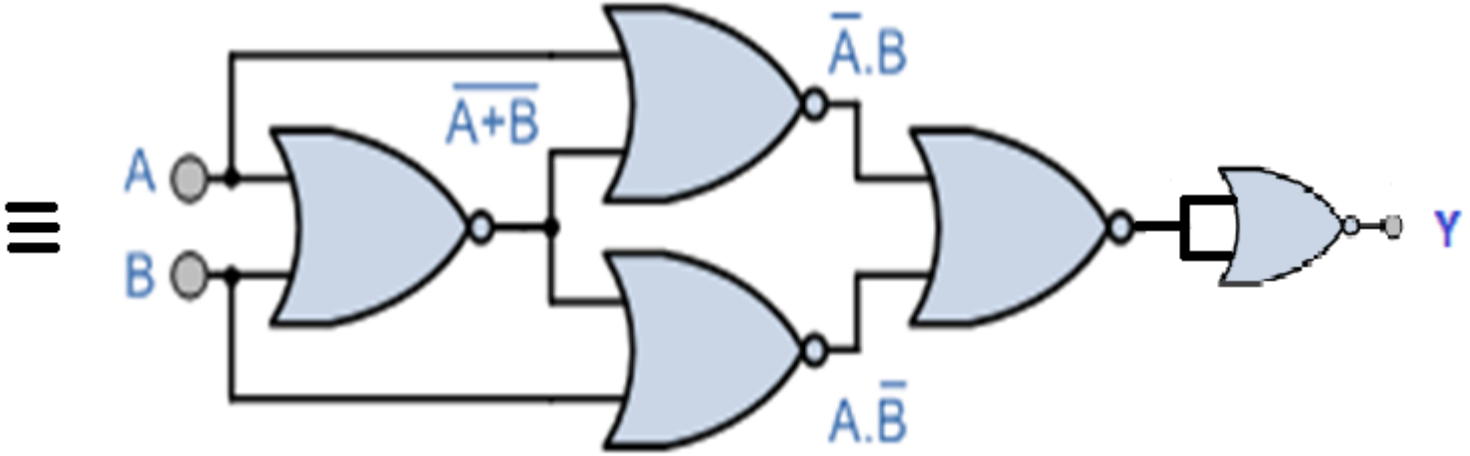
Y = A⊙B

Realization of Boolean expression using Universal Gates

❖ XOR Gate:



$Y = (A \odot B)' = A \oplus B$



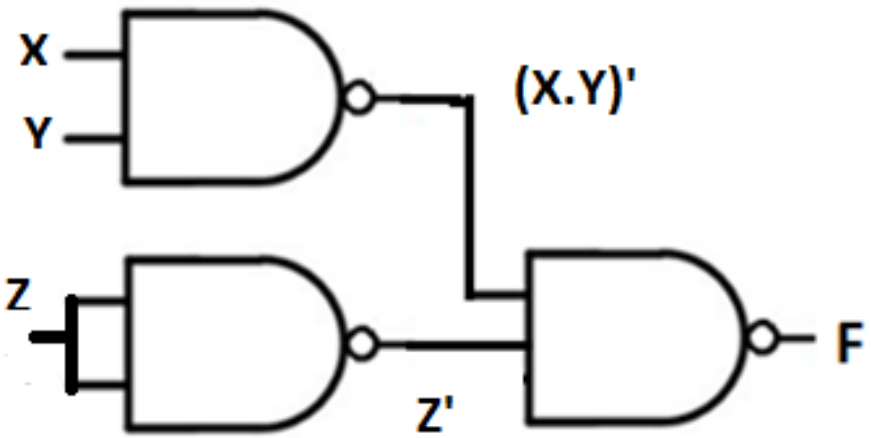
Realization of Boolean expression using Universal Gates

❖ **Implement the given function using NAND Gates only.**

F = X.Y + Z

F = ((X.Y + Z)’)’

F = ((X.Y)’ . Z’))’



Problems on Boolean algebra

❖(1) Simplify the given Boolean expression and implement using basic gates

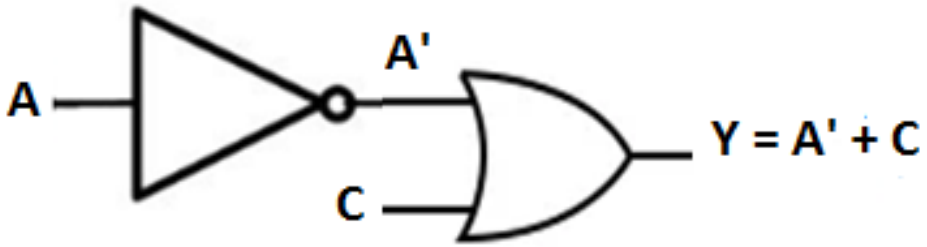
F = A.B.C + A’ + A. B’.C

F = A.C (B + B’)+ A’ where B + B’ = 1

F = A.C + A’ Distributive Law

F = (A’+A) . (A’+ C) A + B.C = (A+B) . (A+C)

F = A’ + C



Logic Diagram

Problems on Boolean algebra

❖**(2) Simplify and realize the given function using basic gates:**

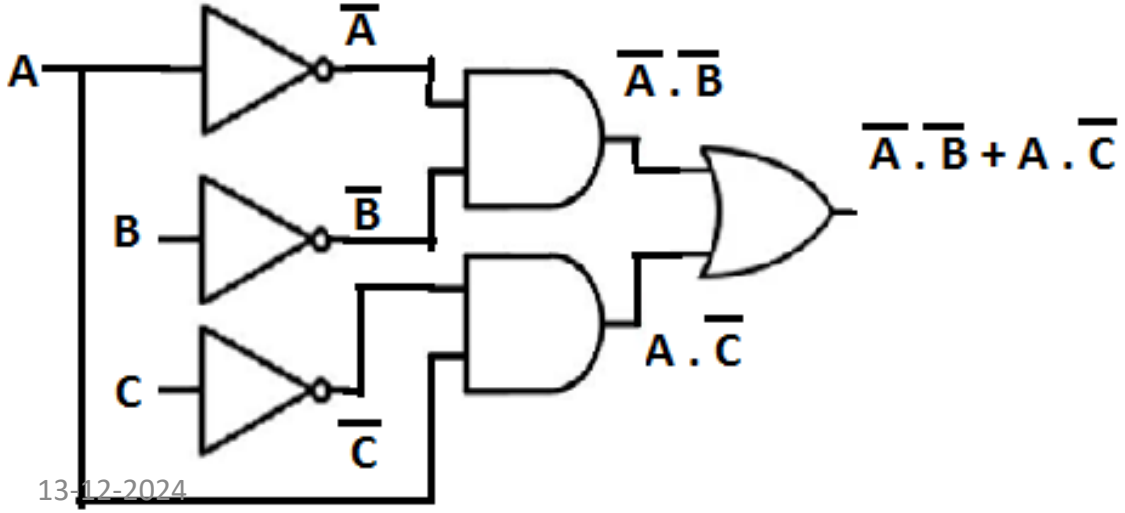
$Y = A'B'C' + AB'C' + A'B' + AC'$

$Y = B'C' (A' + A) + A'B' + AC'$

$Y = B'C' . (1) + A'B' + AC'$

By Consensus Theorem: **$Y = A'B' + AC'$**

$AB + \bar{A}C + BC = AB + \bar{A}C$



Problems on Boolean algebra

- **(3)Simplify and Implement the given function using NAND Gates only.**

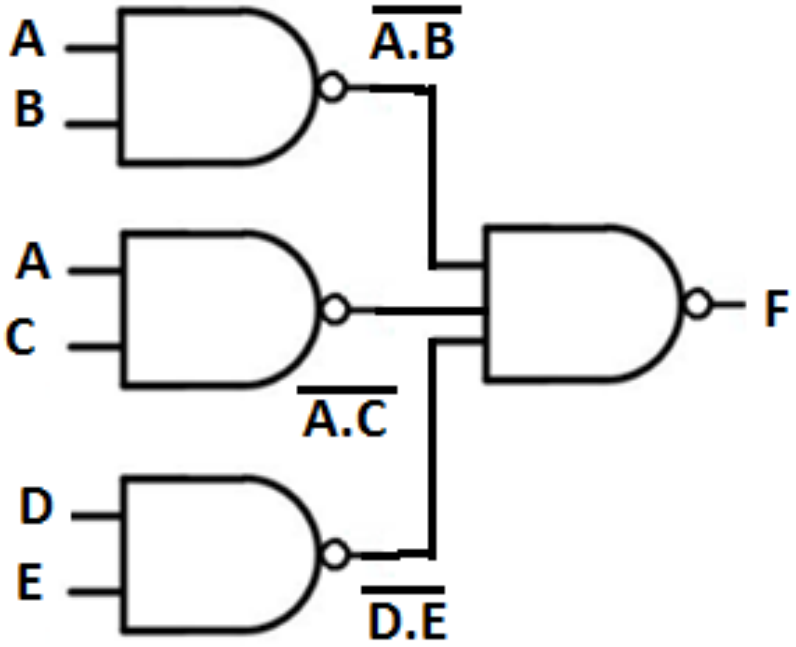
$F = A(B + C) + DE$

- SOP Form: $F = AB + AC + DE$

$F = \overline{\overline{(AB + AC + DE)}}$

$F = \overline{(\overline{A.B}) . (\overline{A.C}) . (\overline{D.E})}$

DeMorgan's Law



Logic Diagram

Problems on Boolean algebra

❖ **(4)Simplify the given Boolean Expression:**

$Y = A + A'.B + A'.B'.C + A'.B'.C'.D + A'.B'.C'.D'.E$

$Y = A + A' (B + B'.C + B'.C'.D + B'.C'.D'.E)$

Absorption Law: $A + A'.B = A + B$

$Y = A + B + B'.C + B'.C'.D + B'.C'.D'.E$

$Y = A + B + B' (C + C'.D + C'.D'.E)$

$Y = A + B + C + C'.D + C'.D'.E$

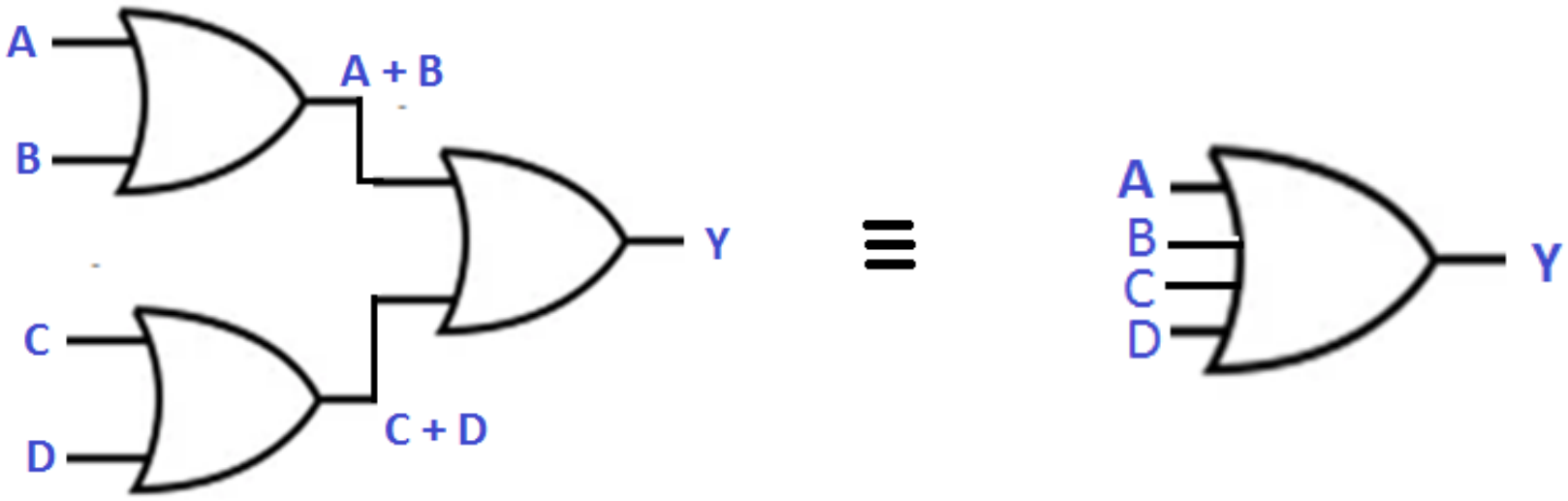
$Y = A + B + C + C' (D + D'.E)$

$Y = A + B + C + D + D'.E$

$\mathbf{Y = A + B + C + D + E}$

Problems on Boolean algebra

❖ **Logic Diagram**



❖ Evaluate the Boolean function Y = C + C'B + BA'

when A = 1, B = 0 and C = 1

Y = 1 + 1'.0 + 0.1' = 1 + 0 + 0

Y = 1

Problems on Boolean algebra

❖ **(5) Simplify the given Boolean expression and implement using Basic and NAND gates**

$F = AB + A(B+C) + B(B+C)$

$F = AB + AB + AC + BB + BC$ Distributive Law

$F = AB + AC + B + BC$

$F = AB + AC + B\,(1 + C)$

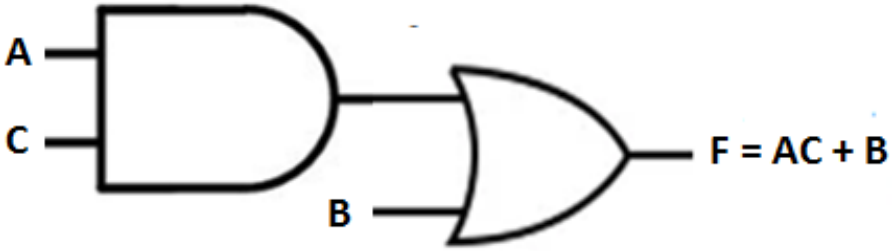
$F = AB + AC + B$

$F = AC + B(A + 1)$

$F = AC + B$

Problems on Boolean algebra

- F = A.C + B
- Using Basic Gates:

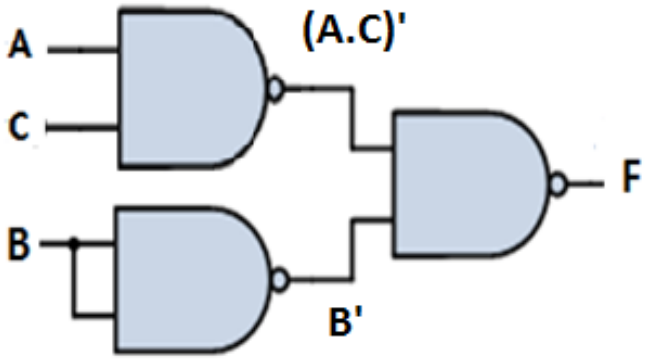


- Using NAND Gates:

F = AC + B

F = ((AC + B)')'

F = ((AC)' . B')'



Problems on Boolean algebra

❖ **(6) Simplify and realize the given function using: (i) Basic Gates: (ii) NAND Gates**

$Y = (A'.B + A' + A.B)'$

De Morgan's Theorem

$Y = (A'.B)' \ . \ (A')' \ . \ (A.B)'$

$Y = ((A')' + B') \ . \ (A) \ . \ (A' + B')$

$Y = (A + B') \ . \ ((A.A') + A.B'))$

$Y = (A + B') \ . \ (A.B')$

$Y = A.A.B' + A.B'.B'$

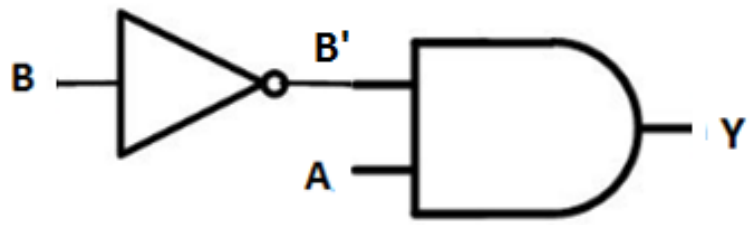
$Y = A.B' + A.B'$

$\mathbf{Y = A.B'}$

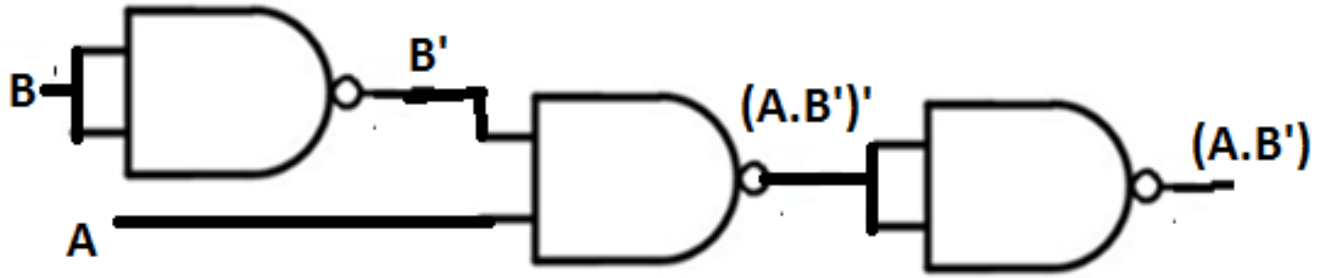
Problems on Boolean algebra

- (7) Y = A.B’

- Using Basic Gates:

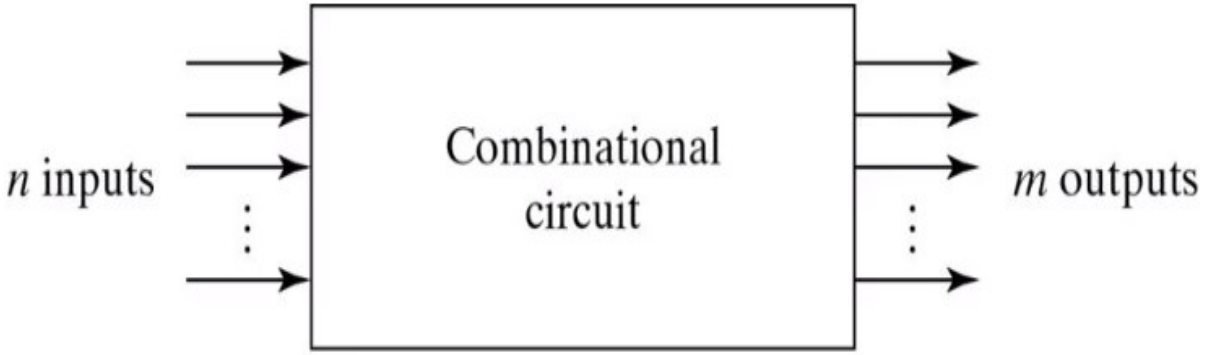


- Using NAND Gates:



Combinational Logic Circuits: Half Adder and Full adder

❖ **Combinational circuits** are constructed by interconnection of logic gates. whose outputs at any time are determined from only the present combination of inputs



❖ A combinational circuit performs an operation that can be specified logically by a set of **Boolean functions**

❖ Examples: Binary Adders, Multiplexers, etc.

❖ Half Adder

- x and y are the two binary inputs
- Sum (s) and Carry (c) are the two binary outputs

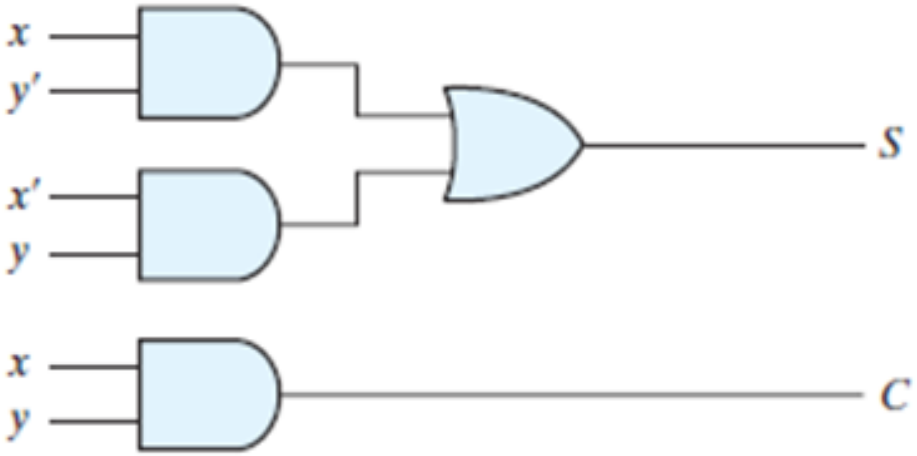
Boolean Expression:

$s = x'.y + x.y'$

$c = x.y$

Truth Table

x	y	C	S
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0



Logic Diagram

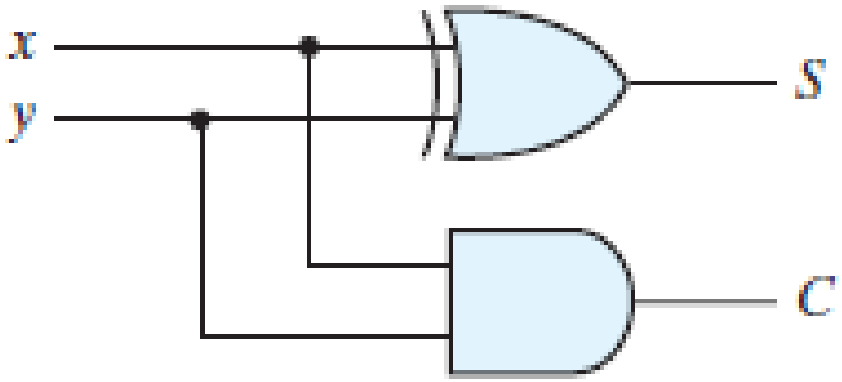
Combinational Logic Circuits: Half Adder and Full adder

❖ **Half Adder:** $s = x \oplus y$

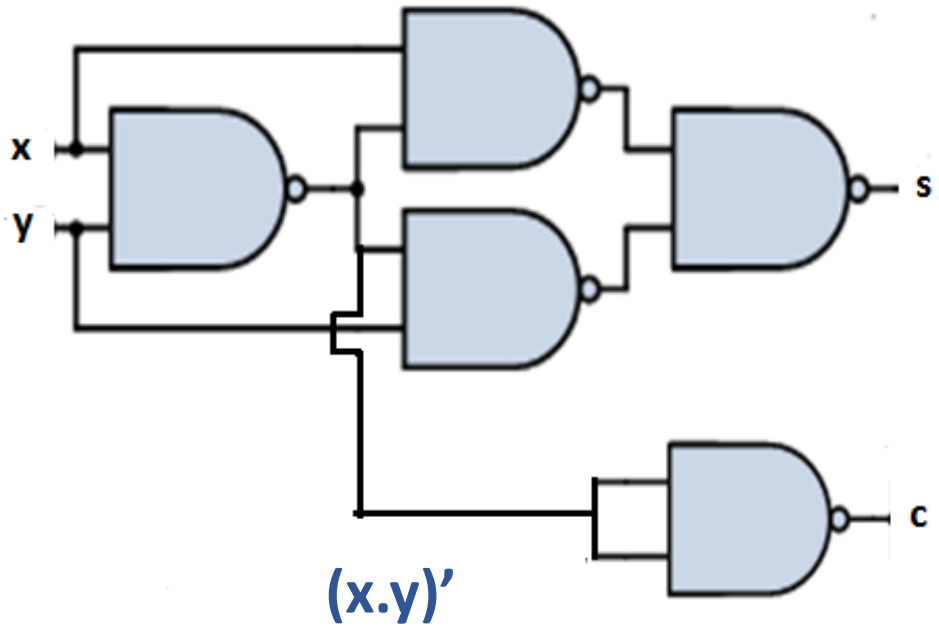
$c = x.y$

Sum expression: $s = x'.y + x.y'$

❖ **Half Adder using Logic Gates**



❖ **Half Adder using NAND Gates only**



Combinational Logic Circuits: Half Adder and Full adder

- Full Adder:
  - x, y and z are three binary inputs.
  - S is sum and C is carry outputs

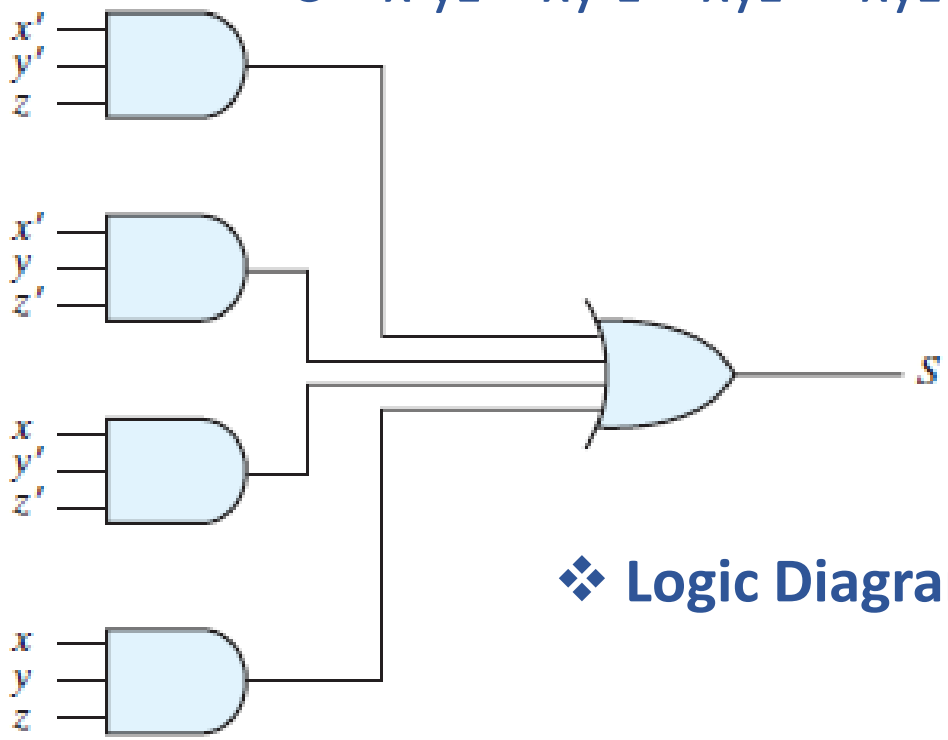
- Truth Table:

x	y	z	C	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

- Boolean Expression:

$S = x'y'z + x'yz' + xy'z' + xyz$

$C = x'yz + xy'z + xyz' + xyz$



- **Logic Diagram**

Reference: "Digital Design with an Introduction to Verilog HDL" M Morris Mano, Michale D Ciletti

- Full Adder:
  - **Carry Expression**:

$C = x'yz + xy'z + xyz' + xyz$

$C = x'yz + xy'z + xy\,(z'+z)$

$C = x'yz + xy'z + xy$

$C = x'yz + x(y'z + y)$ Absorption Law

$C = x'yz + x(z + y)$

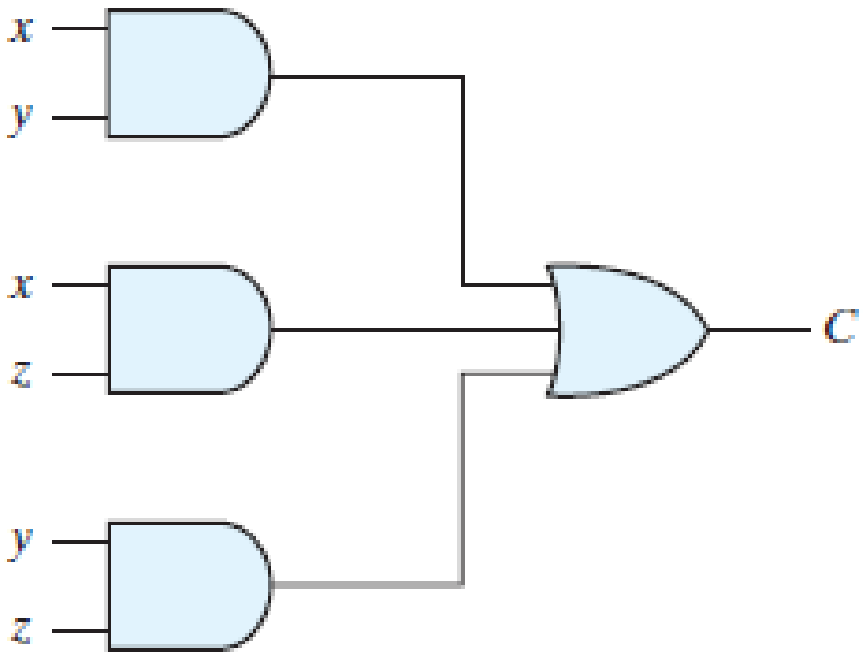
$C = x'yz + xz + xy$

$C = z(x'y + x) + xy$

$C = z(y + x) + xy$

$\mathbf{C = yz + xz + xy}$

- **Logic Diagram**



Reference: "Digital Design with an Introduction to Verilog HDL" M Morris Mano, Michale D Ciletti

Implement Full adder using two Half Adder

- **Boolean Expression for Sum:**

$S = x'y'z + x'yz' + xy'z' + xyz$

$S = x'(y'z + yz') + x(y'z' + yz)$

$S = x'(y \oplus z) + x((y \oplus z)')$

$\mathbf{S = x \oplus (y \oplus z)}$

- **Boolean Expression for Carry:**

$C = x'yz + xy'z + xyz' + xyz$

$C = z.(x'y + xy') + xy(z' + z)$

$C = z.(x \oplus y) + xy.(1)$

$\mathbf{C = (x \oplus y).z + xy}$

Reference: "Digital Design with an Introduction to Verilog HDL" M Morris Mano, Michale D Ciletti

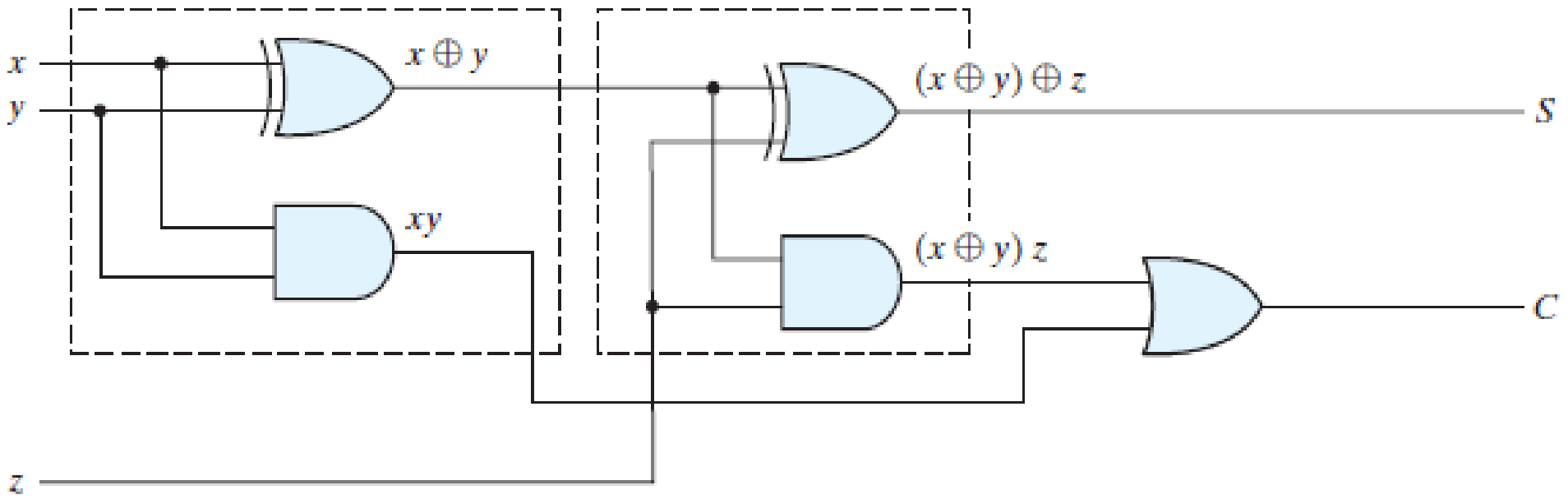
Implement Full adder using two Half Adder

- Full Adder Boolean Expression:

$$S = (x \oplus y) \oplus z$$

$$C = (x \oplus y).z + x.y$$

- Implementation of full adder with two half adders and an OR gate



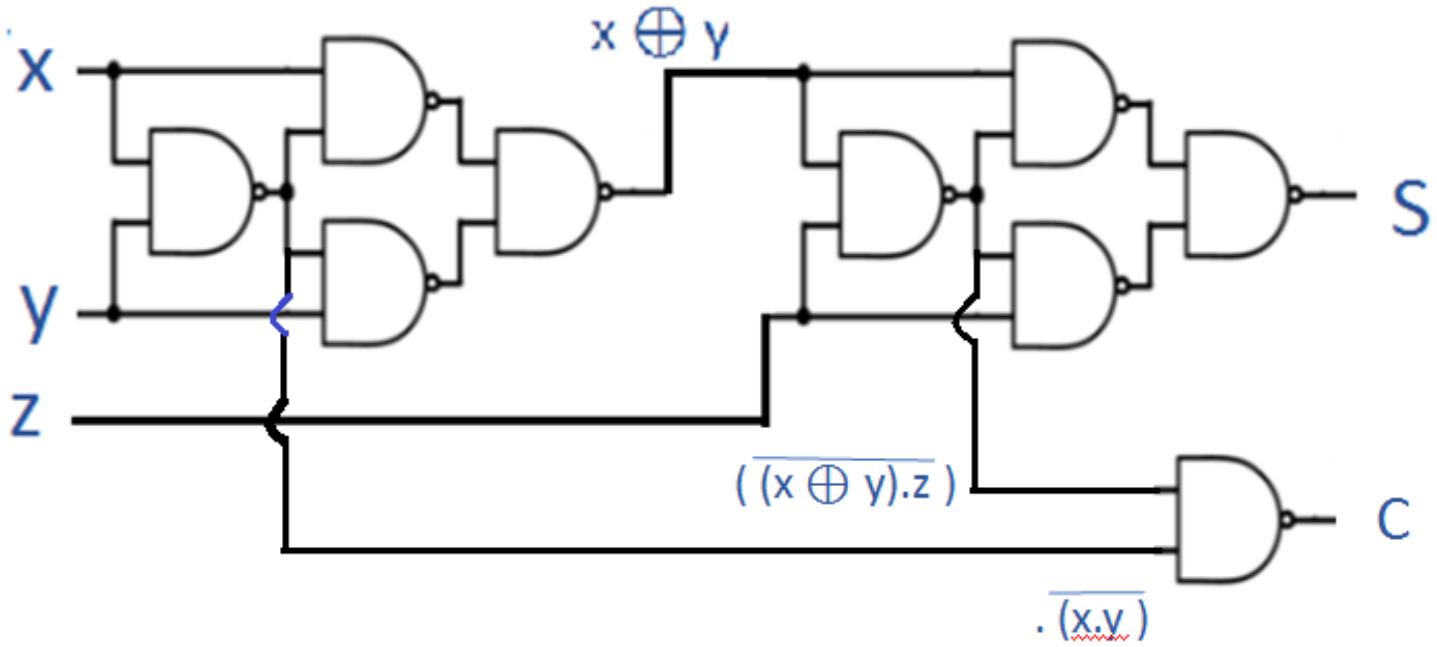
Reference: "Digital Design with an Introduction to Verilog HDL" M Morris Mano, Michale D Ciletti

Implement Full adder using NAND only

- Boolean Expression: $S = (x \oplus y) \oplus z$

  $C = (x \oplus y).z + x.y$

- Full adder circuit using NAND Gates

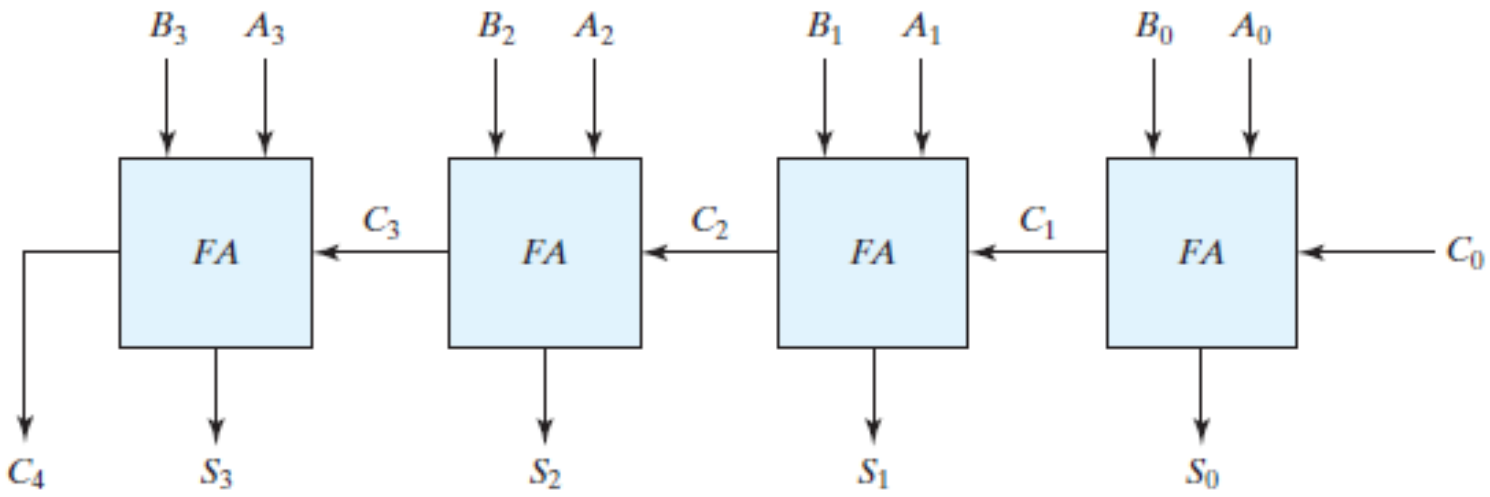


$$C = \overline{\overline{((x \oplus y).z + x.y)}}$$

$$C = \overline{\overline{(\overline{(x \oplus y).z})}.\overline{(x.y)}}$$

❖ Four-bit adder

Using four Full adder Ripple adder circuit is constructed.



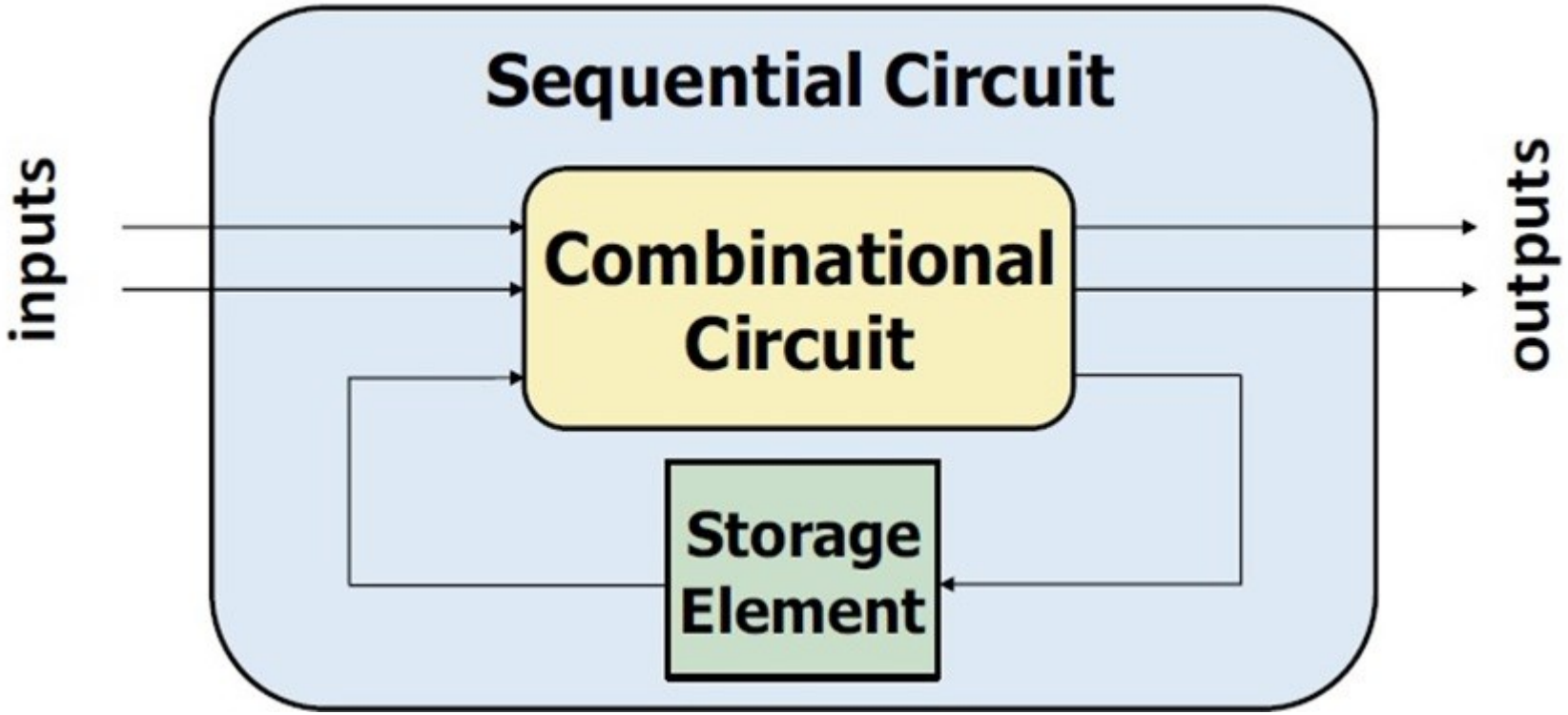
❖ Example

```
      1110
A =   1101
+ B = 0111
      -----
      10100
```

Reference: "Digital Design with an Introduction to Verilog HDL" M Morris Mano, Michale D Ciletti

Introduction: Sequential Circuits

- Combinational Circuit output depend **only** on **present** input.
- We want circuits that produce the output depending on the **current** and **past** input values - Circuits with **memory**.
- How do we design such a circuit that **stores information**?



Types of sequential circuits

- Sequential Circuits are of **two** types

1. <u>Synchronous Circuits:</u>

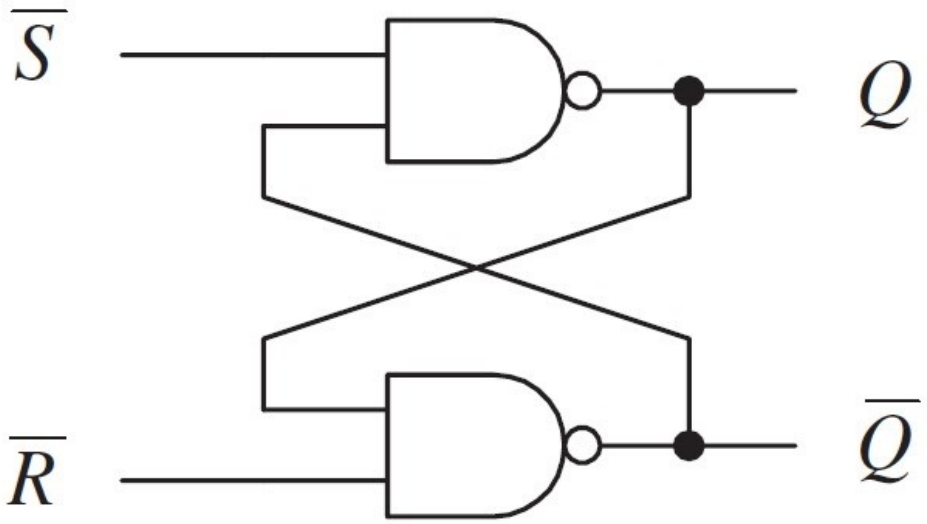
- In synchronous sequential circuits, the state of the device changes only at discrete times in response to a **clock pulse**.

2. <u>Asynchronous Circuits:</u>

- Asynchronous circuit is **not synchronized** by a clock signal; the outputs of the circuit change directly in response to the change in the inputs.

Types of sequential circuits – S'R' latch by Using NAND Gates

Circuit Diagram

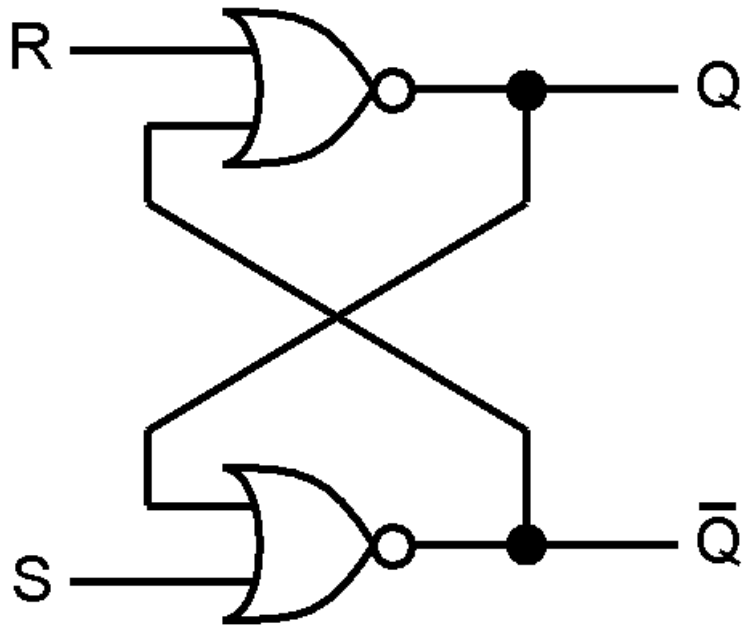


Function Table

INPUTS		OUTPUTS		Status of S'R' Latch
S'	R'	Q	Q'	
0	0	1	1	FORBIDDEN
0	1	1	0	SET
1	0	0	1	RESET
1	1	Q_{-1}	Q'_{-1}	PREVIOUS STATE

Types of sequential circuits – RS latch by Using NOR Gates

Circuit Diagram

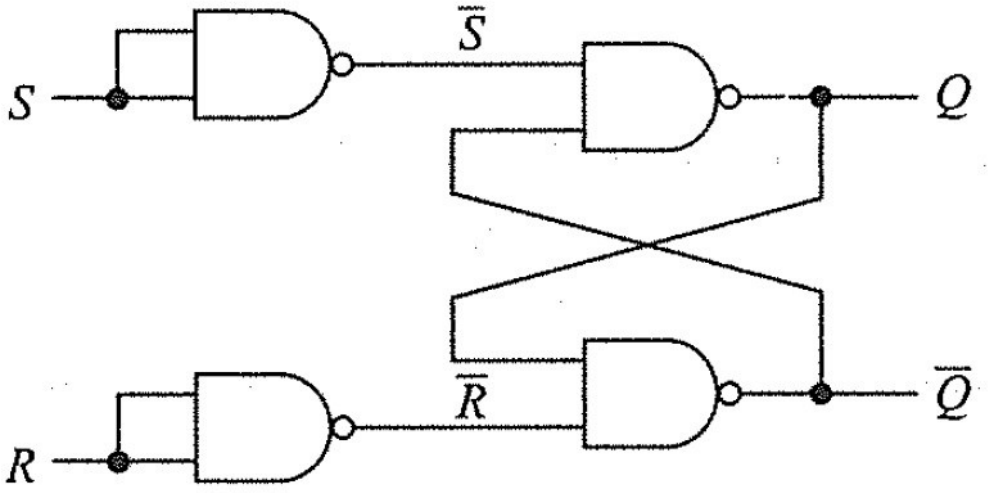


Function Table

INPUTS		OUTPUTS		Status of RS Latch
R	S	Q	Q’	
0	0	Q_{-1}	Q'_{-1}	PREVIOUS STATE
0	1	1	0	SET
1	0	0	1	RESET
1	1	0	0	FORBIDDEN

Types of sequential circuits – SR latch by Using NAND Gates

Circuit Diagram

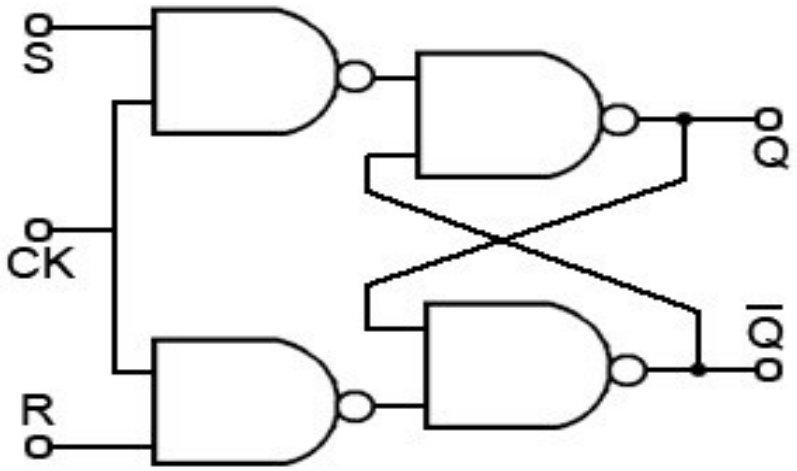


Function Table

INPUTS		OUTPUTS		Status of SR Latch
S	R	Q	Q’	
0	0	Q_{-1}	Q'_{-1}	PREVIOUS STATE
0	1	0	1	RESET
1	0	1	0	SET
1	1	1	1	FORBIDDEN

The S-R (Set - Reset) Flip – Flop / Gated R-S latch

Logic Diagram



Function Table

INPUTS			OUTPUTS		Status of SR Flip-Flop
CK	S	R	Q	Q’	
0	X	X	Q_{-1}	Q'_{-1}	PREVIOUS STATE
1	0	0	Q_{-1}	Q'_{-1}	PREVIOUS STATE
1	0	1	0	1	RESET
1	1	0	1	0	SET
1	1	1	1	1	FORBIDDEN

Conclusion Remarks:

1. Flip – flops are the **building blocks** of sequential circuits.
   But these are built from **latches**.

2. Flip- flops **continuously checks** its inputs and changes its outputs
   correspondingly only at time instant determined by the **clock signal**.

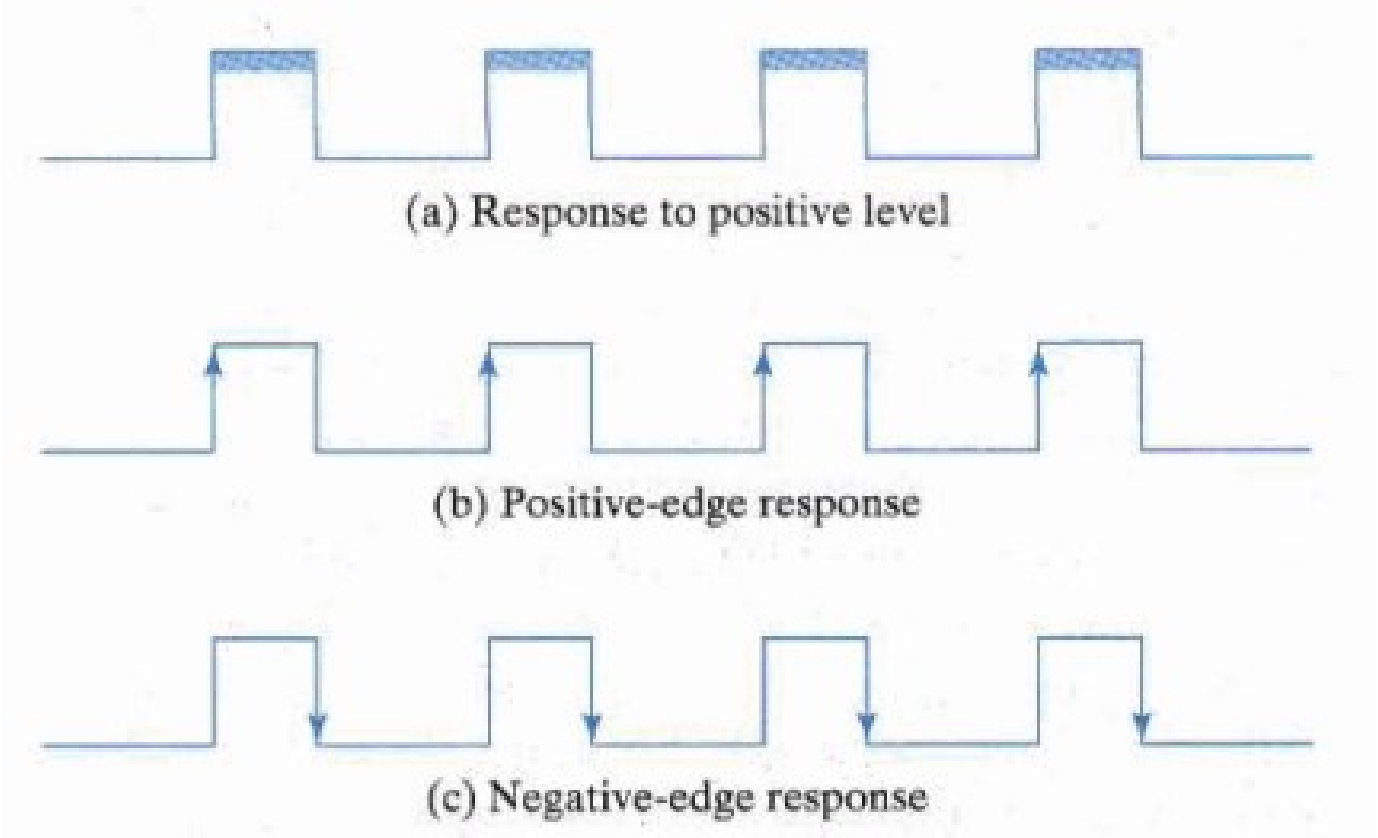
3. Flip – flops is **sensitive** to signal change. They transfer data only at single time instant and data can't be changed till next signal change.
   - Therefore they are used as **registers**.

4. It is an edge triggered circuit, means that the output and the next state input changes, when there's a change in the clock pulse whether it can may be **POSITIVE (up)** or **NEGATIVE (**

Comparison between Flip-flop and Latch

Flip-Flop	Latch
Flip-flop utilizes an edge triggering approach.	Latch follows a level triggering approach.
The clock signal is present.	The clock signal is absent.
You can design it using Latches along with a clock.	You can design it using Logic gates.
Flip-flop is sensitive to the applied input and the clock signal.	Latches are sensitive to the applied input signal- only when enabled.
It has a slow operating speed.	It has comparatively fast operating speed.
You can classify a flip-flop into a synchronous or asynchronous flip-flop.	A user cannot classify the Latch this way.
A flip-flop checks the inputs. It only changes the output at times defined by any control signal like the clock signal.	The latch responds to the changes in inputs continuously as soon as it checks the inputs.
A flip-flop is synchronous. It works based on the clock signal.	A latch is asynchronous. It does not work based on the time signal.

Clock Response in Flip – Flop:

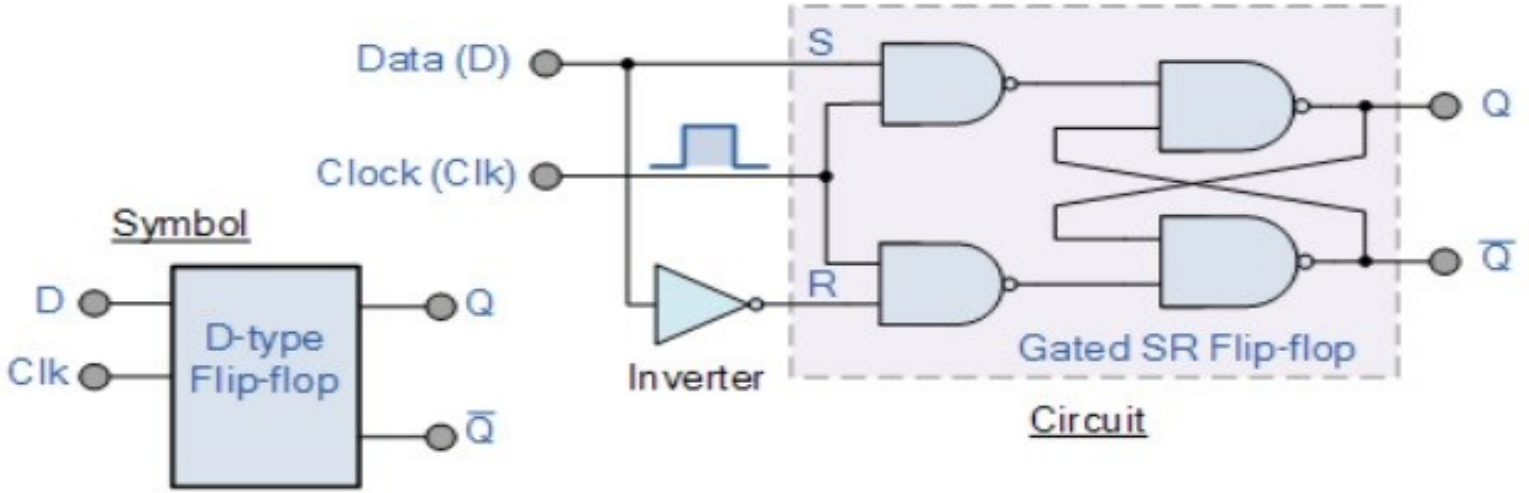


Flip-Flops will change the Output when the clock remains as logic 1 as shown in figure (a)

Flip-Flops will change the Output when the clock changes from logic 0 to Logic 1 as shown in figure (b)

Flip-Flops will change the Output when the clock changes from logic 1 to Logic 0 as shown in figure (c)

The Data (D) Flip – Flop:



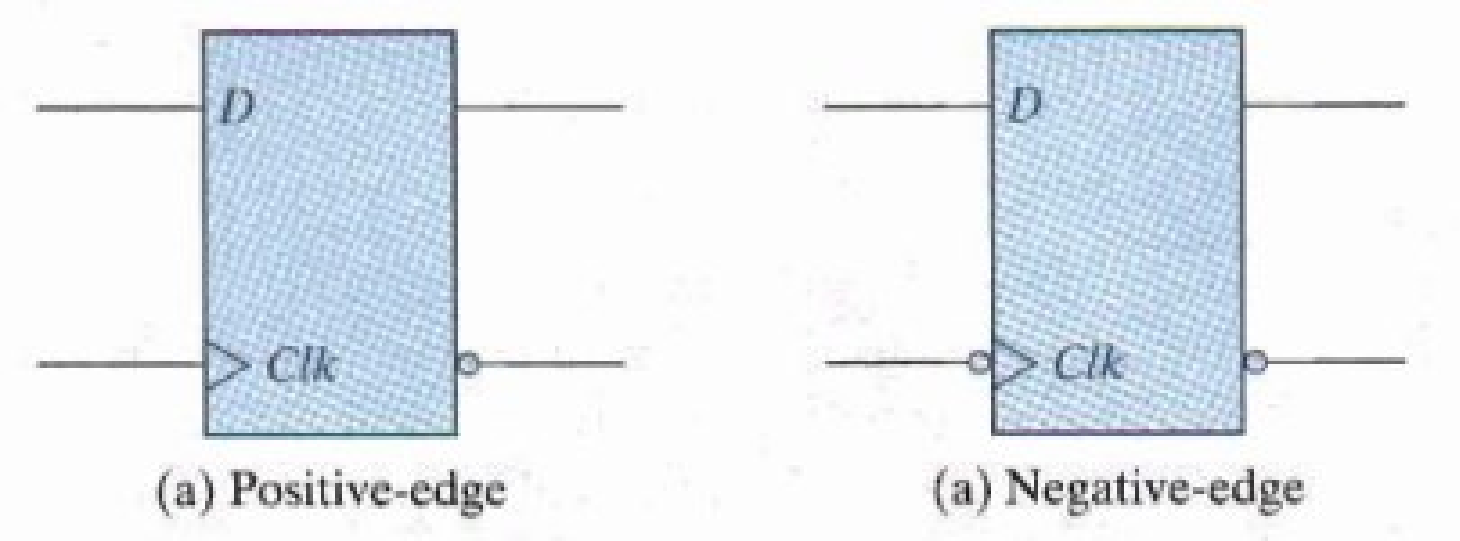
- The **D Flip Flop** is by far the most important of the clocked flip-flops as it ensures that ensures that inputs **S** and **R** are **never equal** to one at the same time.
- The **D Flip Flop** are constructed from a SR flip-flop with an **inverter** added between the **S** and the **R** inputs to allow for a single D (Data) input.

D Flip – Flop (Characteristic Table) :

Clk	D	Q		Description
↓ » 0	X	Q	$\overline{Q}$	Memory no change
↑ » 1	0	0	1	Reset Q » 0
↑ » 1	1	1	0	Set Q » 1

- The D Flip-flop will store and output whatever logic level is applied to its **DATA** input.
- Once the clock input goes LOW the “set” and “reset” inputs of the flip-flop are both held at logic level “1”, so it will not change its state.
- ↓ and ↑ indicates direction of clock pulse as it is assumed D-type flip flops are edge triggered.

Positive & Negative Edge Triggered 'D' Flip – Flop:

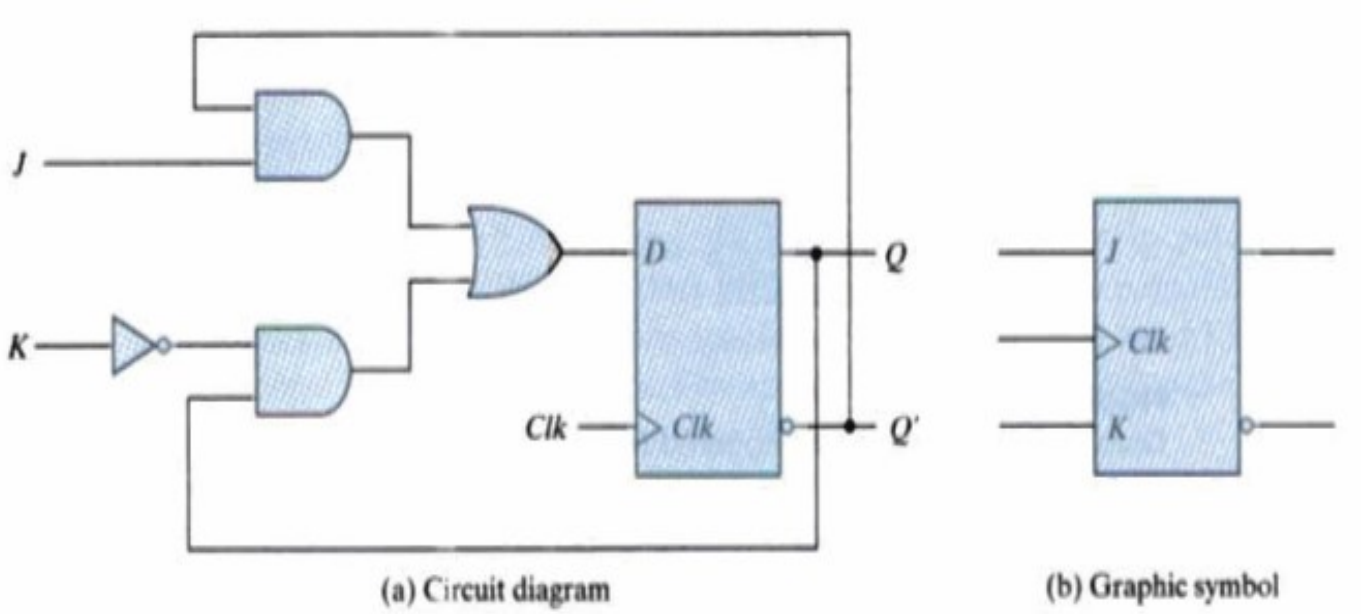


(a) Positive-edge (a) Negative-edge

In D Flip-Flops, Absence of the bubble in front of the Clk indicates Positive edge triggered as shown in figure (a)

In D Flip-Flops, Presence of the bubble in front of the Clk indicates Positive edge triggered as shown in figure (b)

JK Flip – Flop using D flip flop

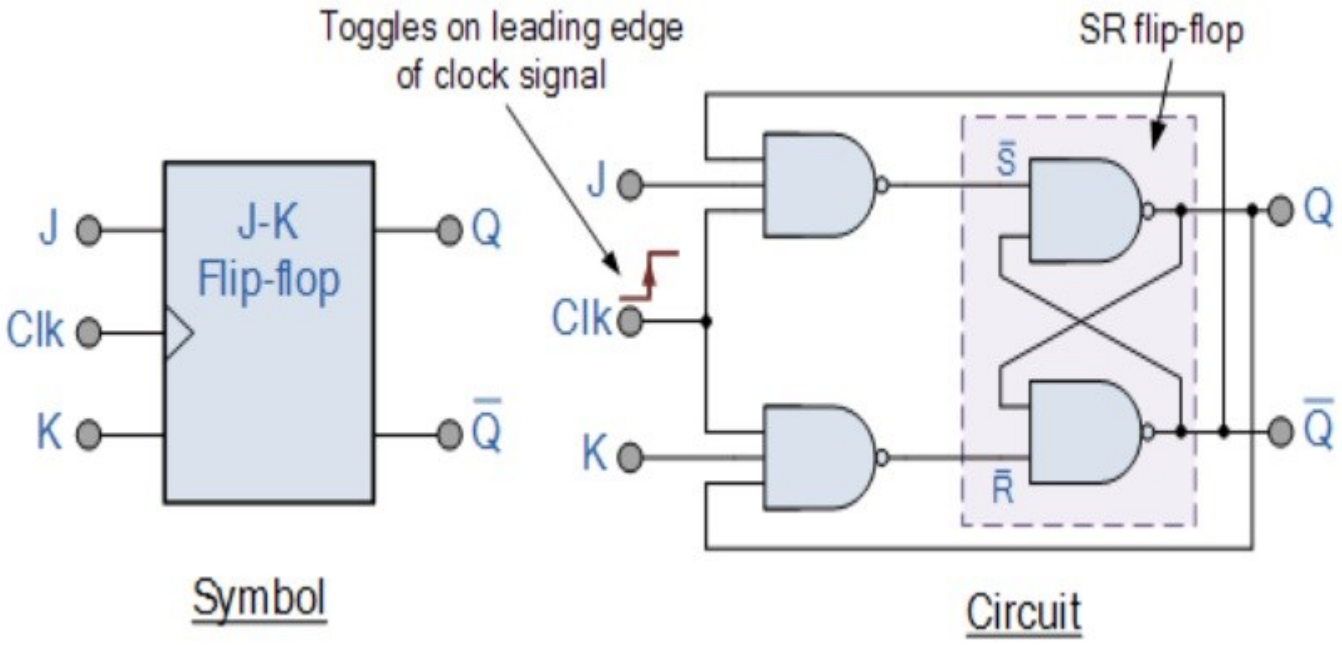


(a) Circuit diagram (b) Graphic symbol

INPUTS			OUTPUTS		Status of JK Flip-Flop
CLK	J	K	Q	Q'	
0	X	X	Q_{-1}	Q'_{-1}	PREVIOUS STATE
1	0	0	Q_{-1}	Q'_{-1}	PREVIOUS STATE
1	0	1	0	1	RESET
1	1	0	1	0	SET
1	1	1	Q'_{-1}	Q_{-1}	TOGGLE

- The Inputs are **J-K** along with the Clk
  - J-K inputs comes after its inventors **Jack Kilby**.

JK Flip – Flop using NAND Gates only



INPUTS			OUTPUTS		Status of JK Flip-Flop
CLK	J	K	Q	Q'	
0	X	X	Q_{-1}	Q'_{-1}	PREVIOUS STATE
1	0	0	Q_{-1}	Q'_{-1}	PREVIOUS STATE
1	0	1	0	1	RESET
1	1	0	1	0	SET
1	1	1	Q'_{-1}	Q_{-1}	TOGGLE

- The **S** and **R** inputs of SR slip-flops are now replaced by **J-K** inputs.
  - J-K inputs comes after its inventors **Jack Kilby**.
  - Then this equates to: **J = S** and **K = R**.

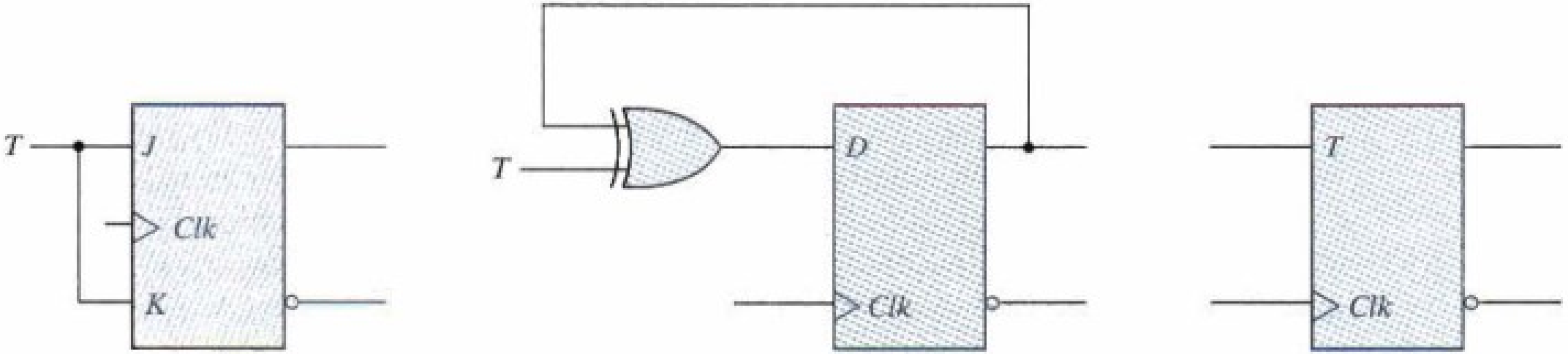
Conclusion Remarks :

- **JK flip-flop** is a sequential circuit, whose state transitions are **synchronized** with the **clock pulse** (+ve / -ve) edge triggered.

- In **JK flip-flop** all the rows are a valid state in the characteristic table, also when J=K=1, the output toggles, **Toggle state**.

- **D flip-flop** is a sequential circuit, whose output is same as the input and hence also called as **transparent flip-flop**.

T Flip – Flop:



(a) From *JK* flip-flop (b) From *D* flip-flop (c) Graphic symbol

T Flip-Flop using JK Flip-Flop & D Flip-Flop

- T Flip-Flop is a **synchronous** device, where high to low or low to high transitions is passed through **clock signal** which **changes** the output state of Flip-Flop.

T Flip – Flop: - Function Table

INPUTS		OUTPUTS		Status of T Flip-Flop
CLK	T	Q	Q’	
0	X	Q_{-1}	Q'_{-1}	PREVIOUS STATE
1	0	Q_{-1}	Q'_{-1}	PREVIOUS STATE
1	1	Q'_{-1}	Q_{-1}	TOGGLE

Advantages of T flip-flop:

- These Flip-Flops has a **toggle input** and a **clock**. When a clock is triggered it **inverts** the value of Flip-Flops.

- They are used for designing the **counters**

Registers:

- A *register* is a group of flip-flops, each one of which shares a common clock and is capable of storing one bit of information.
- An *n* -bit register consists of a group of *n* flip-flops capable of storing *n* bits of binary information.
- In addition to the flip-flops, a register may have combinational gates that perform certain data-processing tasks.
- In its broadest definition, a register consists of a group of flip-flops together with gates that affect their operation.
- The flip-flops hold the binary information, and the gates determine how the information is transferred into the register.

4-bit Register:

- Various types of registers are available commercially.
- The simplest register is one that consists of only flip-flops, without any gates.
- Following Figure (next slide) shows such a register constructed with four *D* -type flip-flops to form a four-bit data storage register.
- The common clock input triggers all flip-flops on the positive edge of each pulse, and the binary data available at the four inputs are transferred into the register.
- The four outputs can be sampled at any time to obtain the binary information stored in the register.
- The input Clear goes to the active-low R (reset) input of all four flip-flops. When this input goes to 0, all flip-flops are reset asynchronously.
- The R inputs must be maintained at logic 1 (i.e., de-asserted) during normal clocked operation.

4-bit Register:

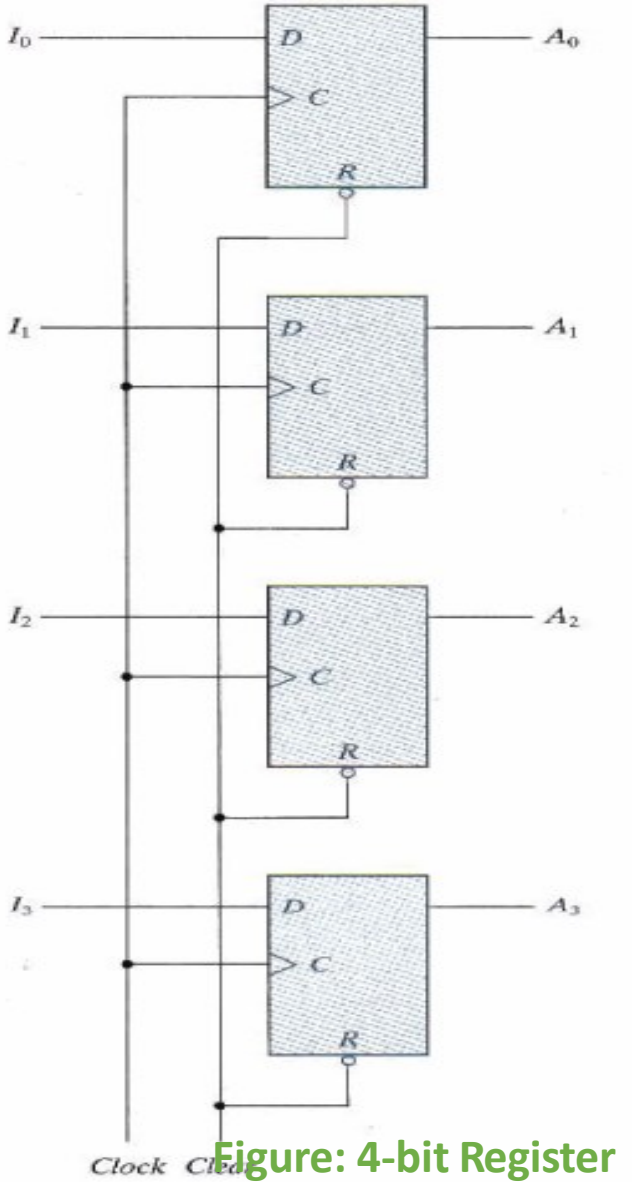


Figure: 4-bit Register

- The transfer of new information into a register is referred to as *loading or updating* the register.
- If all the bits of the register are loaded simultaneously with a common clock pulse, we say that the loading is done *in parallel* .
- A clock edge applied to the *C* inputs of the register of Figure, will load all four inputs in parallel.
- In this configuration, if the contents of the register must be left unchanged, the inputs must be held constant or the clock must be inhibited from the circuit.

SHIFT REGISTERS (SISO)

- A register capable of shifting the binary information held in each cell to its neighboring cell, in a selected direction, is called a *shift register*.
- The logical configuration of a shift register consists of a chain of flip-flops in cascade, with the output of one flip-flop connected to the input of the next flip-flop.
- All flip-flops receive common clock pulses, which activate the shift of data from one stage to the next.
- There are four different types of shift registers:
  - Serial In Serial Out (SISO)
  - Serial In Parallel Out (SIPO)
  - Parallel In Serial Out (PISO)
  - Parallel In Parallel Out (PIPO)

REGISTERS (SISO)

- The simplest possible shift register (SISO) is one that uses only flip-flops, as shown in the following Figure .
- The output of a given flip-flop is connected to the *D* input of the flip-flop at its right.
- This shift register is unidirectional (left-to-right).
- Each clock pulse shifts the contents of the register one bit position to the right.

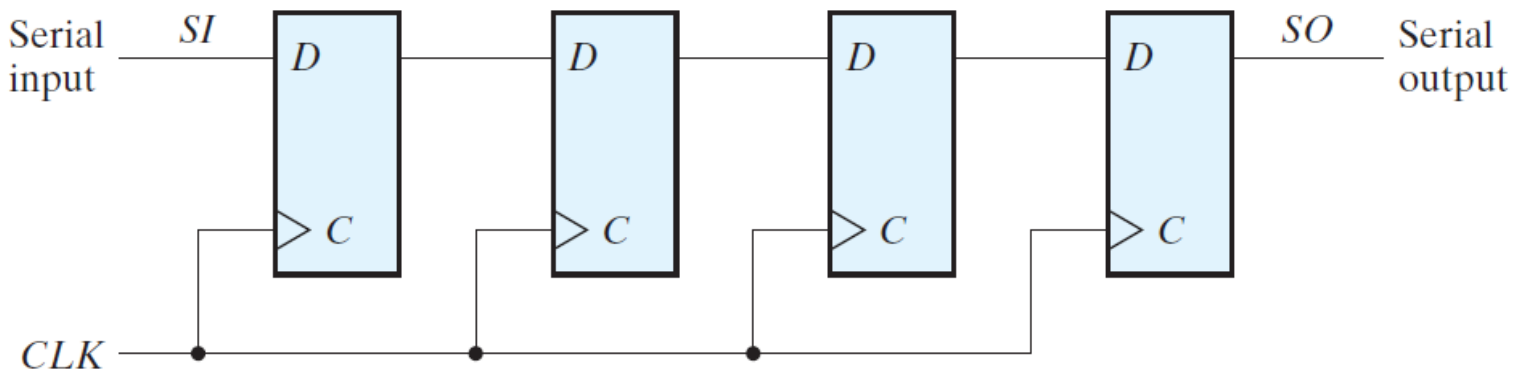
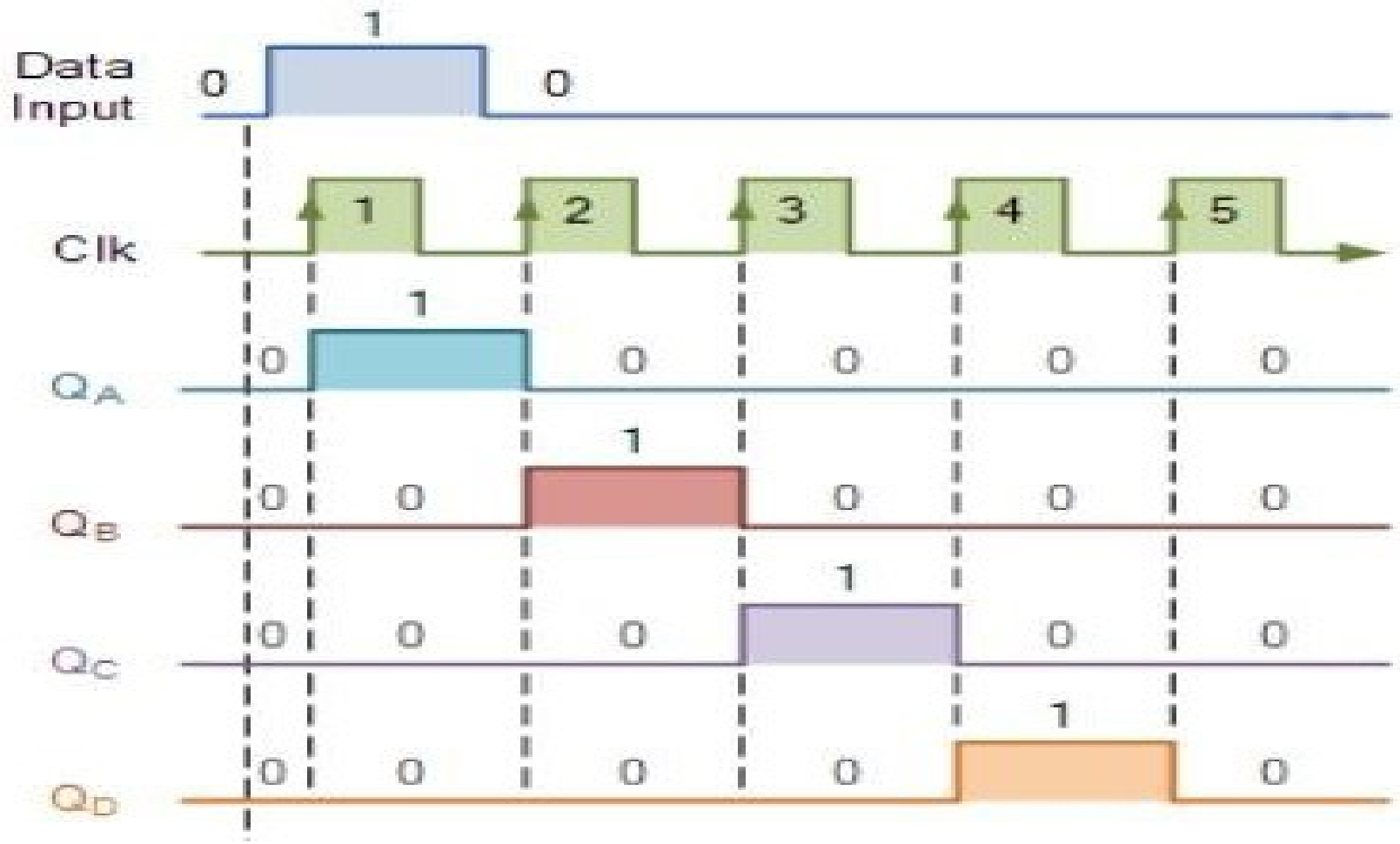


FIGURE: Four-bit shift register



Timing Diagram for SISO register

4-bit Serial Input Serial Output (SISO) register:

Clock Pulse No	QA	QB	QC	QD
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	0	0	1	0
4	0	0	0	1
5	0	0	0	0

Data movement through a shift register

4-bit Serial Input Serial Output (SISO) register:

Example:

The register is shifted six times to the right with the serial input being 0110. What is the content of the register after each shift?

Answer:

0110; 0011; 1001; 1100; 0110; 0011.

4-bit Serial Input Serial Output (SISO) register:

Example:

The contents of a four-bit register is initially 0110. The register is shifted six times to the right with the serial input being 1011100. What is the content of the register after each shift?

Answer:

0110; 0011; 0001; 1000; 1100; 1110; 0111

	Data	QA	QB	QC	QD
	initial	0	1	1	0
1st	0	0	0	1	1
2nd	0	0	0	0	1
3rd	1	1	0	0	0
4th	1	1	1	0	0
5th	1	1	1	1	0
6th	0	0	1	1	1
7th	1	1	0	1	1

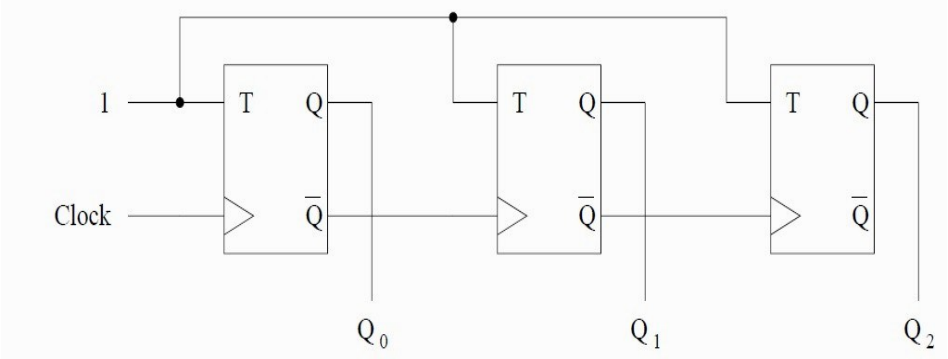
Synchronous and Asynchronous counters (Introduction):

- A register (group of flip-flops) that goes through a prescribed sequence of states upon the application of input pulses is called a *counter* .
- The input pulses may be clock pulses, or they may originate from some external source and may occur at a fixed interval of time or at random.
- The sequence of states may follow the binary number sequence or any other sequence of states.
- A counter that follows the binary number sequence is called a *binary counter* .
- An n -bit binary counter consists of n flip-flops and can count in binary from 0 through 2^n - 1.

Synchronous and Asynchronous counters (Introduction):

- Counters are available in two categories: ripple (or asynchronous) counters and synchronous counters.
- In a ripple counter, a flip-flop output transition serves as a source for triggering other flip-flops.
- In other words, the *C* input of some or all flip-flops are triggered, not by the common clock pulses, but rather by the transition that occurs in other flip-flop outputs.
- In a synchronous counter, the *C* inputs of all flip-flops receive the common clock.

3 bit Asynchronous up- counter:



Circuit diagram

Truth Table

Number of clock pulses	Q_2 (MSB)	Q_1	Q_0 (LSB)
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1

Timing Diagram

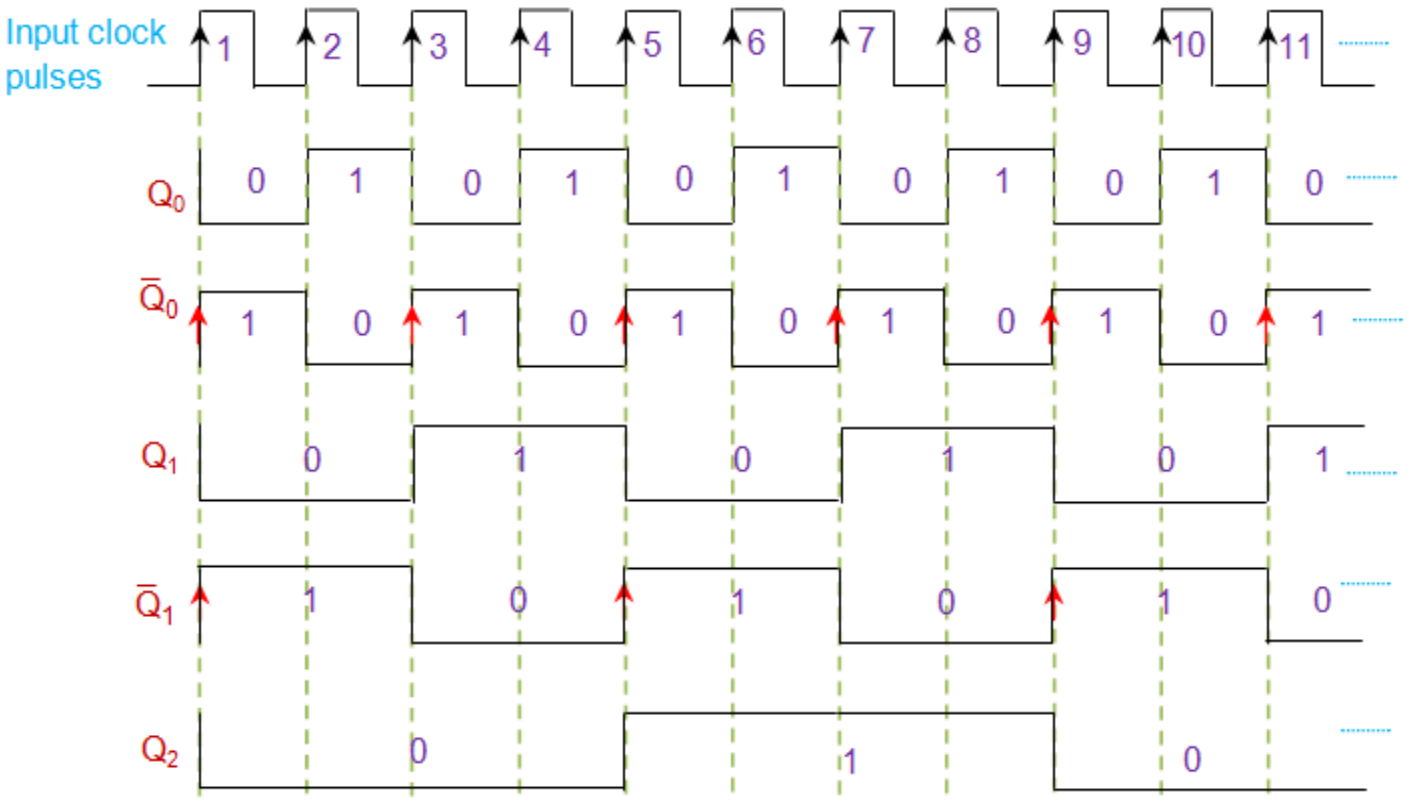
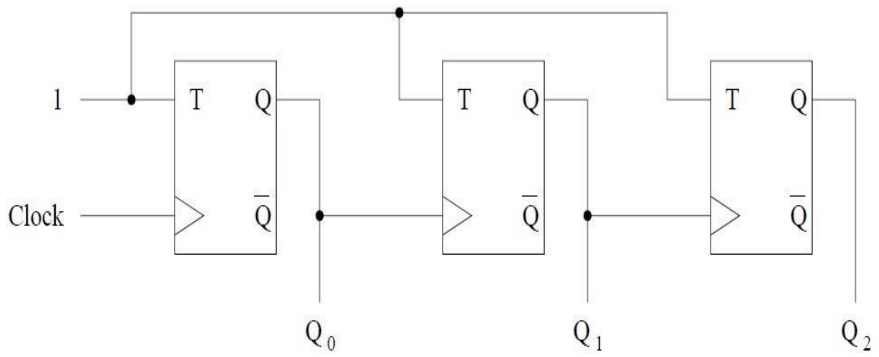


Figure 4 Timing diagram for 3-bit asynchronous positive edge triggered up-counter

3 bit Asynchronous down - counter:

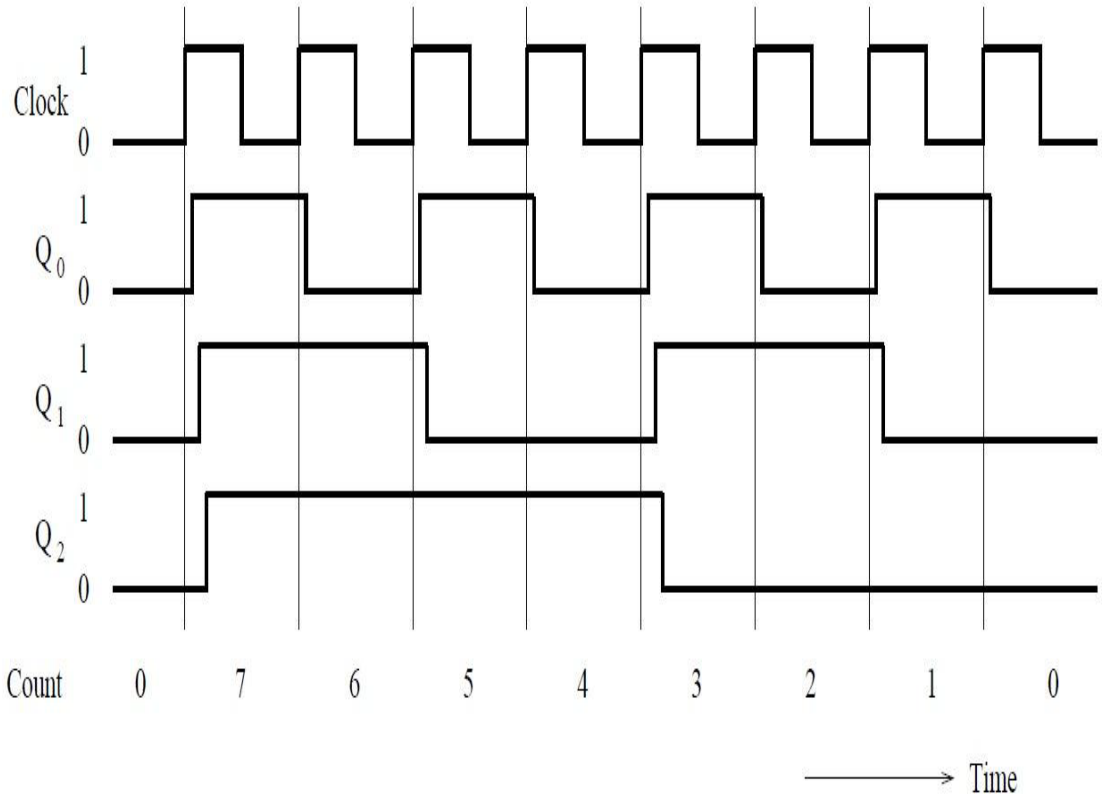


Circuit diagram

Truth Table

Number of clock pulses	Q_2 (MSB)	Q_1	Q_0 (LSB)
0	0	0	0
1	1	1	1
2	1	1	0
3	1	0	1
4	1	0	0
5	0	1	1
6	0	1	0
7	0	0	1

Timing Diagram



ELECTRONIC PRINCIPLES AND DEVICES

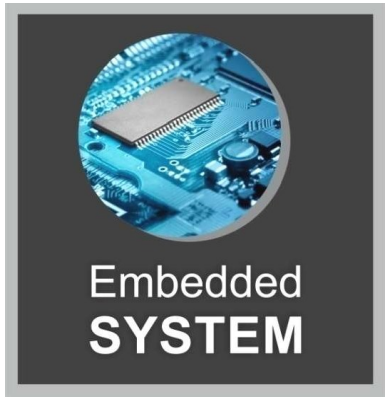
Introduction to Embedded System

❖ Embedded means something that is attached to another thing

❖ A system is an arrangement in which all its unit assemble work together according to a set of rules

'An embedded system is a special-purpose system in which the computer is completely encapsulated by the device it controls'

❖ Unlike a general-purpose computer, such as a personal computer, an embedded system performs pre-defined tasks, usually with very specific requirements



ELECTRONIC PRINCIPLES AND DEVICES

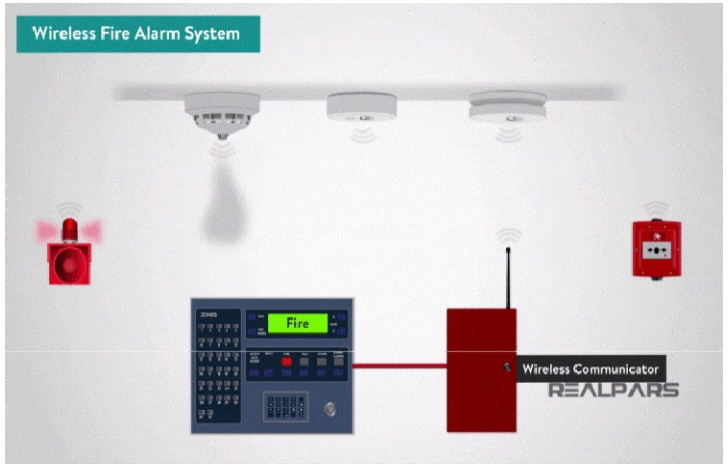
Introduction to Embedded System

❖ An embedded system can be thought of as a computer hardware system having software embedded in it

❖ An embedded system can be an independent system or it can be a part of a large system

❖ An embedded system is a microcontroller or microprocessor based system which is designed to perform a specific task

❖ For example, a fire alarm is an embedded system; it will sense only smoke



What is an Embedded Systems

An Embedded System is an integrated system including both hardware and software is not enough

An embedded system is a dedicated computer system, designed to work f single or few specific functions often within a larger system

Embedded Systems, therefore, are

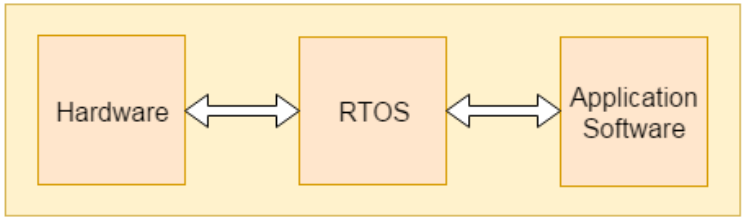
- Built to function with little or no human intervention

- Specially designed keeping in consideration the tasks that need completion in the most efficient way

Main Parts of an Embedded System

An embedded system has three components

- It has hardware
- It has application software
- It has Real Time Operating system (RTOS) that supervises the application software and provide mechanism to let the processor run a process as per scheduling by following a plan to control the latencies



Main Parts of an Embedded System

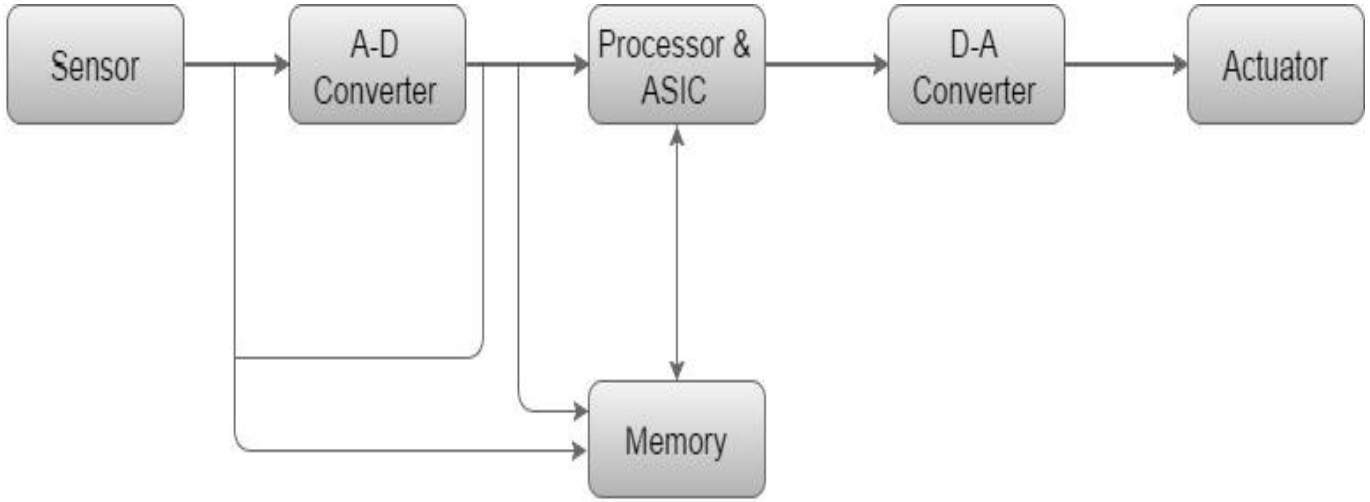
❖ RTOS defines the way the system works. It sets the rules during the execution of application program. A small scale embedded system may not have RTOS

An embedded system as a Microcontroller based, software driven, and reliable, real-time control system

8051 Microcontroller

Basic Structure an Embedded System

The following illustration shows the basic structure of an embedded system



Basic Structure an Embedded System

- **Sensor** – It measures the physical quantity and converts it to an electrical signal which can be read by an observer or by any electronic instrument like an A2D converter. A sensor stores the measured quantity to the memory
- **A-D Converter** – an analog-to-digital converter converts the analog signal sent by the sensor into a digital signal
- **Processor & ASICs** – Processors process the data to measure the output and store it to the memory
- **D-A Converter** – A digital-to-analog converter converts the digital data fed by the processor to analog data
- **Actuator** – An actuator compares the output given by the D-A Converter to the actual (expected) output stored in it and stores the approved output

Features of an Embedded System

❖ **Single-functioned** – an embedded system usually performs a specialized operation and does the same repeatedly

For example: A pager always functions as a pager

❖ **Tightly constrained** – All computing systems have constraints on design metrics, but those on an embedded system can be especially tight

- Design metrics is a measure of an implementation's features such as its cost, size, power, and performance
- It must be of a size to fit on a single chip, must perform fast enough to process data in real time and consume minimum power to extend battery life

Features of an Embedded System Continued…

❖ **Reactive and Real time** – Many embedded systems must continually react to changes in the system's environment and must compute certain results in real time without any delay

Consider an example of a car cruise controller; it continually monitors and reacts to speed and brake sensors. It must compute acceleration or de-accelerations repeatedly within a limited time; a delayed computation can result in failure to control of the car

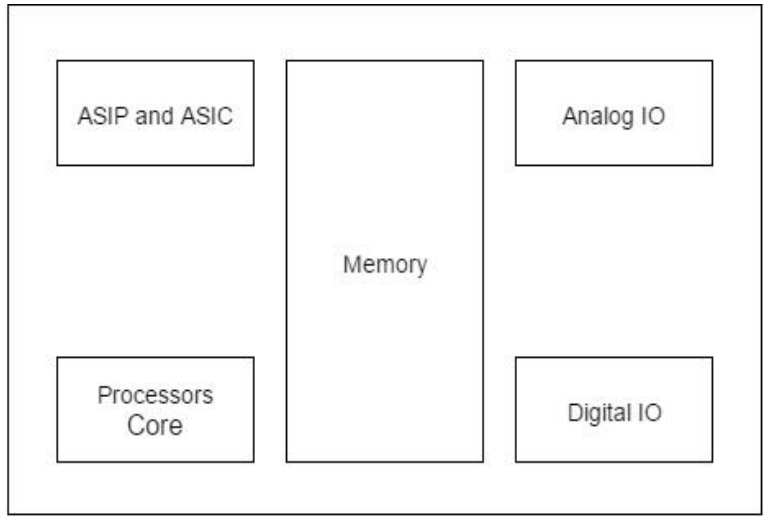
❖ **Microprocessors based** – It must be microprocessor or microcontroller based

❖ **Memory** – It must have a memory, as its software usually embeds in ROM. It does not need any secondary memories in the computer

Features of an Embedded System Continued…

❖**Connected –** It must have connected peripherals to connect input and output devices

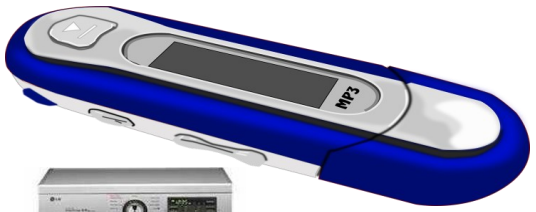
❖**HW-SW systems –** Software is used for more features and flexibility. Hardware is used for performance and security



ELECTRONIC PRINCIPLES AND DEVICES

Characteristics of an Embedded System

- All Embedded Systems are task specific. They do the same task repeatedly /continuously over their lifetime
  - ✓An mp3 player will function only as an mp3 player
- Embedded systems are created to perform the task within a certain time frame. It must therefore perform fast enough
  - ✓A car's brake system, if exceeds the time limit, may cause accidents
- They have minimal or no user interface (UI)
  - ✓A fully automatic washing machine works on its own after the programme is set and stops once the task is over



Characteristics of an Embedded System Continued...

- Some embedded systems are designed to react to external stimuli and react accordingly
  - ✓ A thermometer, a GPS tracking device
- Embedded systems are built to achieve certain efficiency levels

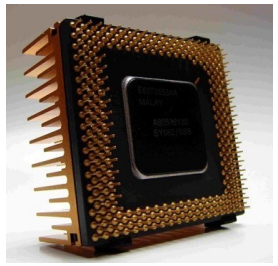
They are small sized, can work with less power and are not too expensive

- Embedded systems cannot be changed or upgraded by the users

Hence, they must rank high on reliability and stability. They are expected to function for long durations without the user experiencing any difficulties

Characteristics of an Embedded System Continued...

- Microcontroller or microprocessors are used to design embedded systems
- Embedded systems need connected peripherals to attach input & output devices
- The hardware of an embedded-system is used for security and performance. The Software is used for features
- The firmware of an ES is pre-programmed and it is non alterable by the end user



Applications of Embedded System

Some real-life applications of Embedded Systems are as follows:

- **Consumer electronics –** Televisions and digital cameras; computer printers; video game consoles and home entertainment systems like PS4
- **Household appliances –** Refrigerators; washing machines, microwave ovens, air conditioners
- **Medical equipment –** Scanners like those for MRI, CT; ECG machines; devices to monitor blood pressure and heartbeat
- **Automobiles –** Fuel injection systems, anti-lock braking systems, music and entertainment systems, controls for air-conditioner

Applications of Embedded System Continued…

- **Industrial applications –** Assembly lines, systems for feedback, systems for data collection
- **Aerospace –** Systems for navigation and guidance, GPS
- **Communications –** Routers, satellite phones

Core of the Embedded System

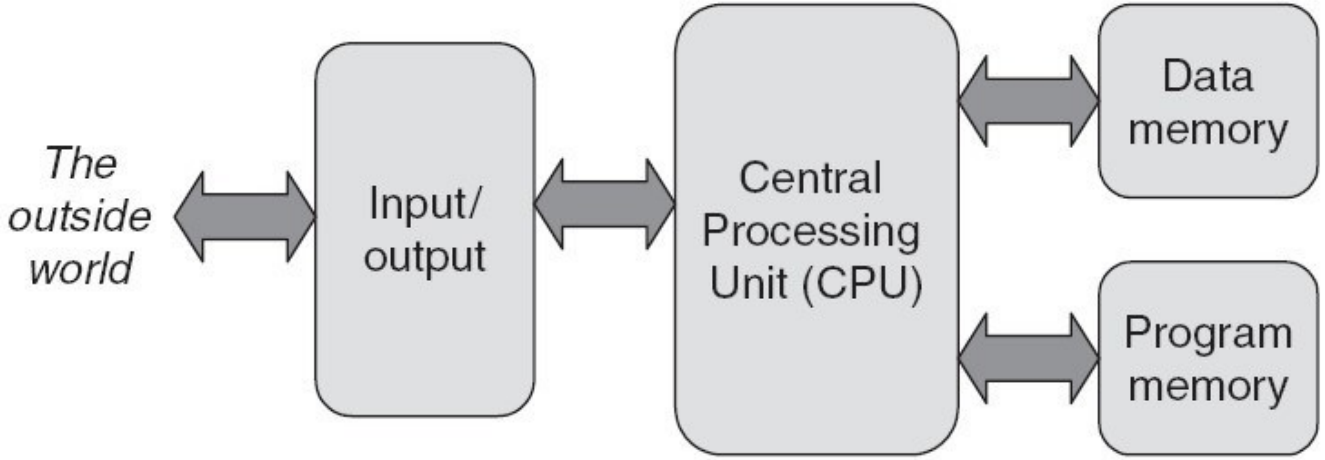
- Embedded systems are domain and application specific and are built around a central core
- The core of the embedded system falls into any of the following categories:
  1. General purpose and Domain Specific Processors
     1. Microprocessors
     2. Microcontrollers 1.3. Digital Signal Processors
  2. Application Specific Integrated Circuits (ASIC)
  3. Programmable logic devices(PLD's)
  4. Commercial off-the-shelf components (COTs)

ELECTRONIC PRINCIPLES AND DEVICES

GENERAL PURPOSE AND DOMAIN SPECIFIC PROCESSOR

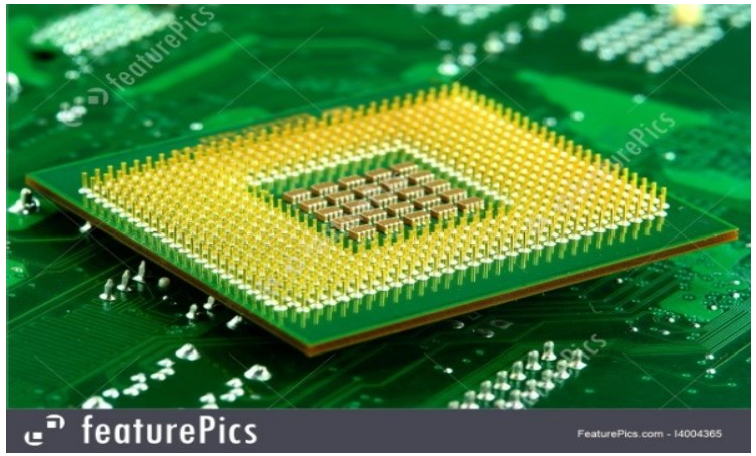
- Almost 80% of the embedded systems are processor/ controller based
- The processor may be microprocessor or a microcontroller or digital signal processor, depending on the domain and application

a



Microprocessors

- A microprocessor is a silicon chip representing a central processing unit



- A microprocessor is a dependent unit and it requires the combination of other hardware like memory, timer unit, and interrupt controller, etc. for proper functioning

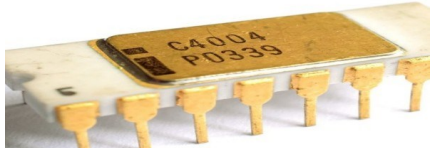
- Architectures used for processor design are Harvard or Von-Neumann

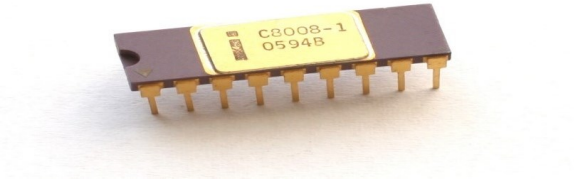
ELECTRONIC PRINCIPLES AND DEVICES

Microprocessors

❖ **Developers of microprocessors**

- ✓ Intel – Intel 4004 – November 1971(4-bit)
- ✓ Intel – Intel 4040
- ✓ Intel – Intel 8008 – April 1972
- ✓ Intel – Intel 8080 – April 1974(8-bit)
- ✓ Motorola – Motorola 6800
- ✓ Intel – Intel 8085 – 1976
- ✓ Zilog - Z80 – July 1976

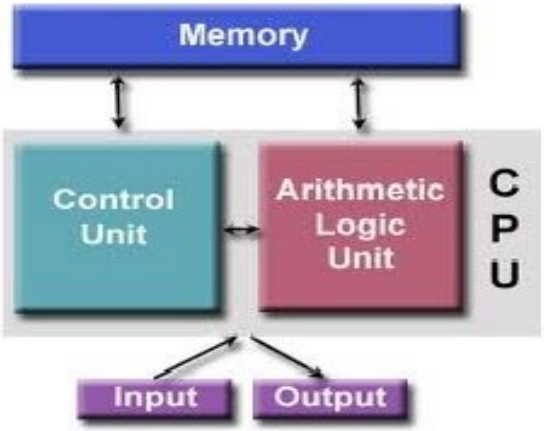




Processors in a System

❖A processor has two essential units –

- ✓Program Flow Control Unit (CU)
- ✓Execution Unit (EU)



➢The CU includes a fetch unit for fetching instructions from the memory

➢The EU has circuits that implement the instructions pertaining to data transfer operation and data conversion from one form to another

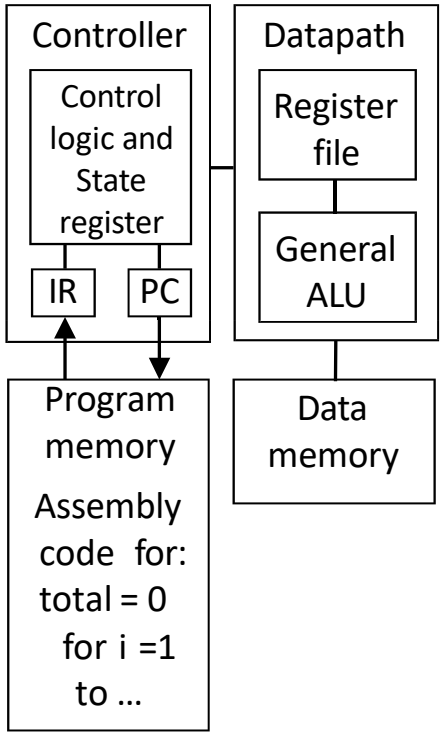
Processors in a System

- The EU includes the Arithmetic and Logical Unit (ALU) and also the circuits that execute instructions for a program control task such as interrupt, or jump to another set of instructions

- A processor runs the cycles of fetch and executes the instructions in the same sequence as they are fetched from memory

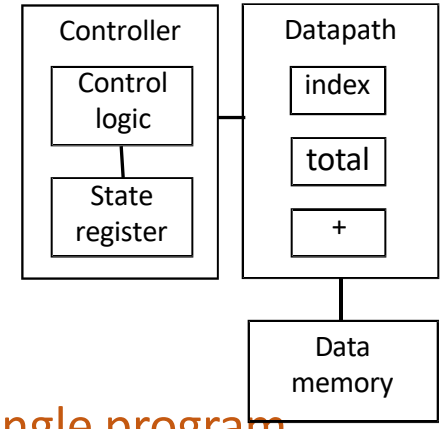
General Purpose Processors

- Programmable device used in a variety of applications
  - ✓ Also known as "microprocessor"
- Features
  - ✓ Program memory
  - ✓ General data path with large register file and general ALU
- User benefits
  - ✓ Low time-to-market and NRE costs
  - ✓ High flexibility
- "Pentium" the most well-known, but there are hundreds of others



Single-purpose processors

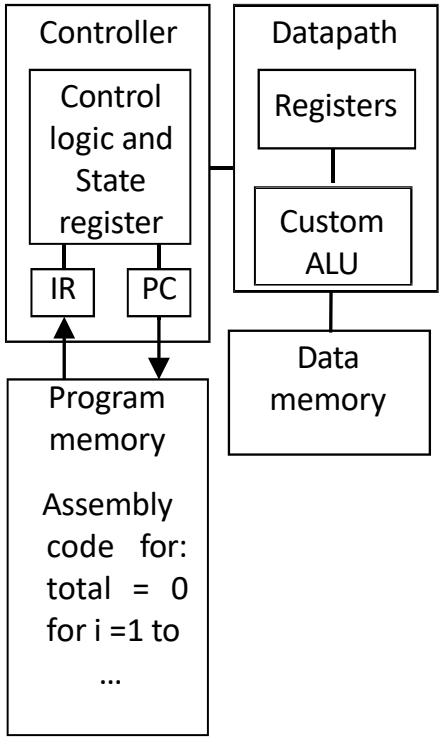
- Digital circuit designed to execute exactly one program
  - ✓ a.k.a. coprocessor, accelerator or peripheral



- Features
  - ✓ Contains only the components needed to execute a single program
  - ✓ No program memory
  - Benefits
  - ✓ Fast
  - ✓ Low power
  - ✓ Small size

Application-Specific Processors

- Programmable processor optimized for a particular class of applications having common characteristics
  - ✓ Compromise between general-purpose and single-purpose processors
- Features
  - ✓ Program memory
  - ✓ Optimized data path
  - ✓ Special functional units
- Benefits
  - ✓ Some flexibility, good performance, size and power



Processor Technology

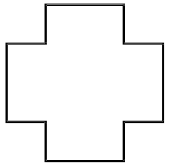
❖ Processors vary in their customization for the problem at hand

Desired functionality

```
total = 0
for i = 1 to N  loop
    total += M[i]
end loop
```

General-purpose processor

Application-specific processor



Single-purpose processor

THANK YOU

Department of Electronics and Communication