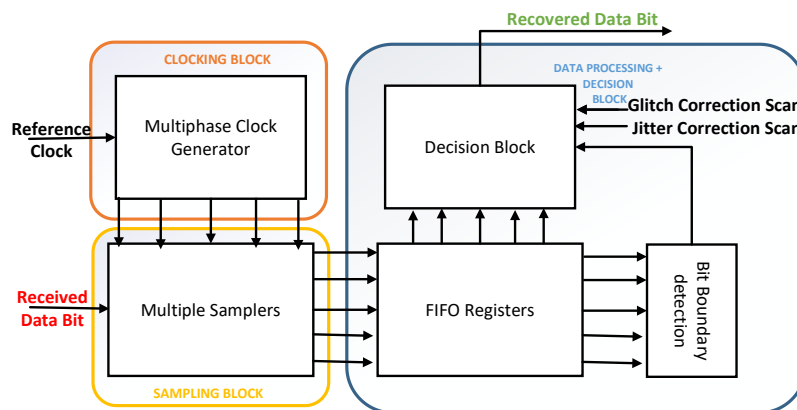


Clock and Data Recovery (CDR) Circuit is a critical component in high speed wireline links, SERDES, backplane communication or chip-to-chip interconnects, etc. CDR plays a key role to get the transmitted data from the distorted received signal and to recover the associated clock timing information. The clock recovery circuit detects the transitions in the received data and generates a periodic clock that is used in extracting correct transmitted bits. [1][2]

The uploaded gds and netlist is an **Oversampling CDR**, which uses a internal clock to sample the received signal at multiple points. The sampled received bits are stored in a data registers and are used to determine the optimal sampling point, by finding the optimal bit boundary for correct transmitted data recovery. Oversampling CDR has fast acquisition time and inherent stability but suffers from rejecting high frequency jitters and requiring large registers for storage of sampled data.

Design Parameters:

Architecture: **Oversampling CDR**



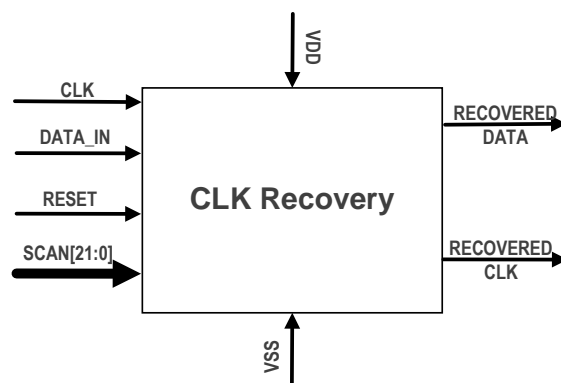
Technology: **Skywater OpenPDK 130nm**

Size: **229um*240um = 0.055mm²**

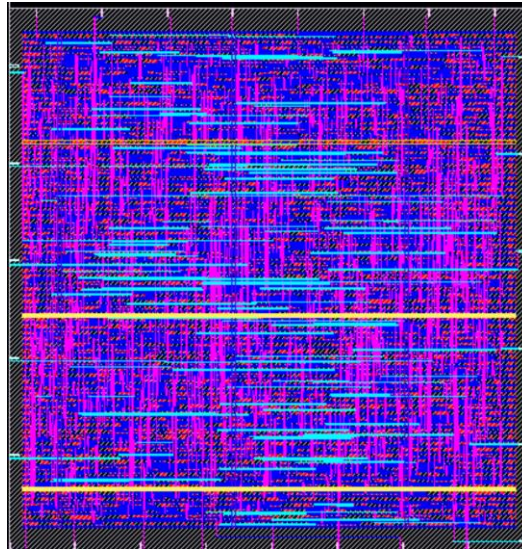
Maximum Frequency of Operation:

Tools Used: **OpenLane, Virtuoso Cadence**

Symbol



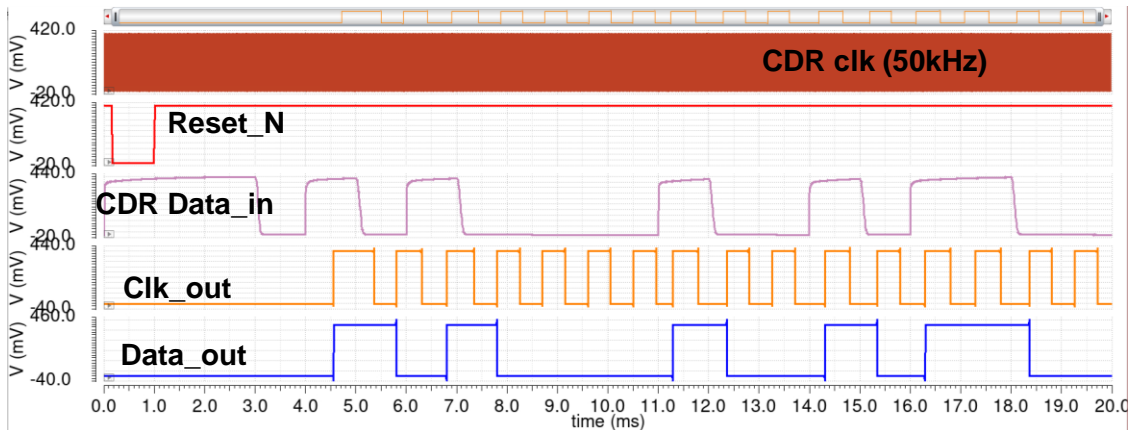
Generated Layout:



Uploaded Files:

- Gds file: CLK_RECOVERY.gds
- Synthesized Verilog file: CLK_RECOVERY.lvs.v
- Spice Netlist: CLK_RECOVERY.sp
- PEX Netlist: CLK_RECOVERY.pex.netlist
- LEF file: CLK_RECOVERY.lef

Results:



Future Works:

We will be uploading the MM-CDR [2] that uses PLL based loop tracking to recover Clock and Data transitions in receiver that is compatible to work in interference-limited broadband communication channels.

References:

- [1] M. Hsieh and G. E. Sobelman, "Architectures for multi-gigabit wire-linked clock and data recovery," in *IEEE Circuits and Systems Magazine*, vol. 8, no. 4, pp. 45-57, Fourth Quarter 2008, doi: 10.1109/MCAS.2008.930152.
- [2] P. Mehrotra, S. Maity and S. Sen, "An Improved Update Rate CDR for Interference Robust Broadband Human Body Communication Receiver," in *IEEE Transactions on Biomedical Circuits and Systems*, vol. 13, no. 5, pp. 868-879, Oct. 2019, doi: 10.1109/TBCAS.2019.2940746.