Design Parameters:

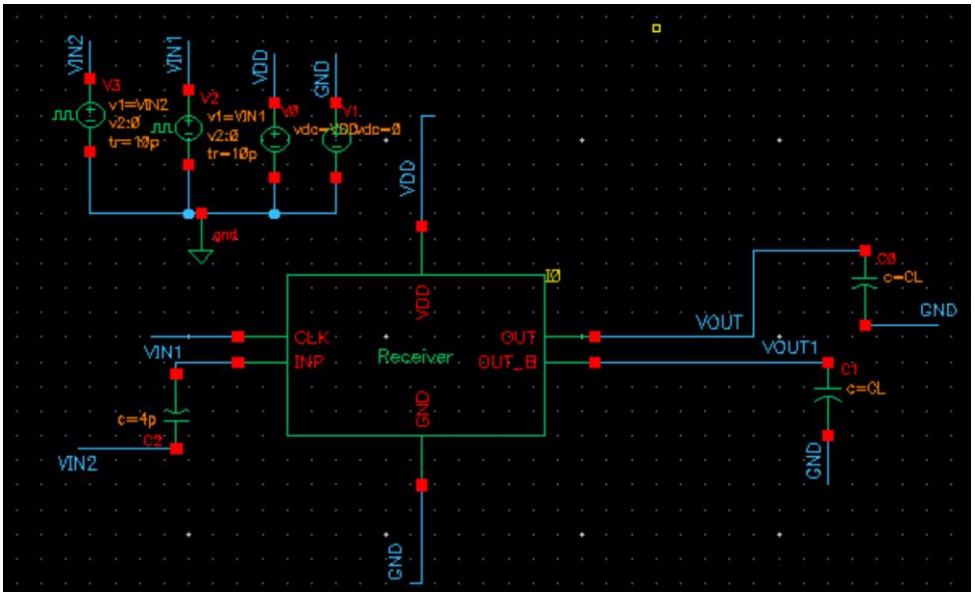
Architecture: **Receiver with CDR bypassed**

Technology: **Skywater OpenPDK 130nm**

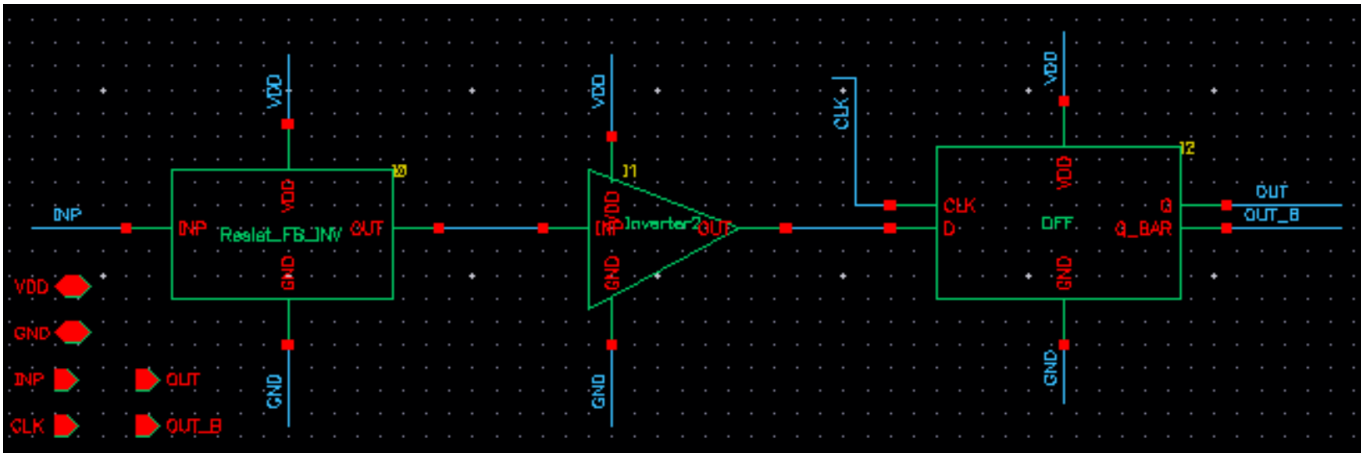
Size: **36um*64um= 0.00023mm^2**

Tools Used: **Virtuoso Cadence**

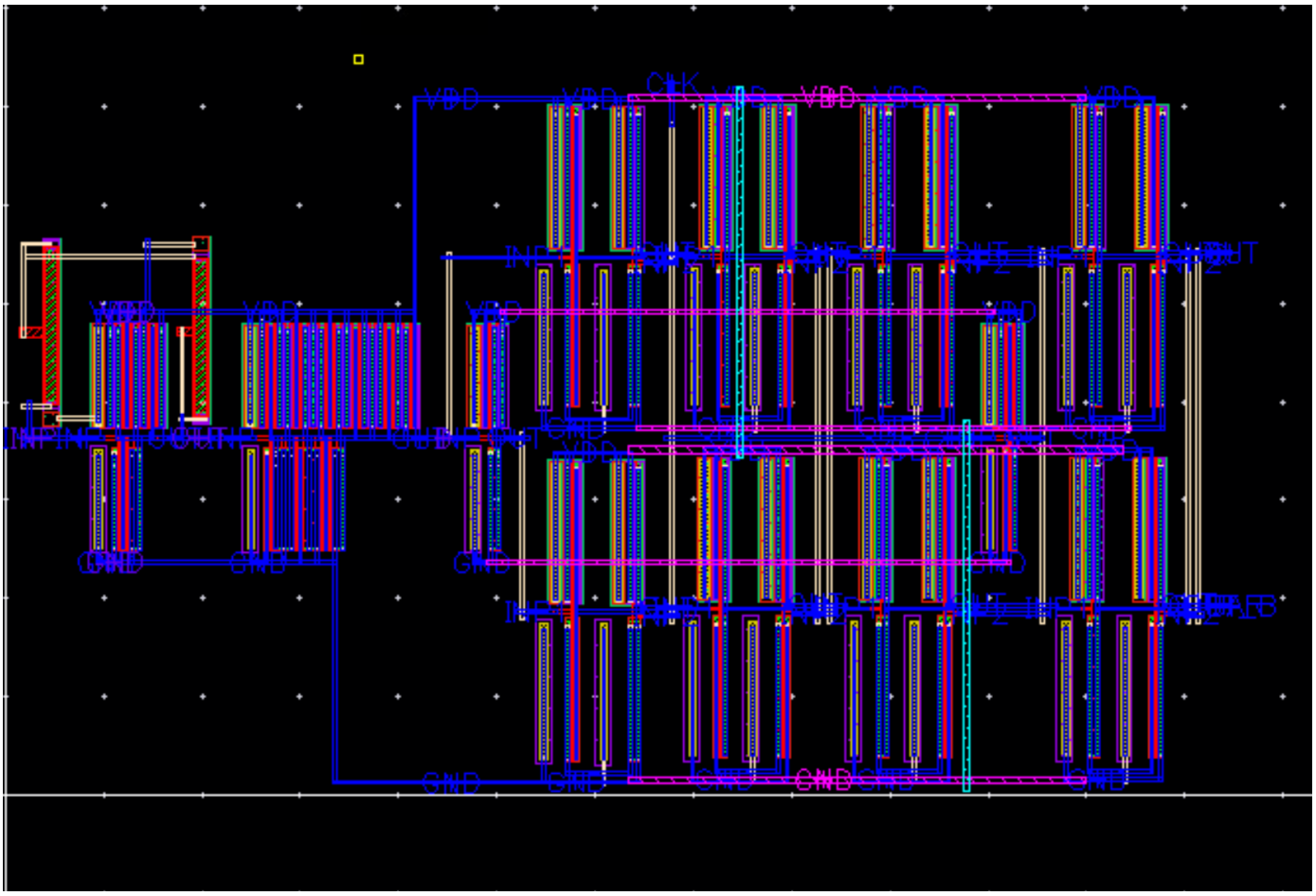
Symbol



Schematic



Generated Layout:



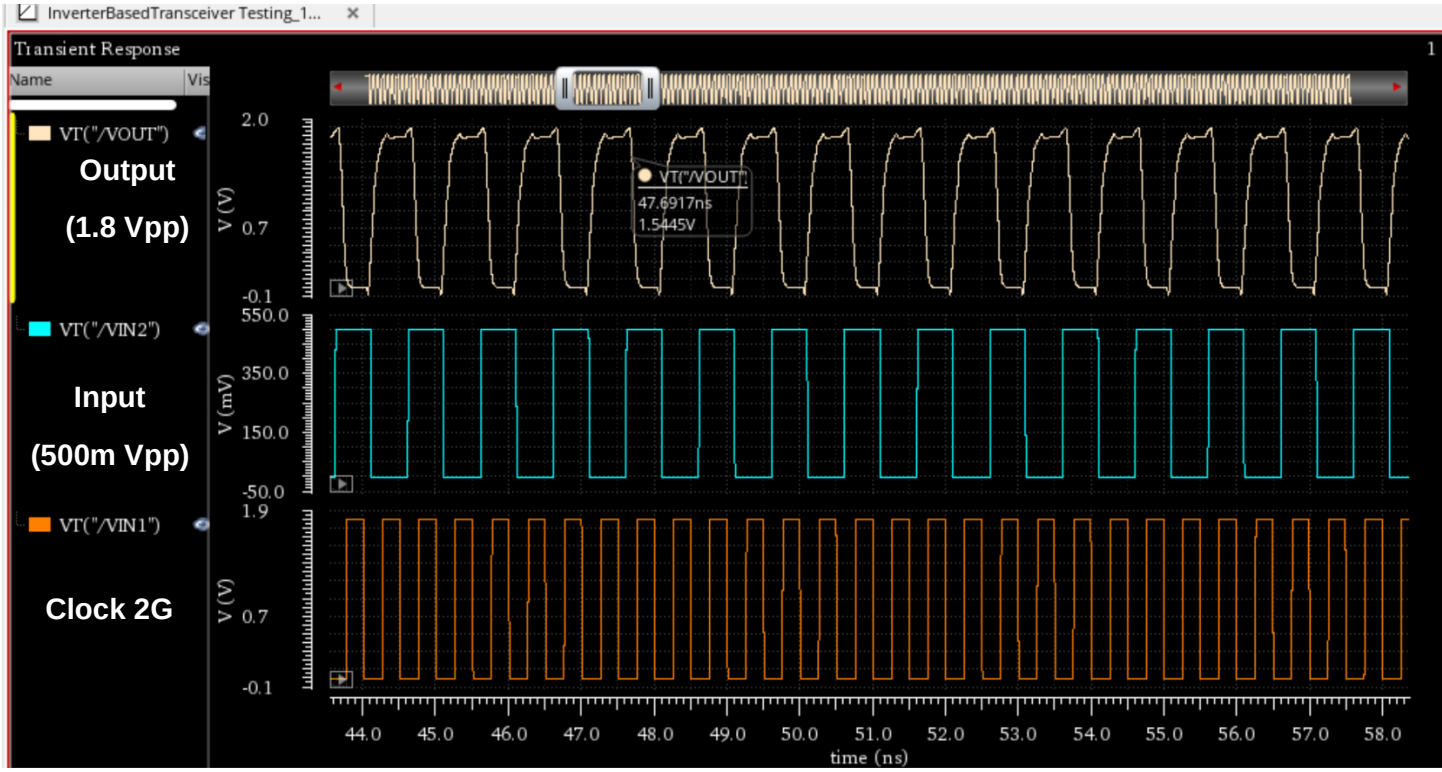
Uploaded Files:

- Gds file: Receiver.gds
- Spice Netlist: Receiver.sp
- PEX Netlist: Receiver.pex.netlist

Highlights:

Achieved faithful decoding of 500mV signal at the input of Receiver with the help of Resistive Feedback Inverter+ CMOS inverter + DFF combination

Results:


InverterBasedTransceiver Testing_1...
Transient Response
Name
VT("/VOUT")
Output
(1.8 Vpp)
VT("/VIN2")
Input
(500m Vpp)
VT("/VIN1")
Clock 2G
V (V)
V (mV)
VT("/VOUT")
47.6917ns
1.5445V
44.0
45.0
46.0
47.0
48.0
49.0
50.0
51.0
52.0
53.0
54.0
55.0
56.0
57.0
58.0
time (ns)