Design Parameters:

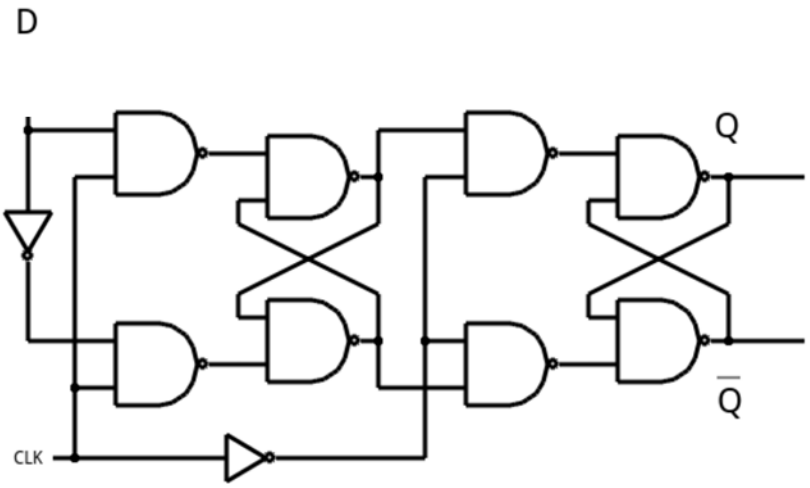
Architecture: **DFF**

Technology: **Skywater OpenPDK 130nm**

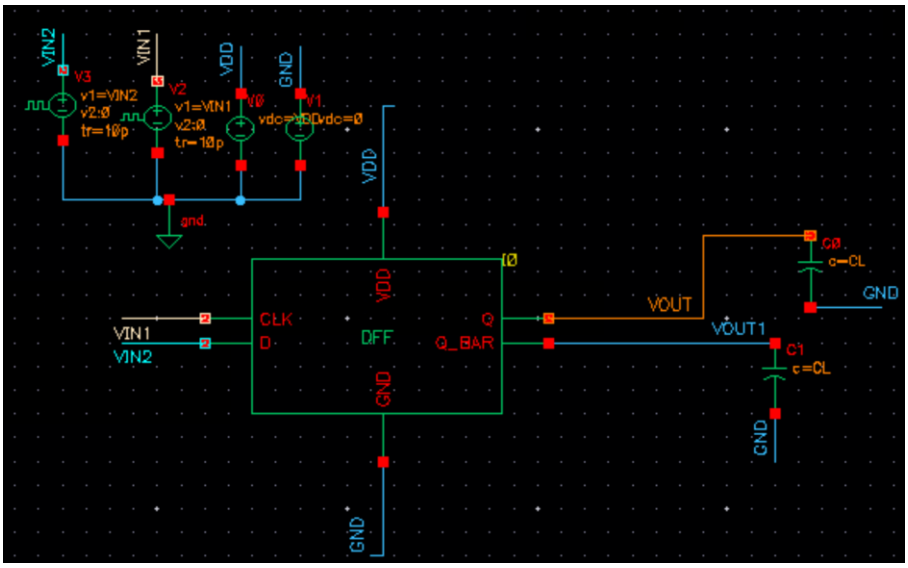
Size: **40um*37um= 0.0015mm^2**

Tools Used: **Virtuoso Cadence**

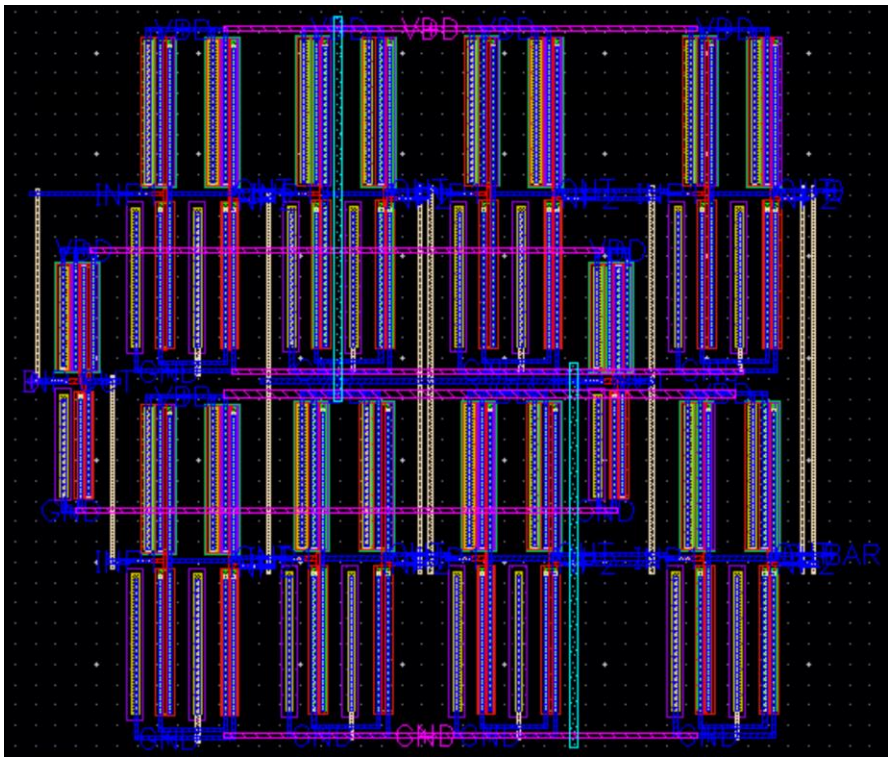
Schematic



Test Circuit



Generated Layout:



Uploaded Files:

- Gds file: DFF.gds
- Synthesized Verilog file: DFF.lvs.v
- Spice Netlist: DFF.sp
- PEX Netlist: DFF.pex.netlist

Results: