Design Parameters:

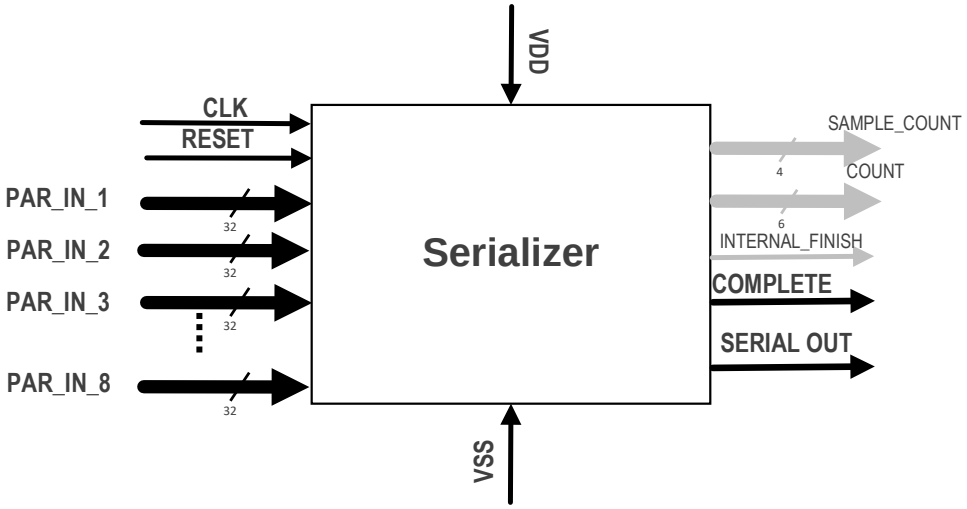
Architecture: **Serializer**

Technology: **Skywater OpenPDK 130nm**

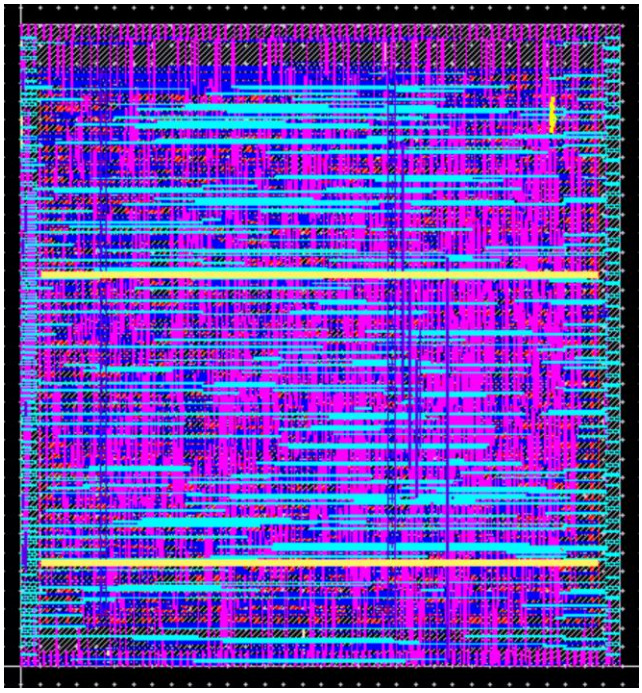
Size: **160um*170um = 0.027mm^2**

Tools Used: **OpenLane**, **Virtuoso Cadence**

Symbol



Generated Layout:



Uploaded Files:

- Gds file: serializer_unit_cell_1.gds
- Synthesized Verilog file: serializer_unit_cell_1.lvs.v
- Spice Netlist: serializer_unit_cell_1.sp
- PEX Netlist: serializer_unit_cell_2.pex.netlist
- LEF file: serializer_unit_cell_1.lef

Results: