Design Parameters:

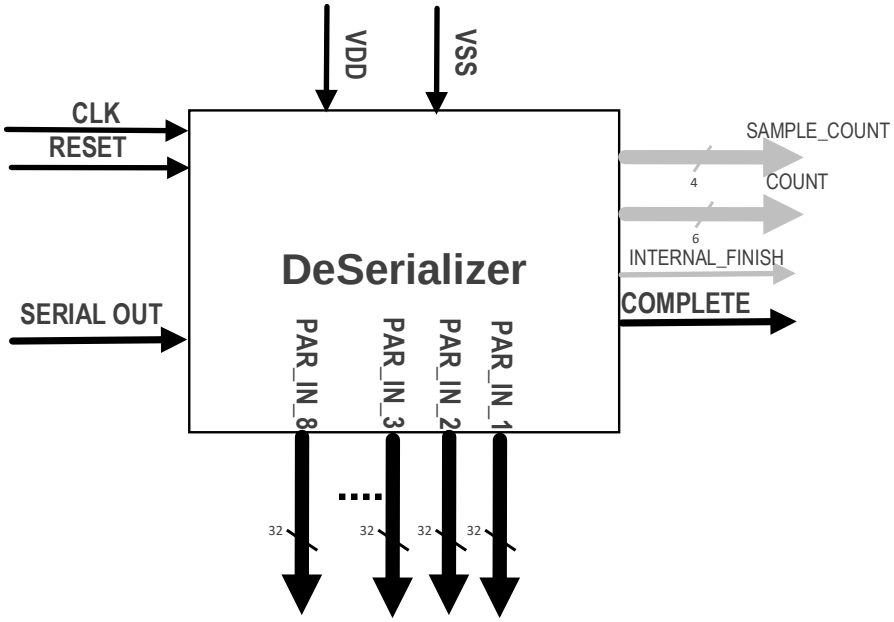
Architecture: **DeSerializer**

Technology: **Skywater OpenPDK 130nm**

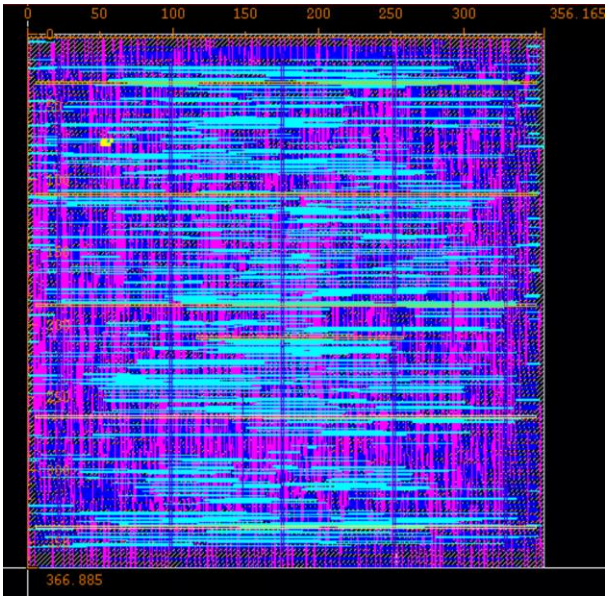
Size: **360um*360um = 0.13mm^2**

Tools Used: **OpenLane**, **Virtuoso Cadence**

Symbol



Generated Layout:



Uploaded Files:

- Gds file: deserializer_unit_cell_1.gds
- Synthesized Verilog file: deserializer_unit_cell_1.lvs.v
- Spice Netlist: deserializer_unit_cell_1.sp
- PEX Netlist: deserializer_unit_cell_1.pex.netlist
- LEF file: deserializer_unit_cell_1.lef

Results: