**Design Parameters:**

Architecture: **DeSerializer**

Technology: **Skywater OpenPDK 130nm**

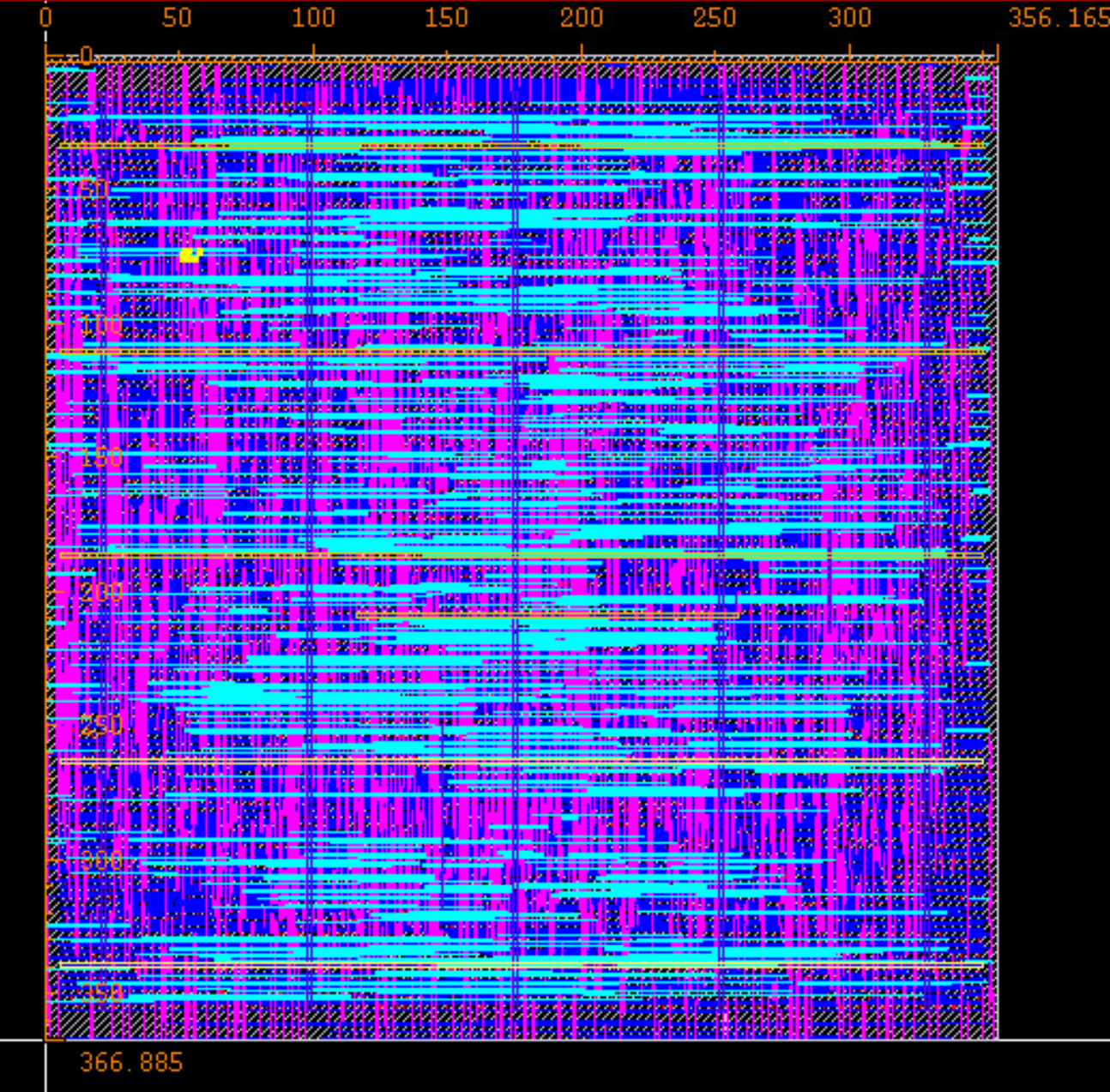
Size: **360um\*360um = 0.13mm2**

Tools Used: **OpenLane**, **Virtuoso Cadence**

**Symbol**



**Generated Layout:**



**Uploaded Files:**

* Gds file: deserializer\_unit\_cell\_1.gds
* Synthesized Verilog file: deserializer\_unit\_cell\_1.lvs.v
* Spice Netlist: deserializer\_unit\_cell\_1.sp
* PEX Netlist: deserializer\_unit\_cell\_1.pex.netlist
* LEF file: deserializer\_unit\_cell\_1.lef

**Results:**

