**Design Parameters:**

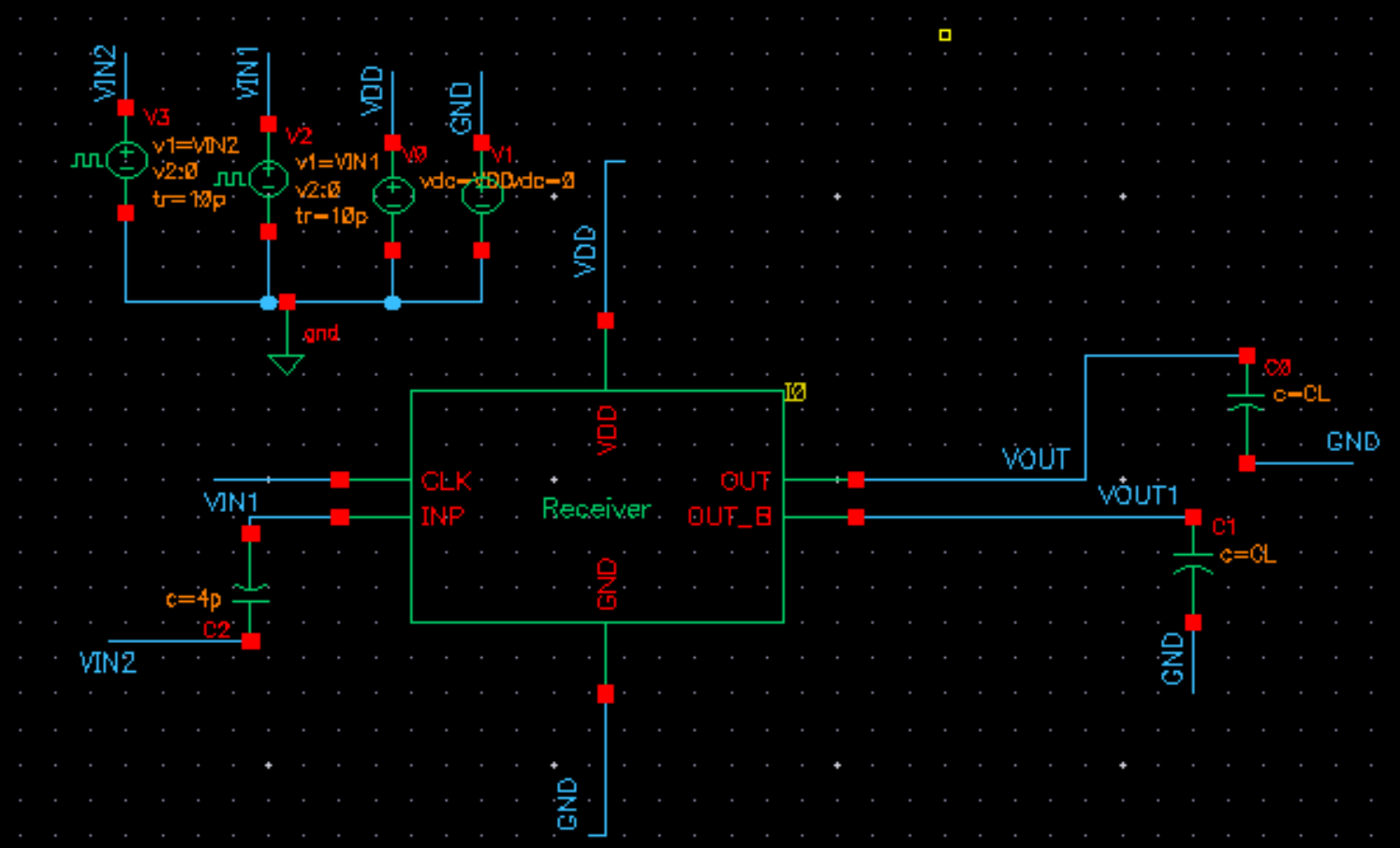
Architecture: **Receiver with CDR bypassed**

Technology: **Skywater OpenPDK 130nm**

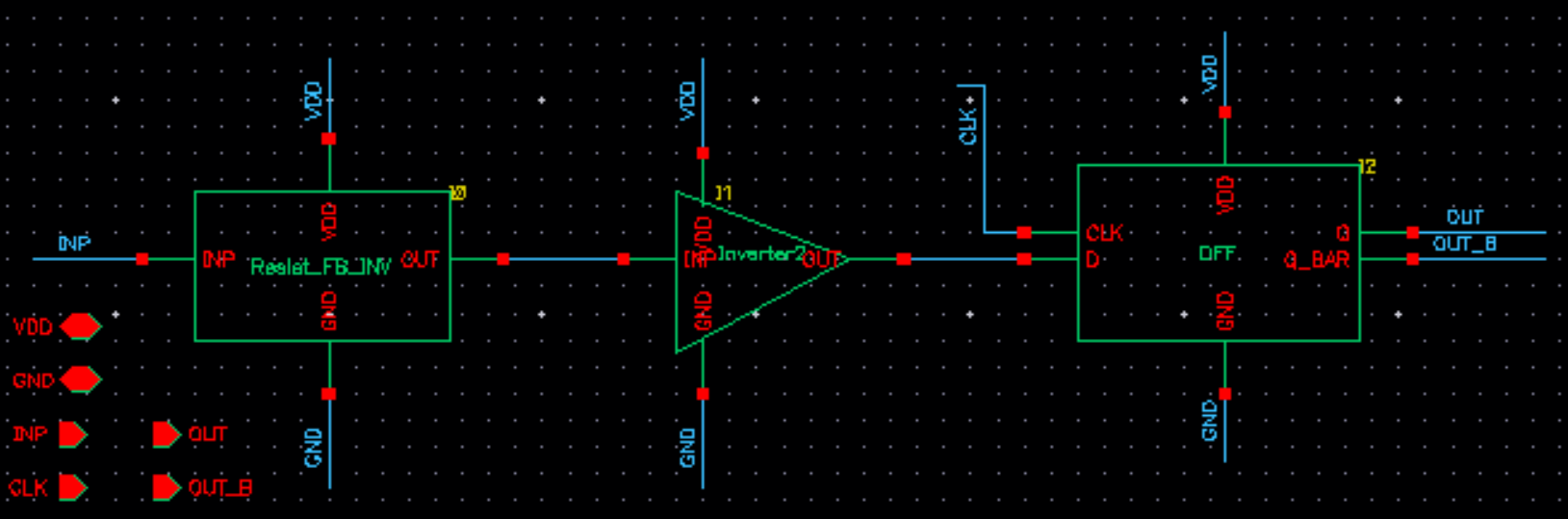
Size: **36um\*64um= 0.00023mm2**

Tools Used: **Virtuoso Cadence**

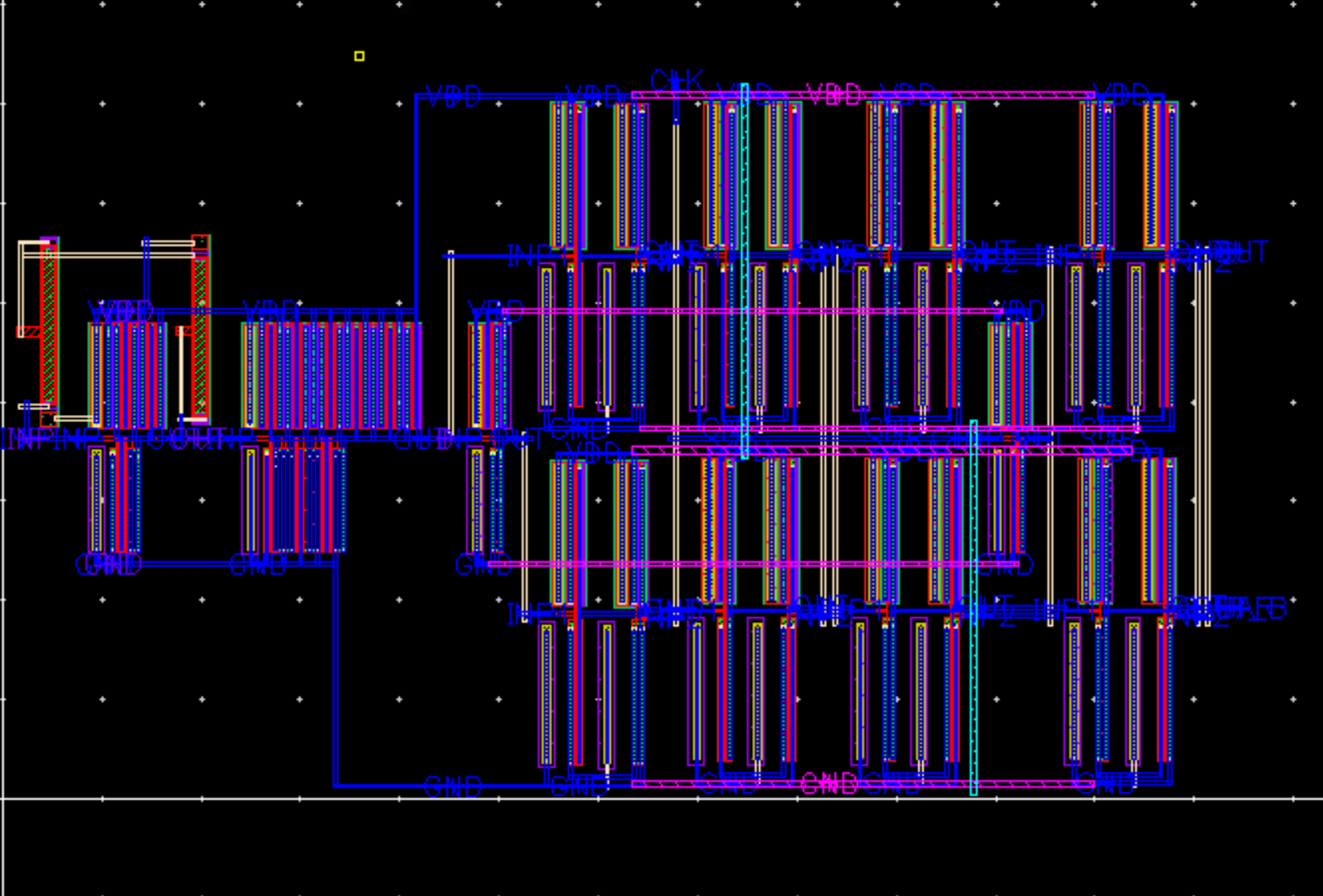
**Symbol**



**Schematic**

****

**Generated Layout:**



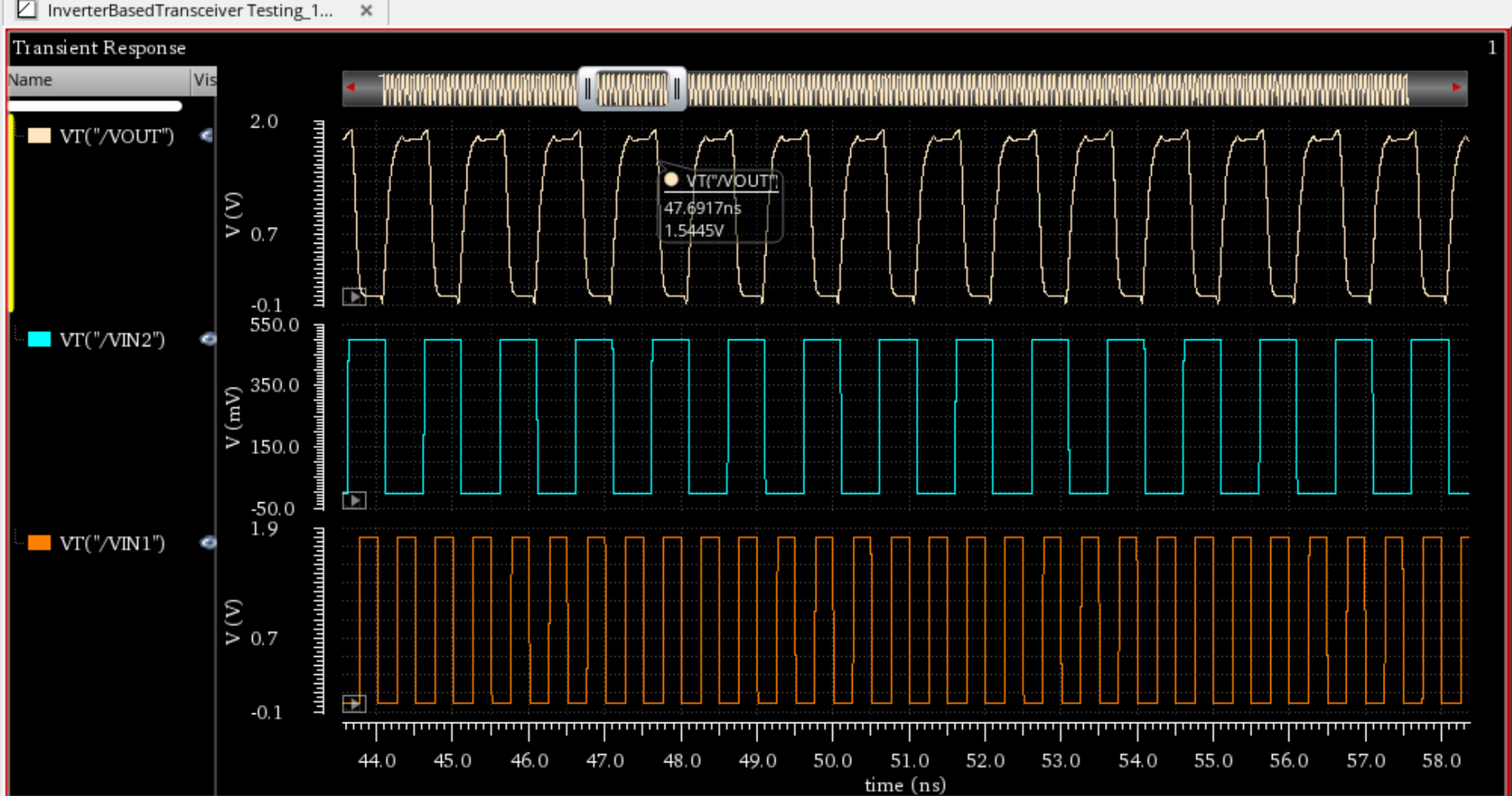
**Uploaded Files:**

* Gds file: Receiver.gds
* Spice Netlist: Receiver.sp
* PEX Netlist: Receiver.pex.netlist

**Highlights:**

Achieved faithful decoding of 500mV signal at the input of Receiver with the help of Resistive Feedback Inverter+ CMOS inverter + DFF combination

**Results:**



**Output**

**(1.8 Vpp)**

**Input**

**(500m Vpp)**

**Clock 2G**