Pre-lab Task 1: **ALSO SUBMIT YOUR MODIFIED DATAPATH**

Add your own control signals used with muxes that you use to support the shift left/right operation

Type	Opcode	funct	ALUSrc	RegDst	RegWrite	ALUOp	MemRead	MemWrite	MemtoReg	PCSrc	RegA	RegB
add	000000	100000	0	1	1	0000	0	0	0	0	0	0
sub	000000	100010	0	1	1	0001	0	0	0	0	0	0
and	000000	100100	0	1	1	0011	0	0	0	0	0	0
or	000000	100101	0	1	1	0100	0	0	0	0	0	0
slt	000000	101010	0	1	1	0101	0	0	0	0	0	0
sll	**000000**	**000000**	X	1	1	1000	0	0	0	0	1	1
srl	**000000**	**000010**	X	1	1	1001	0	0	0	0	1	1
clo	011100	100001	0	1	1	1011	0	0	0	0	0	0
clz	011100	100000	0	1	1	1100	0	0	0	0	0	0
mul	011100	000010	0	1	1	0010	0	0	0	0	0	0
addi	001000	100000	1	0	1	0000	0	0	0	0	0	0
ori	001101	100101	1	0	1	0100	0	0	0	0	0	0