NOVATEK 聯詠科技

Data Sheet

NT98562

Imaging Processor

Datasheet

Table of Contents

Revision History

Rev.	Date	Contents
V0.1	2020/09/10	draft
V0.2	2020/12/09	Modify feature and add pin description

Features

■ High Performance 32-bit CPU

- □ Single Core ARM® Cortex™ - A9
- □ NEON™ and FPU acceleration
- □ 32 KB instruction cache, 32 KB data cache and 128 KB L2 cache
- □ Embedded ICE makes firmware debugging easier

■ Power Management features

- □ Firmware configurable operating frequency of each functional block to meet best power budget

■ Integrated Clock Generator

- □ Internal PLL with spread spectrum capability
- □ 12MHz system
- □ 32768Hz RTC oscillator

■ Scalable Memory Bus Architecture

- □ NT98562: SIP 512Mb DDR2L DRAM
- □ NT98566: SIP 1Gb DDR3 DRAM

■ Sensor Interface Engine

- □ Support high speed serial interface like MIPI/ sub-LVDS /HiSPi up to 4 channels and 2 clocks for most commercial CMOS sensors.
- □ Support parallel sensor interface for most commercial CMOS sensors.
- □ Support 12-bit sensor data input
- □ Support HDR sensor composition such as SONY DOL mode and Omnivision staggered mode
- □ Support companding HDR sensor
- □ Built-in color pattern generation
- □ Sensor black level clamping
- □ Efficient defect concealment algorithm
- □ Flexible image analysis flow for AE, AWB and AF purpose
- □ Programmable histogram analysis
- □ In-pipeline color shading compensation technology
- □ Support EIS with gyro-sensor input
- □ Support RGBIr4x4, RCCB format
- □ Support up to 5Mp30 or 150M pixel/sec for typical case
- □ Support up to 4Mp60 or 240M pixel/sec for Sensor HDR case
- □ Support up to 1 HDR sensor with 2 frames

- □ Support h/w motion detection to wake up system
- □ Support additional digital gain up to 256x
- □ Support DVS sensor
- □ Support Bayer scaling down

■ Image Processing Engine

- □ Support up to 5Mp30 or 150M pixel/sec for typical case
- □ Advanced image pipeline architecture for multi-purpose hardware acceleration
- □ Support online mode direct from Sensor Interface Engine
- □ Support bayer input compression
- □ Support YUV output compression
- □ Support 2 frames HDR with ghost reduction
- □ Support crop and H/V flip
- □ Support dynamic defect pixel concealment
- □ Powerful temporal and spatial noise reduction technology
- □ In-pipeline lens shading compensation technology
- □ Support radial crop
- □ Wide dynamic range (WDR) for global/local illumination enhancement
- □ Proprietary advanced anti-alias CFA color interpolation for Bayer
- □ False color suppression
- □ In-pipeline geometric distortion correction
- □ In-pipeline color aberration correction
- □ R/G/B Gamma LUT
- □ Advanced edge rendering control and continuity enhancement
- □ Specific color control technology (Patented)
- □ Brightness/contrast and hue/saturation adjustment
- □ High precision color correction matrix for sRGB or specific color requirement
- □ Support defog function
- □ Support purple fringe reduction
- □ Support advanced motion compensated temporal filtering (TMNR3) for efficient video noise reduction
- □ Support local contrast enhancement
- □ Support YUYV422 format output

■ Image Manipulation Engine

- □ High quality anti-aliasing scaling engine from 1/16x to 16x

- □ Support 3 sets scaling output
- □ Support 4 sets data stamp
- □ Support 8 sets privacy mask

■ Computer Vision Acceleration

- □ IVE General intelligent video analysis operation
- □ DIS Digital image stabilization and object tracking engine
- □ MDBC Motion detection and background construction engine

■ LCD Display

- □ High performance scaling up/down engine, programmable gamma correction, color transform and color management for LCD display
- □ Two video windows(YUV422 / YUV420 UVPack)
- □ One OSD windows(8bit palette with alpha plane / ARGB4444 / ARGB1555 / ARGB8565 / ARGB8888)
- □ Programmable width & height to meet LCD resolution exactly
- □ Support digital LCD for 8bit-Serial-RGB, 6bit-Serial-RGB, 8bit-Serial-YUV, MIPI-DSI interface(1/2/4 data lane & 1 clock lane)
- □ Support RGB565/RGB666 parallel interface.
- □ Support 16-bit RGB interface.
- □ Support Flip function
- □ Support rectangle about 16 (Face detection rectangle)sets with global alpha
- □ Support output YUV (422/420) data to dram(not including data in video2 path)
- □ Support digital interface
  BT.601(CCIR601_8b&CCIR601_16b)/BT.656(CCIR656_8b)/BT.1120(CCIR656_16b) output port(8bits Double-Data-Rate capable)

3.3V / 1.8V LCD / Digital video out

■ Graphic Engine

- □ Geometric operation including mirror, flip and rotation
- □ Arithmetic operation including addition, subtraction, color keying, logic operation and alpha blending
- □ OSD blending on YUV
- □ RGB invert
- □ Support anti-alias affine transform

■ True Random Number Generator

- □ Generate true random number

- 32-bits Random number generator

Video CODEC

- Support H.264/AVC codec BP/MP/HP, level 5.1
- Support H.265/HEVC codec MP, level 5.0
- Support multi-channel encoding with performance up to 5-megapixel@30fps
- Support picture resolutions from 208x208 to 4096x4096
- Support CBR, VBR and Macro block QP table
- Support adaptive quantization
- Support frame rotation by 90, 180 and 270 degrees
- Support ROI (10 sets) enhancing picture quality
- Support OSG function

F/W Audio CODEC

- AAC encode / decode (32KHz, 48KHz @ 192kbps)
- ADPCM /G.711 / G.726
- AEC / ANR and ALC

H/W Audio CODEC

- Stereo 16-bits ADC audio recording
- Mono 16-bits DAC audio playback
- Programmable ALC / Noise Gate (for recording)
- Audio sampling rate : 8k, 11.025k, 12k, 16k, 22.05k, 24k, 32k, 44.1k, 48kHz
- Support dual microphone inputs
- Support 4-channel Digital microphone (MEMS-microphone) inputs

JPEG CODEC

- Supports Motion JPEG 5 megapixel@30fps encoding
- Support ISO/IEC 10918-1 baseline JPEG compression/decompression.
- Still image maximum resolutions will be up to 65536x65536 pixels
- Support input format: 420, 211
- Support Encode/Decode mode, rotate 90, 180, 270 degree (only 420 format)
- JPEG supports downloadable Quantization and Huffman tables
- Support Exchangeable Image File format (EXIF 2.2.3 and newer)
- Support OSG function

Digital Audio Interface

- Support I2S codec interface
- Audio clock generator

■ Dual Graphic-based OSD (OSG)

- □ Support 1/2/4-bit palette and ARGB (1555/4444/8888) & RGB565 format / Color key
- □ Support 2 layers OSD
- □ Fixed OSD layer priority (top to down: OSD1->OSD2->Image)
- □ Support max. size up to 2624x2624(H.264/H.265) per layer (depend on encoder)
- □ Support Codec video encode OSD function
- □ Support up to 16 regions per layer, all regions can't overlap inside a layer and one macro-block can't have two or more regions inside a layer.
- □ Support Pixel alpha (ARGB1555, ARGB4444, ARGB8888 and Palette) and Global alpha (RGB565)
- □ Support OSD QP

■ Storage Memory Controller

- □ Secure Digital card and SDIO
- □ Support SD 3.0
- □ Support UHS-I: UHS50 (Max. freq. 96MHz)
- □ Support SPI-NAND and SPI-NOR flash
- □ Support eMMC v4.41 interface

■ USB

- □ Fully compliant with USB2.0 device/host (1 set)
- □ Support Control / Isochronous / Interrupt and Bulk transfer
- □ Support PC camera mode

■ Timers

- □ RTC can be powered by separate backup battery
- □ Watch dog timer
- □ 20 programmable HW timers support resolution up to 3MHz and 32 bits counter

■ Peripheral Interface

- □ Support I2C interface (3 set)
- □ Support 12 channels PWM including built-in 2 (2 sets) pattern generators for μ-Stepping motor control
- □ Support GPIO and flexible PWM interface with micro-stepping
- □ Support programmable 3-wired serial interface (with DMA transfer)
- □ Support SPI interface (only PIO)
- □ Dedicated SPI for gyroscope reading (only PIO)
- □ Support UART interface (3 set, 1 with PIO and 2/3 with DMA transfer and support RS485

standard)

- □ Support Remote interface
- □ Support 2 channels of 9-bit ADC, the max. sample rate up to 12.5 KHz per channel (one is thermal channel)
- □ Embedded Ethernet 10M/100M MAC and TSO/UFO acceleration for reducing the CPU usage.
- □ Embedded Ethernet PHY, Fully compliant with 100BASE-TX, and 10BASE-T PMD level standards (IEEE 802.3, 802.3u)
- □ Embedded temperature sensor for obtaining the internal chip temperature.

■ **On-chip Boot Strap Loader**

- □ Built-in on-chip mask ROM
- □ User program can be stored in NAND-type flash and external static memory is not necessary
- □ On-chip mask ROM can be disabled
- □ System can boot from SPI NOR/ NAND flash, memory cards, eMMC, Ethernet

■ **Triple Voltage Power Supply**

- □ 0.9V core logic voltage
- □ 1.5V DDR power for NT98562 , 1.5V/1.35V DDR power for NT98566
- □ 3.3V I/O interface and analog circuit voltage

■ **Package**

■ 88 pin QFN, 9x9 mm^2

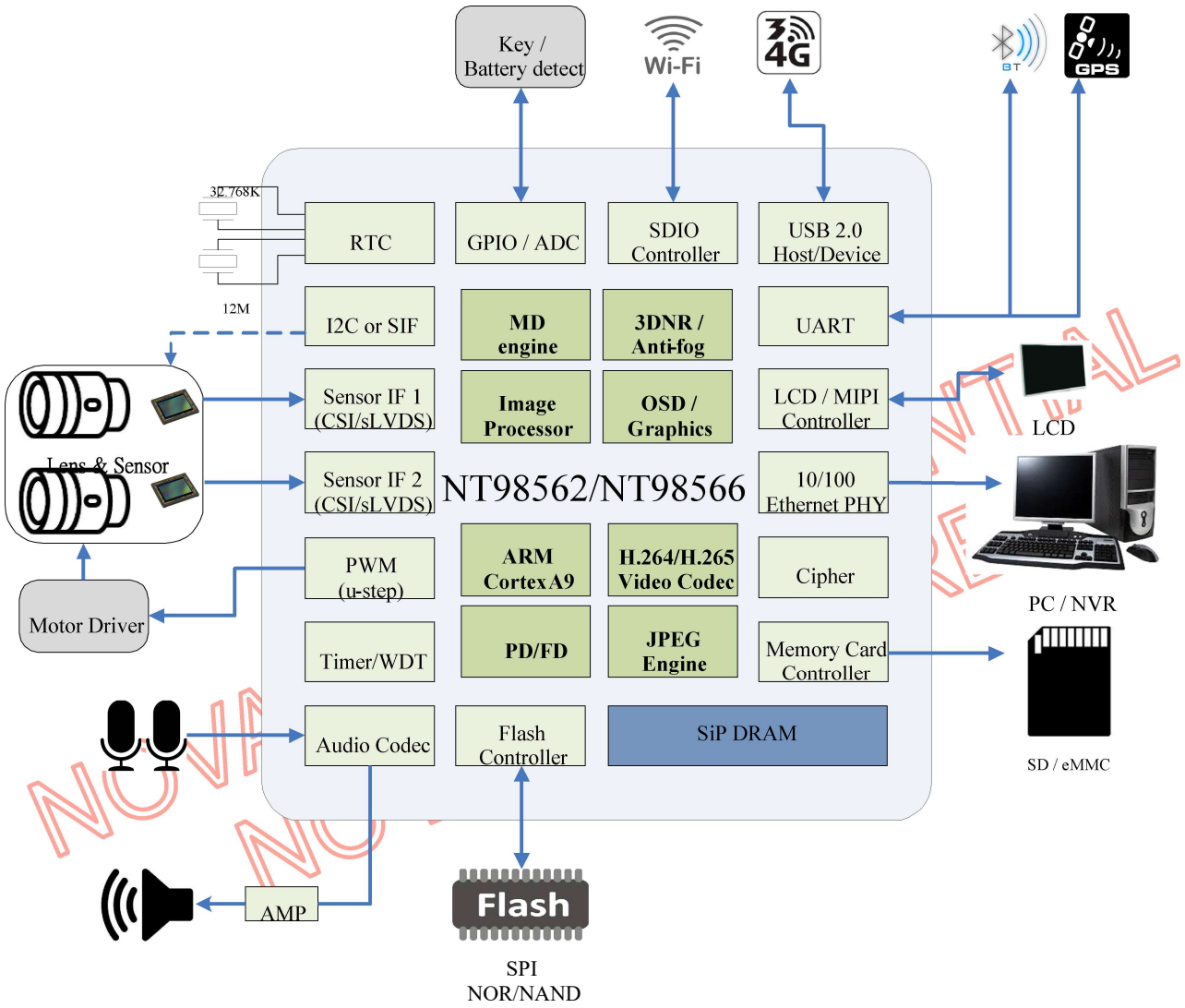
General Description(NT98562)

Novatek NT98562 is a highly-integrated SoC with high image quality, low bitrate, low power consumption, targets on 2Mp to 4Mp Edge-IP camera application. The SoC integrates ARM Cortex A9 CPU core, new generation ISP, H.265/H.264 video compression codec, high performance hardware DLA module, graphic engine, display controller, Ethernet PHY, USB 2.0 Host/Device, audio codec, RTC and SD/SDIO 3.0 to provide best cost performance Edge-IP camera solution.

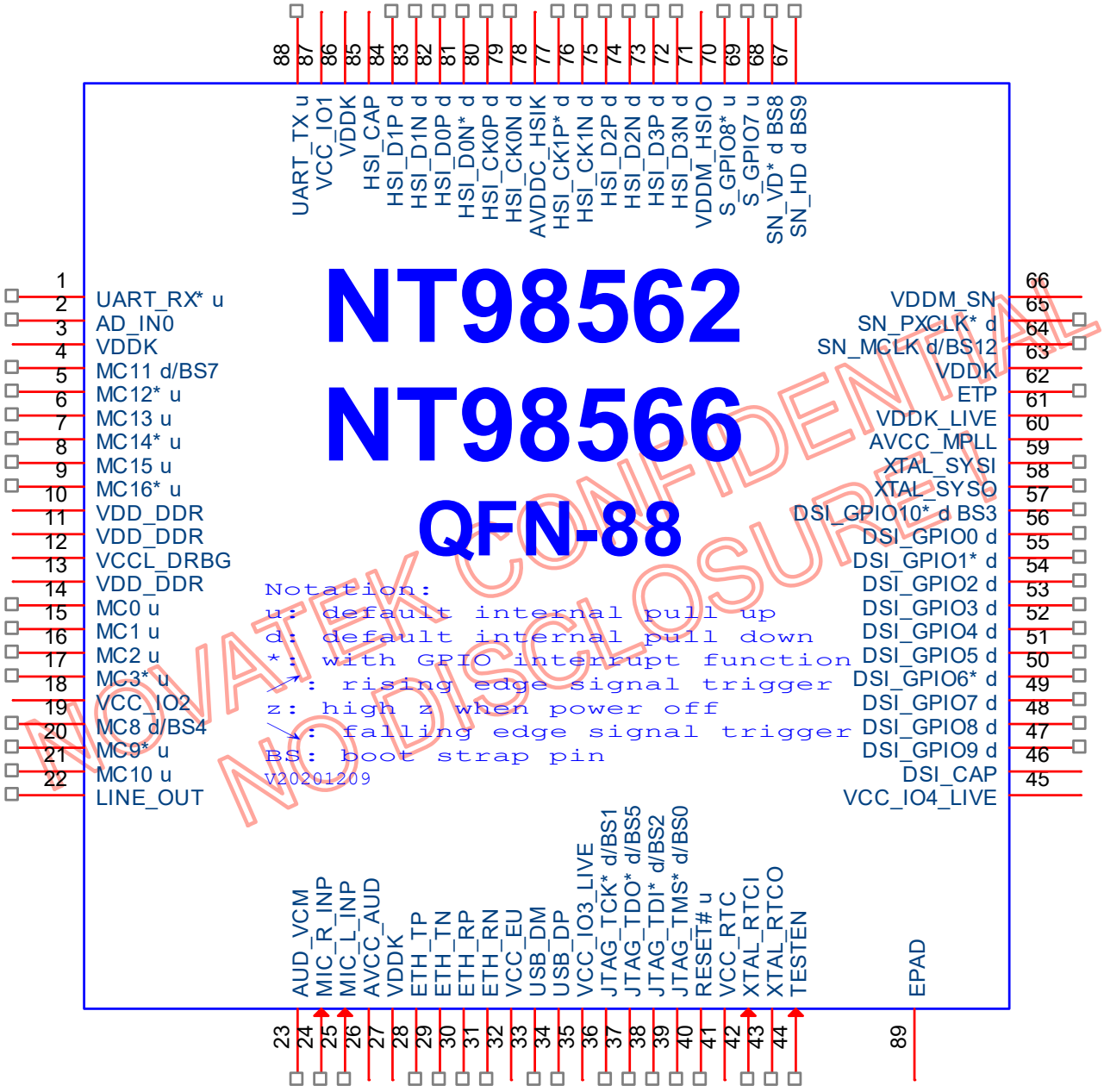
General Description(NT98566)

Novatek NT98566 is a highly-integrated SoC with high image quality, low bitrate, low power consumption, targets on 4Mp to 5Mp Edge-IP camera application. The SoC integrates ARM Cortex A9 CPU core, new generation ISP, H.265/H.264 video compression codec, high performance hardware DLA module, graphic engine, display controller, Ethernet PHY, USB 2.0 Host/Device, audio codec, RTC and SD/SDIO 3.0 to provide best cost performance Edge-IP camera solution.

Block Diagram



Pin Configuration



Pin Configuration

1.

QFN-88

Pin	Pin Name	Pin	Pin Name	Pin	Pin Name	Pin	Pin Name
1	UART_RX	23	AUD_VCM	45	VCC_IO4	67	SN_HD
2	AD_IN0	24	MIC_R_INP	46	DSI_CAP	68	SN_VD
3	VDDK	25	MIC_L_INP	47	DSI_GPIO9	69	S_GPIO7
4	MC11	26	AVCC_AUD	48	DSI_GPIO8	70	S_GPIO8
5	MC12	27	VDDK	49	DSI_GPIO7	71	VDDM_HSIO
6	MC13	28	ETH_TP	50	DSI_GPIO6*	72	HSI_D3N
7	MC14	29	ETH_TN	51	DSI_GPIO5	73	HSI_D3P
8	MC15	30	ETH_RP	52	DSI_GPIO4	74	HSI_D2N
9	MC16	31	ETH_RN	53	DSI_GPIO3	75	HSI_D2P
10	VDD_DDR	32	VCC_EU	54	DSI_GPIO2*	76	HSI_CK1N
11	VDD_DDR	33	USB_DM	55	DSI_GPIO1	77	HSI_CK1P
12	VCCL_DRBG	34	USB_DP	56	DSI_GPIO0	78	AVDDC_HSIK
13	VDD_DDR	35	VCC_IO3	57	DSI_GPIO10	79	HSI_CK0N
14	MC0	36	JTAG_TCK	58	XTAL_SYSO	80	HSI_CK0P
15	MC1	37	JTAG_TDO	59	XTAL_SYSI	81	HSI_D0N
16	MC2	38	JTAG_TDI	60	AVCC_MPLL	82	HSI_D0P
17	MC3	39	JTAG_TMS	61	VDDK	83	HSI_D1N
18	VCC_IO2	40	RESET#	62	ETP	84	HSI_D1P
19	MC8	41	VCC_RTC	63	VDDK	85	HSI_CAP
20	MC9	42	XTAL_RTCO	64	SN_MCLK	86	VDDK
21	MC10	43	XTAL_RTCI	65	SN_PXCLK	87	VCC_IO1
22	LINE_OUT	44	TESTEN	66	VDDM_SN	88	UART_TX
89	**EPAD / GND**						

Pin Descriptions

I = input port with Schmitt trigger

O = output port with normal driving/sinking

I/O = bi-directional port with normal driving/sinking and Schmitt input

I/O_D = bi-directional port with open drain output and Schmitt input

mvI/O = multi voltage bi-direction port with Schmitt input

I/O_{5VT} = bi-directional port with normal driving/sinking and 5V tolerance input

I/O = bi-direction port with different driving/sinking capability

HSI = high speed serial interface with multi voltage input port

LVD = low voltage detect function pin

p/u = internal pull-up

p/d = internal pull-down

AI = analog input port

AO = analog output port

AI/O = analog bi-directional port

H = output high

L = output low

P = power or ground

Note: * means this pin has interrupted function.

2. NT98562 88 pins

Total:88 pins

2.1. System interface (8)

Pin No.	Name	Type	Reset	Descriptions
59	XTAL_SYSI	AI	-	Crystal input for system oscillator. (12MHz)
58	XTAL_SYSO	AO	-	Output for system oscillator.
40	RESET#	LVD	p/u	System Reset. Connect a capacitor to ground for reset time control.
44	TESTEN	I	I p/d	Enable test mode. Keep low for normal operation.
39	JTAG_TMS / DGPIO3* / BS0	I/O	I p/d	CPU's JTAG test interface / BS2..0 : **BOOT_SRC** Note: BOOT_SRC BS3 pin is LCD0 The boot source BS3..0 setting description: 0x0: SPI_NOR 0x1: SDIO 0x2: SPI_NAND with on die ECC(2 kbytes) 0x3: SPI_NAND with RS ECC(2 kbytes) 0x4: ETHERNET 0x5: USB high speed 0x6: SPI_NAND with on die ECC(4 kbytes) 0x7: Reserved 0x8: eMMC(4 bits data bus) 0x9: eMMC(8 bits data bus) 0xA: SPI_NAND with RS ECC(4 kbytes) 0xB: USB full speed 0xC: UART Others: Reserved
36	JTAG_TCK / DGPIO4* / BS1	I/O	I p/d	
38	JTAG_TDI / DGPIO5* / BS2	I/O	I p/d	
37	JTAG_TDO / DGPIO6* / BS5	I/O	I p/d	CPU's JTAG test interface / BS5 : **EJTAG_SEL** EJTAG select 0: GPIO (TRST, TMS, TCK, TDI, TDO are GPIO) 1: EJTAG (assign **EJTAG_CH_SEL** to JTAG on boot) [**Note**] When (EJTAG_SEL **=** 1), EJTAG function pin out priority is higher than others

2.2. RTC & Power Button Controller (2)

Pin No.	Name	Type	Default	Descriptions
42	XTAL_RTCI	AI	-	Crystal input for real time clock oscillator. (32.768KHz).
43	XTAL_RTCO	AO	-	Output for real time clock oscillator.

2.3. Sensor interface (19)

Pin No.	Name	Type	Reset	Descriptions
85	HSI_CAP	P	-	Internal Supply Voltage decoupling for HSI circuit

81	HSI_D0N / HSI_GPIO0*	HSI	I p/d	High speed differential sensor interface and parallel interface. (When sensor interface is configured as high speed differential sensor interface, the clock lane should be a dedicated differential lane. And each data lanes may be permuted in established group, refer to below table)
82	HSI_D0P / HSI_GPIO1			
83	HSI_D1N / HSI_GPIO2			
84	HSI_D1P / HSI_GPIO3			
79	HSI_CK0N / HSI_GPIO4			
80	HSI_CK0P / HSI_GPIO5			
74	HSI_D2N / HSI_GPIO6			
75	HSI_D2P / HSI_GPIO7			
72	HSI_D3N / HSI_GPIO8			
73	HSI_D3P / HSI_GPIO9			
76	HSI_CK1N / HSI_GPIO10			
77	HSI_CK1P / HSI_GPIO11*			
64	SN_MCLK / S_GPIO[0] / BS12	mvI/O	I p/d	Programmable Clock output for sensor BS12 : **WDT_FAIL_RESET_FUNC** Enable WDT fail reset function. Enable this function can skip internal storage when internal storage boot failed. (boot from SPI nand/SPI nor /eMMC) 0: Enable 1: Disable
65	SN_PXCLK / SN2_MCLK / S_GPIO[1]*	mvI/O	I p/d	Sensor Pixel Clock Input Programmable Clock output for sensor 2
68	SN_VD / S_GPIO[2]* / BS8	mvI/O	I p/d	Sensor Vertical and Horizontal Sync input / output BS9..8 : **ETH_MODE_SEL** (Only referred by f/w) The boot source BS9..8 setting description: 0: Embedded PHY 1: RMII (refclk output mode) 2: RMII (refclk input mode) 3: Reserved
67	SN_HD / S_GPIO[3] / BS9	mvI/O	I p/d	
69	S_GPIO[7] / SN_SCK / I2C_SCL	mvI/O_D	I p/u	General serial interface 0 clock output. I2C-BUS clock output(Open Drain IO structure)
70	S_GPIO[8] / SN_DAT / I2C_SDA	mvI/O_D	I p/u	General serial interface 0 data output. I2C-BUS data input / output(Open Drain IO structure)

Note*: The pin can trigger interrupt.

Note1 : The input voltage of HSI_GPI corresponds to VDDM_HSIO.

Note2 : The mvI/O voltage of Sensor interface corresponds to VDDM_SN.

Name	MIPI/LVDS/HiSPi (1C4D)		MIPI / HiSPi SIE1 & 2 (1C2Dx2)		Parallel SIE1 (RAW12)		CCIR601 SIE1 (8 bits)					
HSI_GPI[0]	HSI_D0N	I	HSI_D0N	I	SN_D2	I						
HSI_GPI[1]	HSI_D0P	I	HSI_D0P	I	SN_D3	I						
HSI_GPI[2]	HSI_D1N	I	HSI_D1N	I	SN_D4	I	SN_YC0	I				
HSI_GPI[3]	HSI_D1P	I	HSI_D1P	I	SN_D5	I	SN_YC1	I				
HSI_GPI[4]	**HSI_CK0N**	I	**HSI_CK0N**	I	SN_D6	I	SN_YC2	I				
HSI_GPI[5]	**HSI_CK0P**	I	**HSI_CK0P**	I	SN_D7	I	SN_YC3	I				
HSI_GPI[6]	HSI_D2N	I	HSI2_D0N	I	SN_D8	I	SN_YC4	I				
HSI_GPI[7]	HSI_D2P	I	HSI2_D0P	I	SN_D9	I	SN_YC5	I				
HSI_GPI[8]	HSI_D3N	I	HSI2_D1N	I	SN_D10	I	SN_YC6	I				
HSI_GPI[9]	HSI_D3P	I	HSI2_D1P	I	SN_D11(MSB)	I	SN_YC7	I				
HSI_GPI[10]			**HSI2_CK0N**	I	SN_D0	I						
HSI_GPI[11]			**HSI2_CK0P**	I	SN_D1(LSB)	I						
S_GPIO[0]	SN_MCLK	O	SN_MCLK	O	SN_MCLK	O	SN_MCLK	O				
S_GPIO[1]	SN_PXCLK	I	SN2_MCLK	I	SN_PXCLK	I	SN_PXCLK	I				
S_GPIO[2]	SN_VD	I	SN_VD	I	SN_VD	I/O	SN_VD	I				
S_GPIO[3]	SN_HD	I	SN_HD	I	SN_HD	I/O	SN_HD	I				

2.4. Memory Card interface (13)

Pin No.	Name	Type	Reset	Descriptions
14	MC0 / C_GPIO[0]	I/O	I p/u	Memory Card interface(see below table)
15	MC1 / C_GPIO[1]	I/O	I p/u	
16	MC2 / C_GPIO[2]	I/O	I p/u	
17	MC3 / C_GPIO[3]*	I/O	I p/u	
19	MC8 / C_GPIO[8] / BS4	I/O	I p/d	Memory Card interface / BS4: **EJTAG_CH_SEL** EJTAG channel select 0: EJTAG_1 (assign DGPIO2~DGPIO6 to JTAG) 1: EJTAG_2 (assign MC2,MC3,P_GPIO23,P_GPIO24 to JTAG)
20	MC9 / C_GPIO[9]*	I/O	I p/u	Memory Card interface(see below table)
21	MC10 / C_GPIO[10]	I/O	I p/u	
4	MC11 / C_GPIO[11] / BS7	I/O_{SD}	I p/d	Memory Card interface / **BS7 DSI_PROT_EN** Enable DSI function 0: DSI PHY function disabled 1: DSI PHY function available
5	MC12 / C_GPIO[12]*	I/O_{SD}	I p/u	Memory Card interface(see below table)
6	MC13 / C_GPIO[13]	I/O_{SD}	I p/u	

7	MC14 / C_GPIO[14]*	I/O_{SD}	I p/u	
8	MC15 / C_GPIO[15]	I/O_{SD}	I p/u	
9	MC16 / C_GPIO[16]*	I/O_{SD}	I p/u	

Note*: The pin can trigger interrupt.

Memory card interface pinmux table

Name	SD/MMC/eMMC (BS*)		SPI flash(1~4 bits) (BS*)									
MC0	eMMC_D0	I/O	SPI_DO/D0	I/O								
MC1	eMMC_D1	I/O	SPI_DI/D1	I/O								
MC2	eMMC_D2	I/O	SPI_WP/D2	I/O								
MC3	eMMC_D3	I/O	SPI_HOLD/D3	I/O								
MC8	eMMC_CLK	O	SPI_CLK	O								
MC9	eMMC_CMD	I/O										
MC10	eMMC_RST#		SPI_CS#	O								
Name	SD Card (BS*)											
MC11	SD_CLK	O	SPI3_2_CLK	O	PWM4_2	O	I2C3_2_SCL	O	I2S_MCLK_2	O	DMCLK_3	O
MC12	SD_CMD	I/O	SPI3_2_DO/D0 /DIO	IO	PWM5_2	O	I2C3_2_SDA	IO	I2S_BCLK_2	IO	DMDAT0_3	I
MC13	SD_D0	I/O	SPI3_2_CS	O	PWM0_2	O	Uart2_2_CTS	I	I2S_SYNC_2	IO	DMDAT1_3	I
MC14	SD_D1	I/O	SPI3_2_DI/D1	IO	PWM1_2	O	Uart2_2_RTS	O	I2S_SDATAO_2	O		
MC15	SD_D2	I/O	SPI3_2_RDY	I	PWM2_2	O	Uart2_2_TX	O	I2S_SDATAI_2	I		
MC16	SD_D3	I/O			PWM3_2	O	Uart2_2_RX	I				

Note BS*: In general, it is a resident device. Please choose one of them as boot source(FW).

2.5. UART interface (2)

Pin No.	Name	Type	Reset	Descriptions
88	P_GPIO[23] / UART_TX	I/O_{5VT}	O	UART Transmit
1	P_GPIO[24]* / UART_RX	I/O_{5VT}	I p/u	UART Receive

2.6. ADC interface (1)

Pin No.	Name	Type	Reset	Descriptions
2	AD_IN0 / AGPIO0	AIO	-	General ADC 0 Input with buffer Gerneal Purpose IO

2.7. Audio Codec(4)

Pin No.	Name	Type	Reset	Descriptions
23	AUD_VCM	AO	-	Decoupling for audio codec reference voltage.
24	MIC_R_INP	AI	-	Right channel microphone differential input positive side.
25	MIC_L_INP	AI	-	Left channel microphone differential input positive side.
22	LINE_OUT	AO	-	Right channel Line output.

2.8. Ethernet interface (4)

Pin No.	Name	Type	Reset	Descriptions
28	ETH_TP	AIO	-	Ethernet transmitter differential pair
29	ETH_TN	AIO	-	Ethernet transmitter differential pair
30	ETH_RP	AIO	-	Ethernet receiver differential pair
31	ETH_RN	AIO	-	Ethernet receiver differential pair

2.9. USB device interface (2)

Pin No.	Name	Type	Reset	Descriptions
34	USB20_DP	AI/O	-	USB2.0 FS/HS Differential Data Plus (D+)
33	USB20_DM	AI/O	-	USB2.0 FS/HS Differential Data Minus (D-)

2.10. DSI GPIO (12)

Pin No.	Name	Type	Reset	Descriptions
46	DSI_CAP	P	-	Internal Supply Voltage decoupling for DSI GPIO
56	DSI_GPIO0	AIO	-	MIPI DSI differential clock lane output
55	DSI_GPIO1	AIO	-	
54	DSI_GPIO2*	AIO	-	MIPI DSI differential data lane input / output
53	DSI_GPIO3	AIO	-	
52	DSI_GPIO4	AIO	-	
51	DSI_GPIO5	AIO	-	
50	DSI_GPIO6*	AIO	-	
49	DSI_GPIO7	AIO	-	
48	DSI_GPIO8	AIO	-	
47	DSI_GPIO9	AIO		
57	DSI_GPIO10* / BS3	AIO	-	DSI_GPIO10/ BS3 : **BOOT_SRC** The boot source setting table is shown in JTAG interface.

2.11. Power (21)

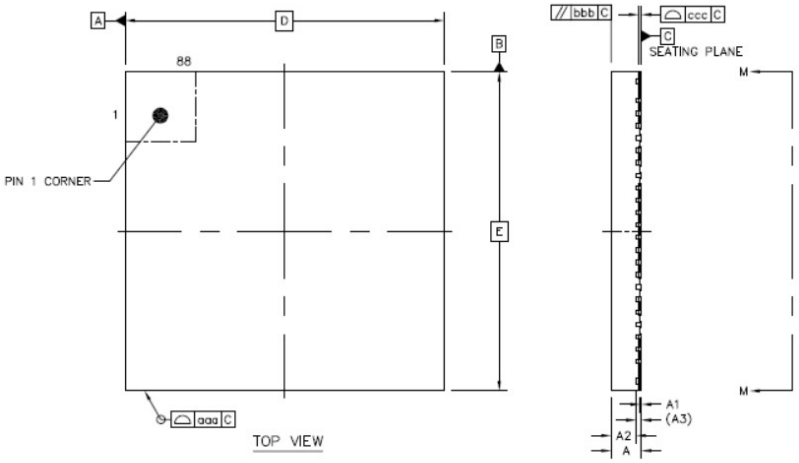
Pin No.	Name	Type	Descriptions
3, 27, 61, 63, 86	VDDK(5)	P	Core Power
87	VCC_IO1	P	General 3.3V I/O Pad Power
18	VCC_IO2	P	General 3.3V I/O Pad Power
35	VCC_IO3	P	General 3.3V I/O Pad Power
45	VCC_IO4	P	General 3.3V I/O Pad Power
12	VCCL_DRBG	P	3.3V Bandgap power for Main DRAM PHY
10,11,13	VDD_DDR	P	DRAM power
60	AVCC_MPLL	P	Analog 3.3V power for Multi-PLL
41	VCC_RTC	P	RTC Power
78	AVDDK_HSI	P	Analog core power for HSI PHY
71	VDDM_HSIO	P	Multi-level input power for HSI Input
66	VDDM_SN	P	Multi-level IO power for sensor interface
26	AVCC_AUD	P	Analog 3.3V power for Audio Codec

32	VCC_EU	P	3.3V power for Ethernet and USB interface
62	ETP	-	Connected 100K Ohm resistor to ground

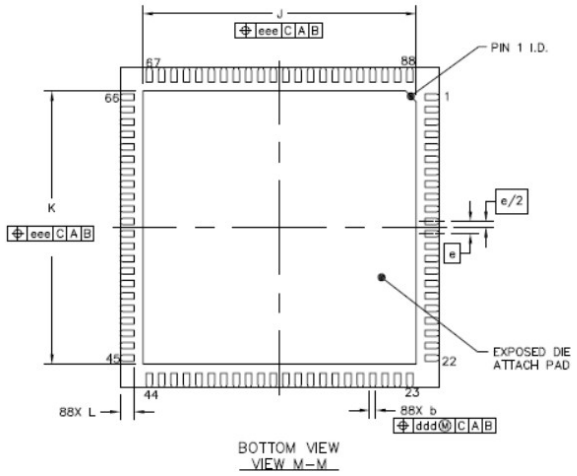
Package Information

3.

QFN-88



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.8	0.85	0.9
STAND OFF		A1	0	0.035	0.05
MOLD THICKNESS		A2	---	0.7	---
L/F THICKNESS		A3		0.152 REF	
LEAD WIDTH		b	0.13	0.18	0.23
BODY SIZE	X	D		9 BSC	
	Y	E		9 BSC	
LEAD PITCH		e		0.35 BSC	
EP SIZE	X	J	7.6	7.7	7.8
	Y	K	7.6	7.7	7.8
LEAD LENGTH		L	0.35	0.4	0.45
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		bbb		0.1	
COPLANARITY		ccc		0.08	
LEAD OFFSET		ddd		0.1	
EXPOSED PAD OFFSET		eee		0.1	



NOTES

1.0 COPLANARITY APPLIES TO LEADS, CORNER LEADS AND DIE ATTACH PAD.
2.0 TOTAL THICKNESS NOT INCLUDE SAW BURR.

Ordering Information

Item \ Part No.	NT98562	NT98566
Package	QFN-88 9x9 mm^2	QFN-88 9x9 mm^2
SIP KGD	512Mb DRAM	1Gb DRAM

Important Notice

NT98562 is a product that is not specifically designed and marketed, and shall not be directly and/or knowingly sold or used as to be incorporated into, any of the following products:

(i) military products or proliferation application (including but not limited to missiles, nuclear, chemical and biological weapons); or

(ii) commercial space products or applications that are controlled under the U.S. Munitions List (USML); or

(iii) medical appliances; and

(iv) automotive driver safety assistant system

furthermore, NT98562 shall not be directly and knowingly shipped to any country subject to "embargo" or exported to, re-exported to, transferred to, or used by any restricted entity, including but not limited to those listed on the U.S. Department of Commerce Entity List, under the U.S. laws and or its applicable regulations (e.g., the U.S. Export Administration Regulations) in effect from time to time.