R&T BiCMOS run2

Low Noise, Cryogenic Differential Amplifier

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DESCRIPTION

This ASIC, fabricated using IHP technology, integrates three distinct circuits designed for cryogenic operation (77 K). It features two low-noise differential amplifiers: a fully integrated version with on-chip resistors and a flexible version utilizing external resistors. Both amplifiers deliver an ultralow noise floor of $1\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$ and are optimized for promising low flicker noise at cryogenic temperatures. The bandwidth is specified at $25\,\mathrm{MHz}$ for the on-chip variant and $50\,\mathrm{MHz}$ for the external resistor configuration. Additionally, a large-geometry

NMOS transistor ($W/L \approx 190,000$) is included for discrete characterization.

ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (V^+ to V^-)   5.15V

Input Current (Note 2) $\pm$40mA

Operating Junction Temperature Range
(Note 5) -40°C to 125°C

BLOCK DIAGRAM
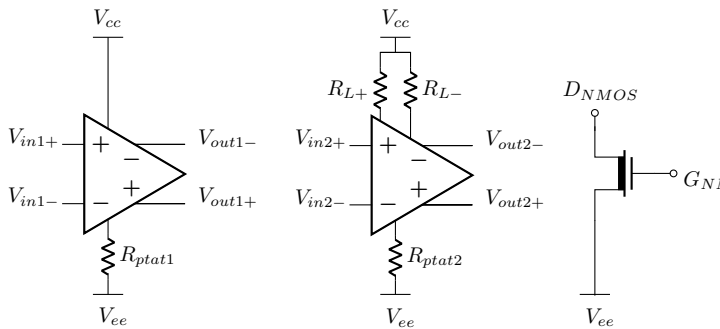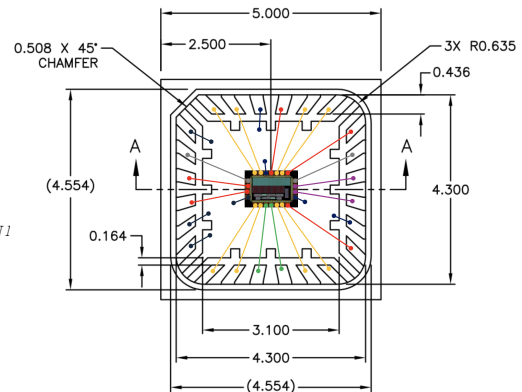

LNA 1   LNA 2   NMOS Block

PACKAGE

Bonding diagram with QFN24 package

TABLE 1: ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	NOTES	$\mathbf{T_A = 27^\circ C}$			SUB-GROUP	$\mathbf{-55^\circ C \le T_A \le 125^\circ C}$			SUB-GROUP	UNITS
				MIN	TYP	MAX		MIN	TYP	MAX		
V_{OS}	Input Offset	$V_S = \pm1.65$V			0.6	2	1			4	2,3	mV
	Voltage	$V_{CM} = V^-$ to V^+			2.5	6	1			9	2,3	mV
I_B	Input Bias	$V_S = \pm1.65$V			8	18	1			20	2,3	μA
	Current	$V_{CM} = V^+$		-50	-23		1	-100			2,3	μA
	Input Noise	$0.1\,Hz$ to $10\,Hz$			8	18	1			20	2,3	μA
	Voltage	$V_{CM} = V^+$		-50	-23		1	-100			2,3	nV_{p-p}
SR	Slew Rate	$V_{in} \pm 1.25\,mV$ — LNA1		28	30	31	1	29	30	32	2,3	$V/\mu s$
		$V_{in} \pm 1.25\,mV$ — LNA2		39	36	42	1	38	39	40	2,3	$/\mu s$

Slew Rate Measurement

Example of signal response @27° C
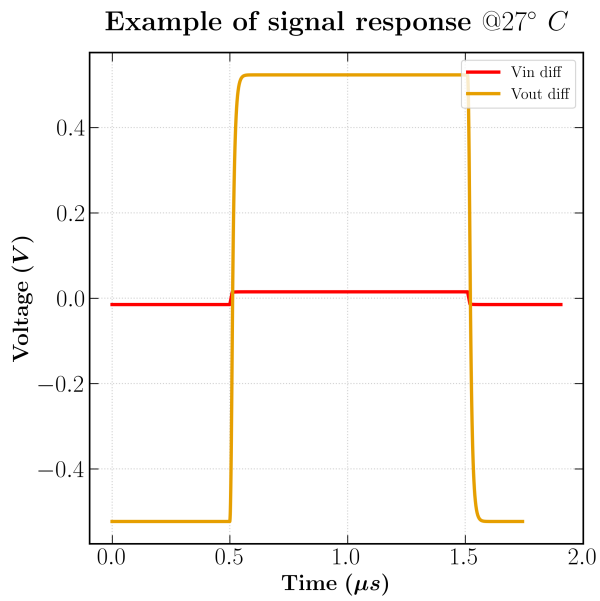
Figure 1: Output Response

Slew Rate Calculate (10% − 90%) Example

Figure 3: Slew Rate Estimation

Slew Rate vs Temperature
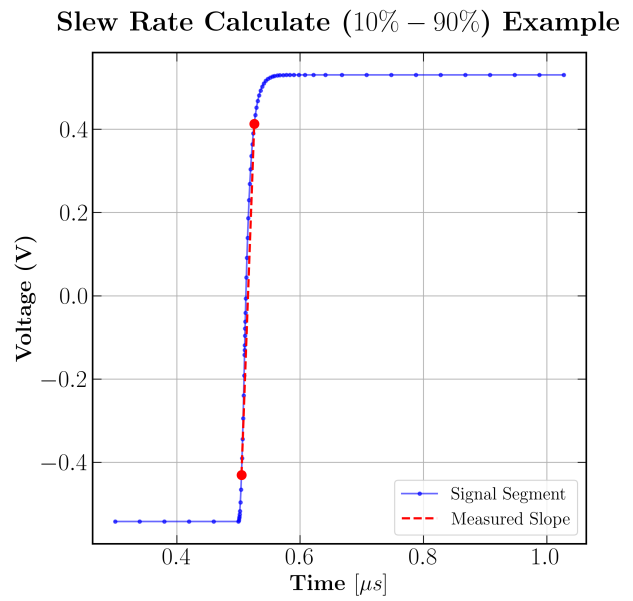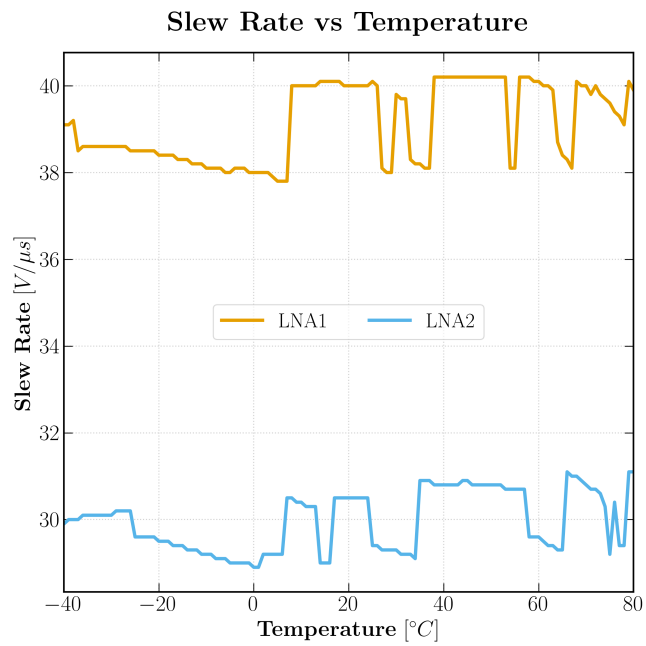

Figure 2: Slew Rate
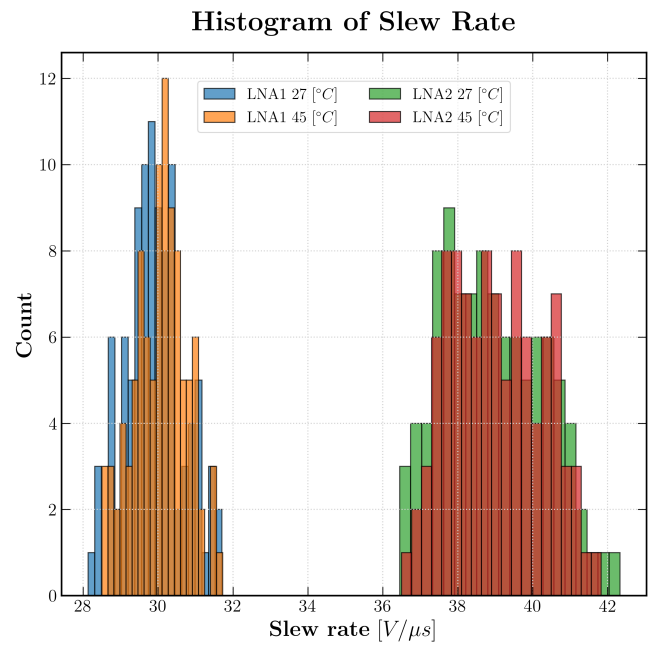
Histogram of Slew Rate

Figure 4: Slew Rate Histogram
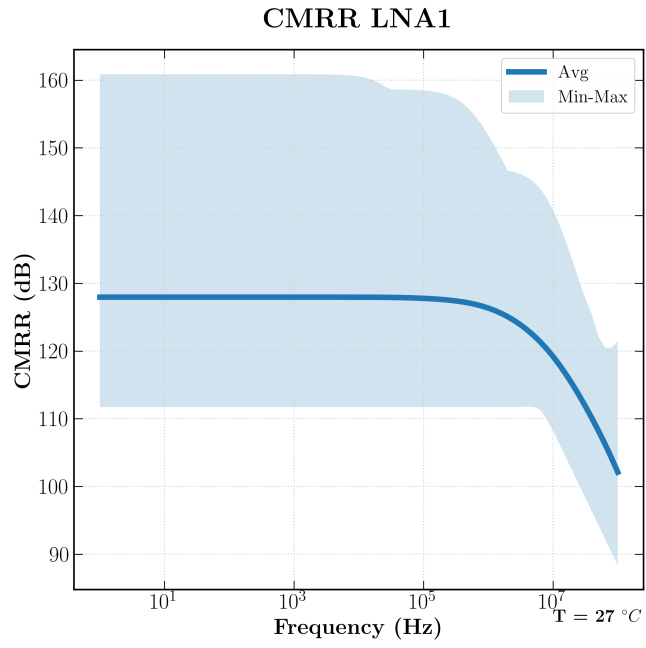
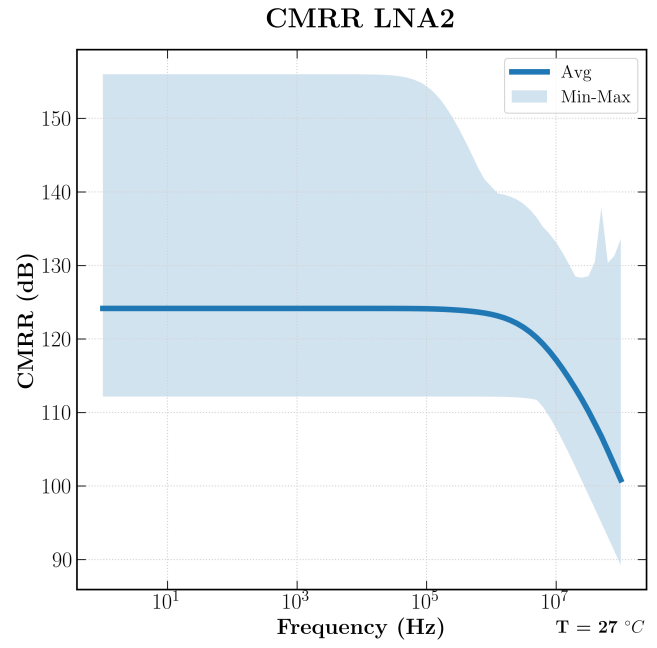## Common-mode Rejection Ratio (CMRR)

Figure 5: CMRR LNA1

Figure 6: CMRR LNA2

Power Suppy Rejection Ratio

PSRR LNA1 (VCC)

Figure 7: PSRR LNA1 VCC

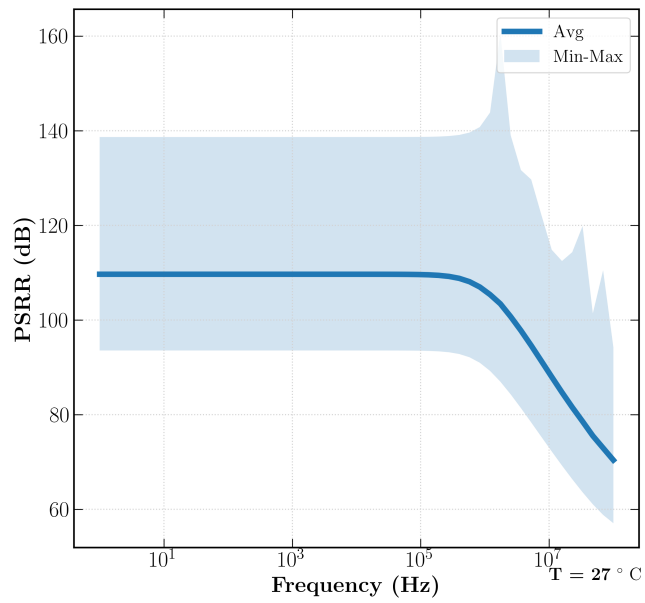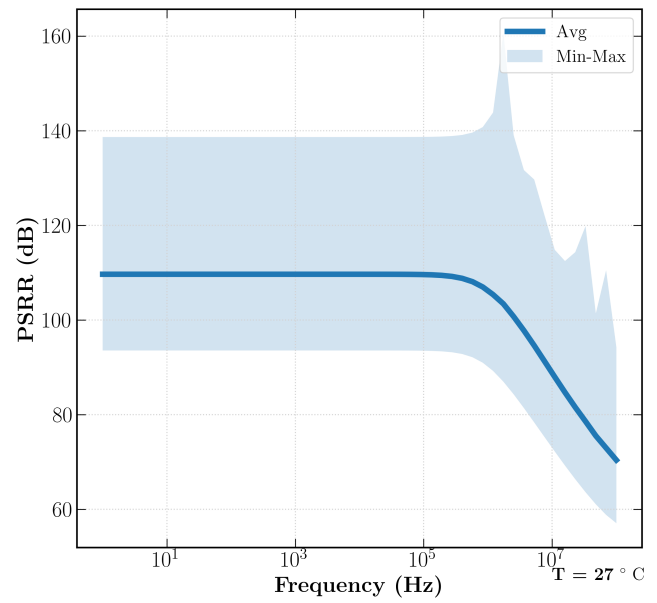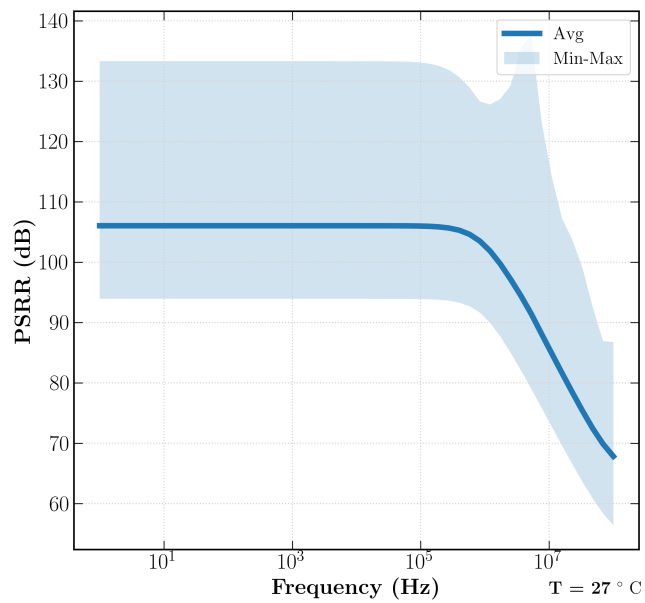### PSRR LNA1 (VCC)

Figure 8: PSRR LNA1 VCC

PSRR LNA2 (VCC)

PSRR LNA2 (VEE)