



R&T BiCMOS run2

Low Noise, Cryogenic Differential Amplifier

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DESCRIPTION

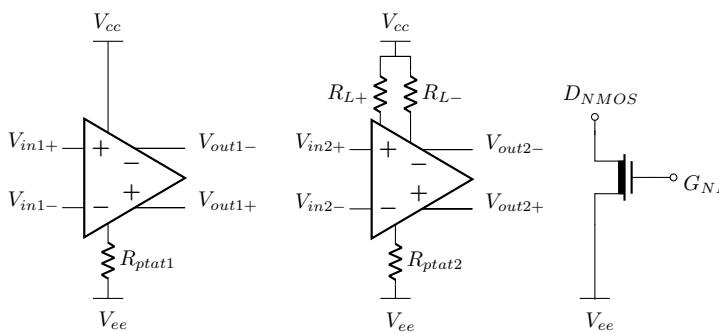
This ASIC, fabricated using IHP technology, integrates three distinct circuits designed for cryogenic operation (77 K). It features two low-noise differential amplifiers: a fully integrated version with on-chip resistors and a flexible version utilizing external resistors. Both amplifiers deliver an ultralow noise floor of $1 \text{ nV}/\sqrt{\text{Hz}}$ and are optimized for promising low flicker noise at cryogenic temperatures. The bandwidth is specified at 25 MHz for the on-chip variant and 50 MHz for the external resistor configuration. Additionally, a large-geometry

NMOS transistor ($W/L \approx 190,000$) is included for discrete characterization.

ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (V^+ to V^-)	5.15V
Input Current (Note 2)	$\pm 40\text{mA}$
Operating Junction Temperature Range (Note 5)	-40°C to 125°C

BLOCK DIAGRAM

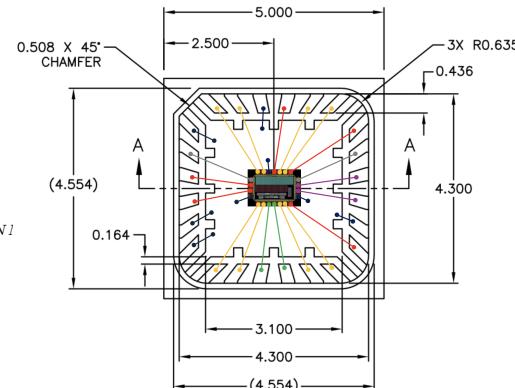


LNA 1

LNA 2

NMOS Block

PACKAGE



Bonding diagram with QFN24 package

TABLE 1: ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	NOTES	$T_A = 27^\circ\text{C}$			SUB-GROUP	$-55^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$			SUB-GROUP	UNITS
				MIN	TYP	MAX		MIN	TYP	MAX		
V_{OS}	Input Offset Voltage	$V_S = \pm 1.65\text{V}$ $V_{CM} = V^-$ to V^+		0.6	2	1	1	4	2,3	mV	2,3	mV
				2.5	6	1		9	2,3	mV		
I_B	Input Bias Current	$V_S = \pm 1.65\text{V}$ $V_{CM} = V^+$		8	18	1	1	20	2,3	μA	2,3	μA
		0.1 Hz to 10 Hz $V_{CM} = V^+$	-50	-23				-100	20	2,3	μA	
SR	Input Noise Voltage	$0.1 \text{ Hz to } 10 \text{ Hz}$ $V_{CM} = V^+$		8	18	1	1	20	2,3	μA	2,3	nV_{p-p}
	Slew Rate	$V_{in} \pm 1.25 \text{ mV} — \text{LNA1}$ $V_{in} \pm 1.25 \text{ mV} — \text{LNA2}$		28	30	31		29	30	32		
				39	36	42	1	38	39	40	2,3	/ μs

TYPICAL PERFORMANCE CHARACTERISTICS