



R&T BiCMOS run2

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DESCRIPTION

This ASIC, fabricated using IHP technology, integrates three distinct circuits designed for cryogenic operation (77 K). It features two low-noise differential amplifiers: a fully integrated version with on-chip resistors and a flexible version utilizing external resistors. Both amplifiers deliver an ultralow noise floor of $1 \text{ nV}/\sqrt{\text{Hz}}$ and are optimized for promising low flicker noise at cryogenic temperatures. The bandwidth is specified at 25 MHz for the on-chip variant and 50 MHz for the external resistor configuration. Additionally, a large-geometry

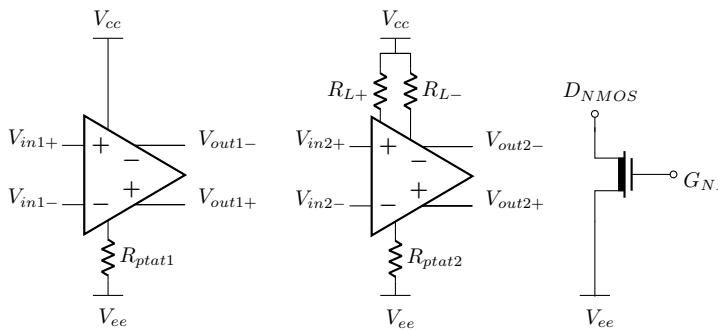
Low Noise, Cryogenic Differential Amplifier

NMOS transistor ($W/L \approx 190,000$) is included for discrete characterization.

ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (V^+ to V^-)	5.15V
Input Current (Note 2)	$\pm 40 \text{ mA}$
Operating Junction Temperature Range (Note 5)	-40°C to 125°C

BLOCK DIAGRAM

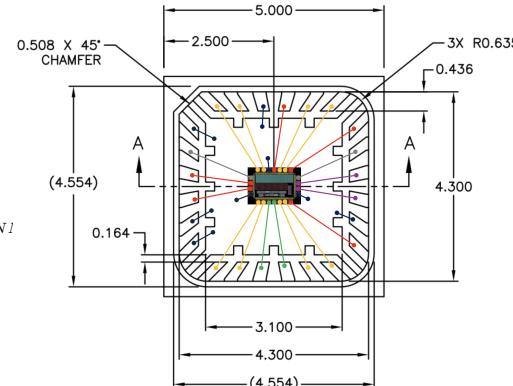


LNA 1

LNA 2

NMOS Block

PACKAGE



Bonding diagram with QFN24 package

TABLE 1: ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	NOTES	$T_A = 27^\circ\text{C}$			SUB-GROUP	$-55^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$			SUB-GROUP	UNITS
				MIN	TYP	MAX		MIN	TYP	MAX		
V_{OS}	Input Offset Voltage	$V_S = \pm 1.65\text{V}$ $V_{CM} = V^- \text{ to } V^+$		0.6	2	1		4		2,3		mV
				2.5	6	1		9		2,3		mV
I_B	Input Bias Current	$V_S = \pm 1.65\text{V}$ $V_{CM} = V^+$		8	18	1		20		2,3		μA
				-50	-23	1		-100		2,3		μA
	Input Noise Voltage	$0.1 \text{ Hz to } 10 \text{ Hz}$ $V_{CM} = V^+$		8	18	1		20		2,3		μA
				-50	-23	1		-100		2,3		nV_{p-p}
SR	Slew Rate	$V_{in} \pm 1.25 \text{ mV} — \text{LNA1}$ $V_{in} \pm 1.25 \text{ mV} — \text{LNA2}$		28	30	31	1	29	30	32	2,3	$\text{V}/\mu\text{s}$
				39	36	42	1	38	39	40	2,3	$/\mu\text{s}$
CMRR	Common-mode Rejection Ratio	$V_S \pm 1.65\text{V} — \text{LNA1}$ $V_S \pm 1.65\text{V} — \text{LNA2}$		112	128	161	1	110	128	163	2,3	dB
				112	124	156	1	110	123	147	2,3	dB
PSRR	Power Supply Rejection Ratio	$V_S \pm 1.65\text{V} — \text{LNA1}$ $V_S \pm 1.65\text{V} — \text{LNA2}$	VCC @1kHz VEE @1kHz VCC @1kHz VEE @1kHz	94	106	133	1				2,3	dB
				92	108	137	1				2,3	dB
				94	106	133	1				2,3	dB
				92	104	135	1				2,3	dB

Slew Rate Measurement

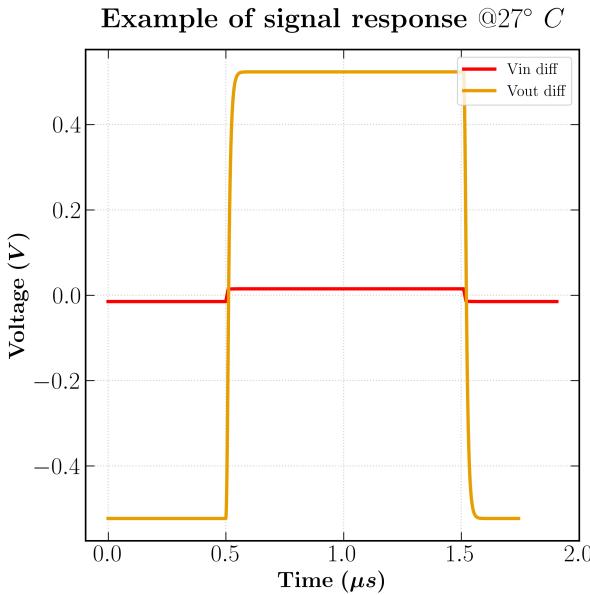


Figure 1: Output Response

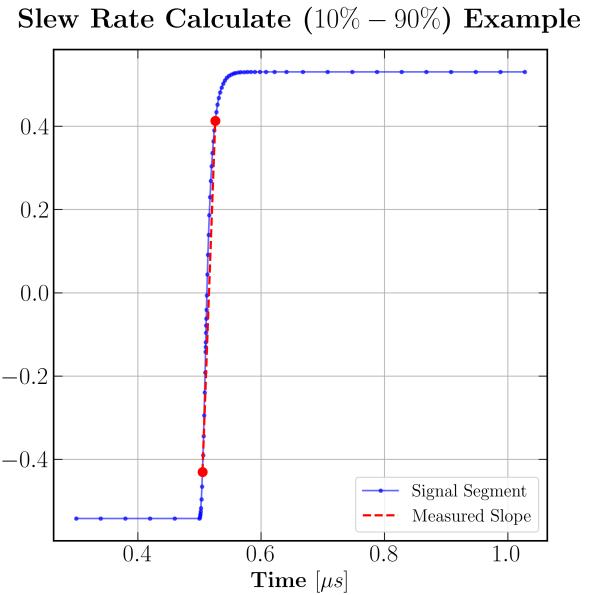


Figure 3: Slew Rate Estimation

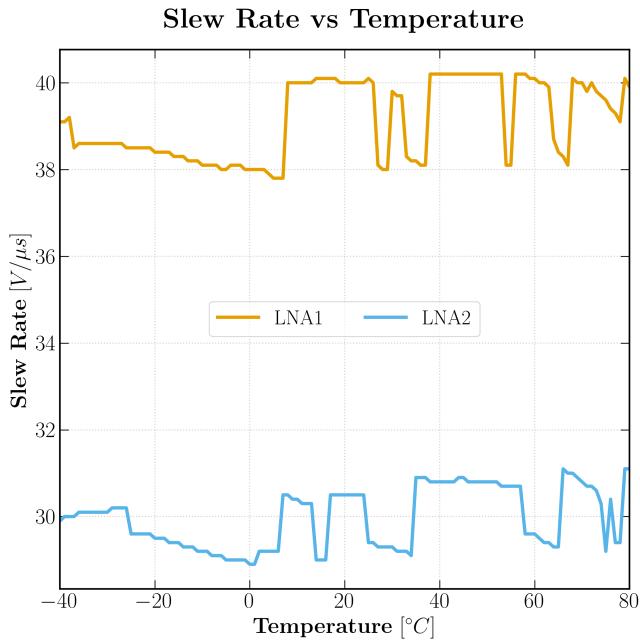


Figure 2: Slew Rate

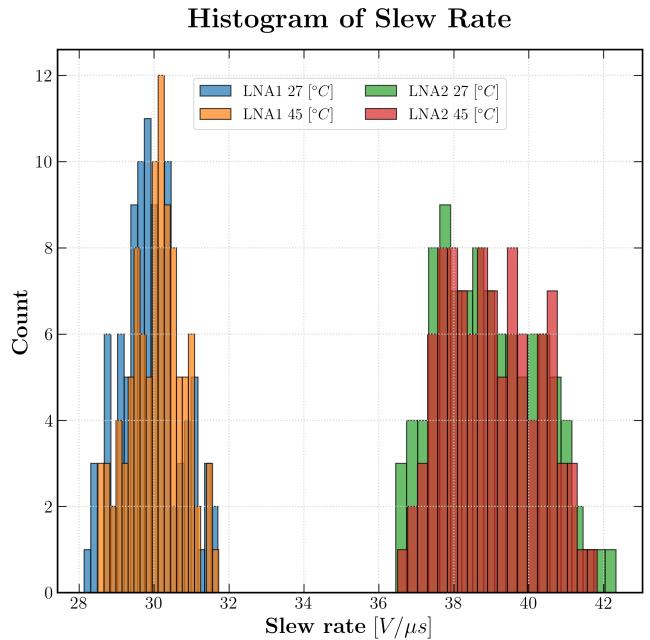


Figure 4: Slew Rate Histogram

Common-mode Rejection Ratio (CMRR)

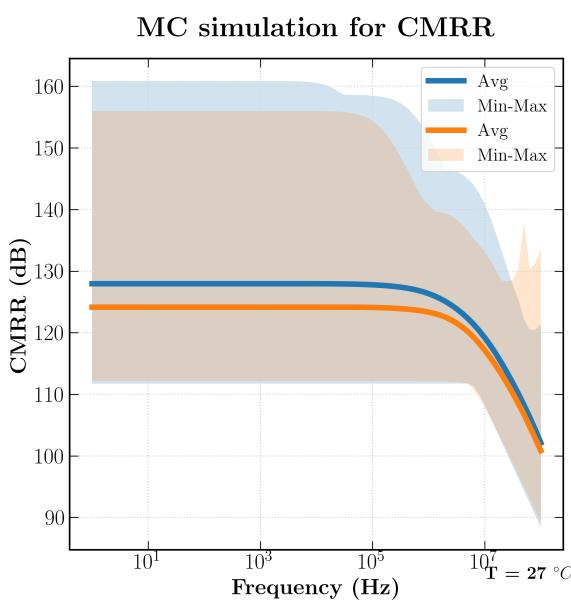


Figure 5: CMRR of LNA1/LNA2 vs Frequency (1 MHz to 100 MHz) at 27 °C

MC simulation CMRR vs T @ 1kHz

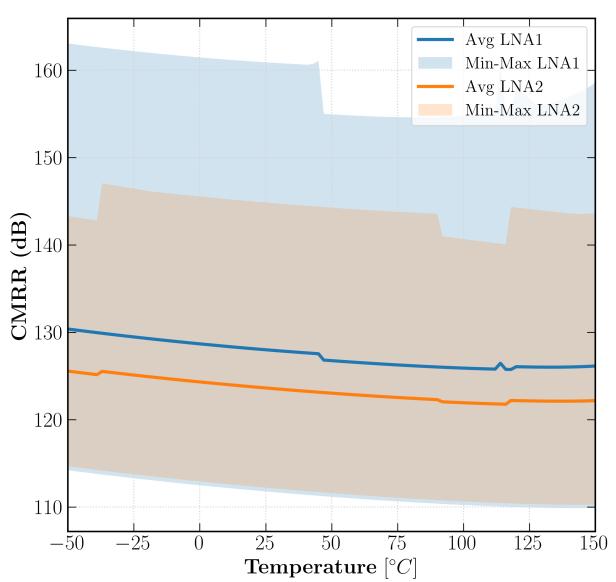


Figure 6: CMRR of LNA1/LNA2 vs Temperature (-50 °C to 150 °C) at 1 kHz

Power Supply Rejection Ratio (PSRR)

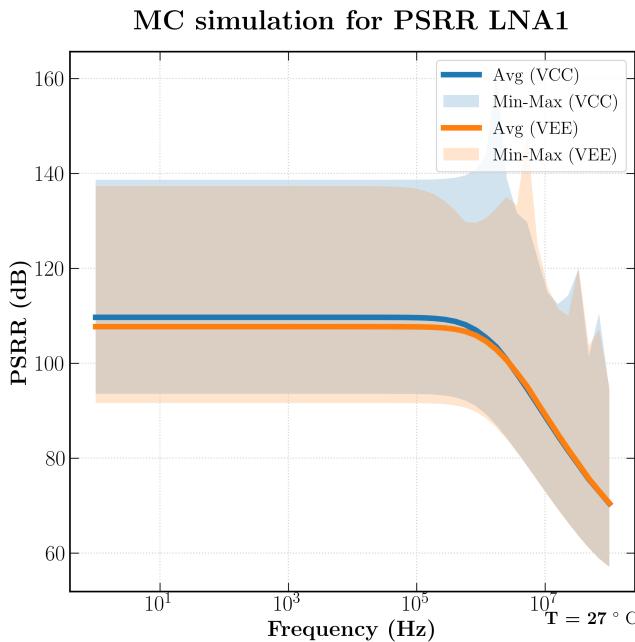


Figure 7: LNA1 PSRR (VCC, VEE) vs Frequency (1 MHz to 100 MHz) at 27 °C

MC simulation for PSRR LNA2

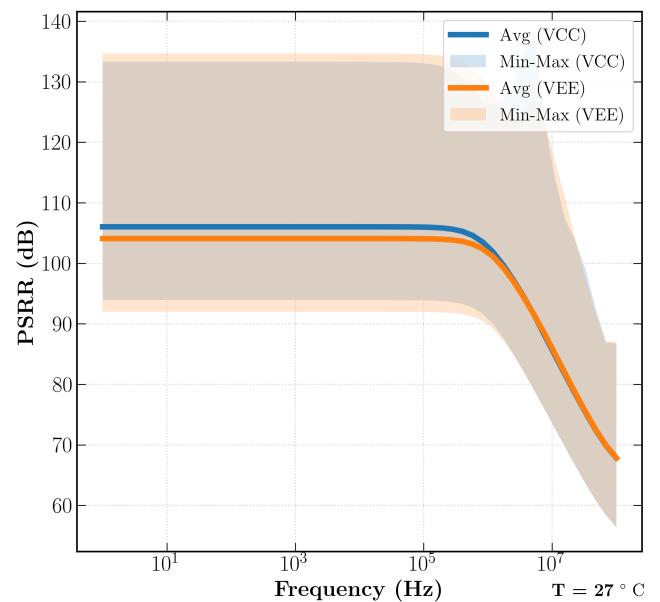


Figure 8: LNA2 PSRR (VCC, VEE) vs Frequency (1 MHz to 100 MHz) at 27 °C