R&T BiCMOS run2

Low Noise, Cryogenic Differential Amplifier

Prepared by: Bao TON

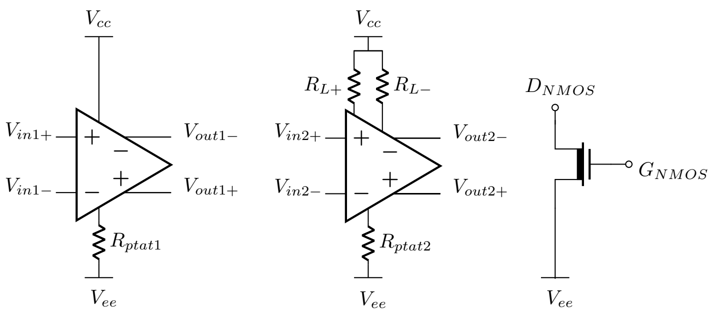
DESCRIPTION

This ASIC, fabricated using IHP technology, integrates three distinct circuits designed for cryogenic operation (77 K). It features two low-noise differential amplifiers: a fully integrated version with on-chip resistors and a flexible version utilizing external resistors. Both amplifiers deliver an ultralow noise floor of $1\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$ and are optimized for promising low flicker noise at cryogenic temperatures. The bandwidth is specified at 25 MHz for the on-chip variant and 50 MHz for the external resistor configuration. Additionally, a large-geometry NMOS transistor ($W/L \approx 190,000$) is included for discrete characterization.

ABSOLUTE MAXIMUM RATINGS

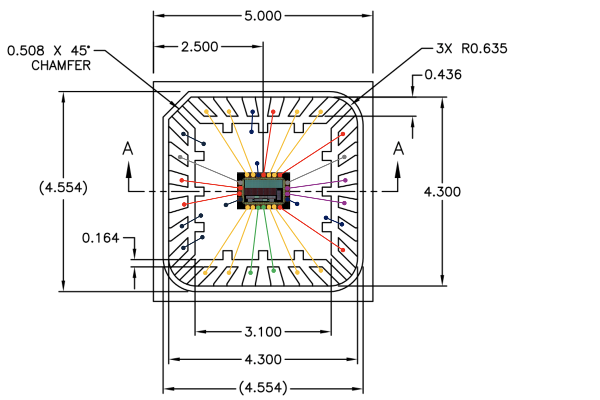
Total Supply Voltage (V^+ to V^-)	5.15V
Input Current (Note 2)	±40mA
Operating Junction Temperature Range (Note 5)	−40°C to 125°C

BLOCK DIAGRAM



LNA 1 LNA 2 NMOS Block

PACKAGE



Bonding diagram with QFN24 package

TABLE 1: ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	NOTES	$T_A = 27°C$			NOTES	$-55°C \le T_A \le 125°C$			SUB-GROUP	UNITS
				MIN	TYP	MAX		MIN	TYP	MAX		
V_{OS}	Input Offset	$V_S = \pm1.65V$			0.6	2				4	2,3	mV
	Voltage	$V_{CM} = V^-$ to V^+			2.5	6				9	2,3	mV
I_B	Input Bias	$V_S = \pm1.65V$			8	18				20	2,3	μA
	Current	$V_{CM} = V^+$		-50	-23			-100			2,3	μA
	Input Noise	$0.1\ Hz$ to $10\ Hz$			8	18				20	2,3	μA
	Voltage	$V_{CM} = V^+$		-50	-23			-100			2,3	nV_{p-p}
SR	Slew Rate	$V_{in} \pm 1.25\ mV$ — LNA1		28	30	31		29	30	32	2,3	$V/\mu s$
		$V_{in} \pm 1.25\ mV$ — LNA2		39	36	42		38	39	40	2,3	$/\mu s$
CMRR	Common-mode Rejection Ratio	$V_S \pm 1.65V$ — LNA1		112	128	161		110	128	163	2,3	dB
		$V_S \pm 1.65V$ — LNA2		112	124	156		110	123	147	2,3	dB
PSRR	Power Supply Rejection Ratio	$V_S \pm 1.65V$ — LNA1		94	106	133	VCC @1kHz	89	107	140	2,3	dB
				92	108	137	VEE @1kHz	91	109	141	2,3	dB
		$V_S \pm 1.65V$ — LNA2		94	106	133	VCC @1kHz	91	106	131	2,3	dB
				92	104	135	VEE @1kHz	89	104	130	2,3	dB

Slew Rate Measurement

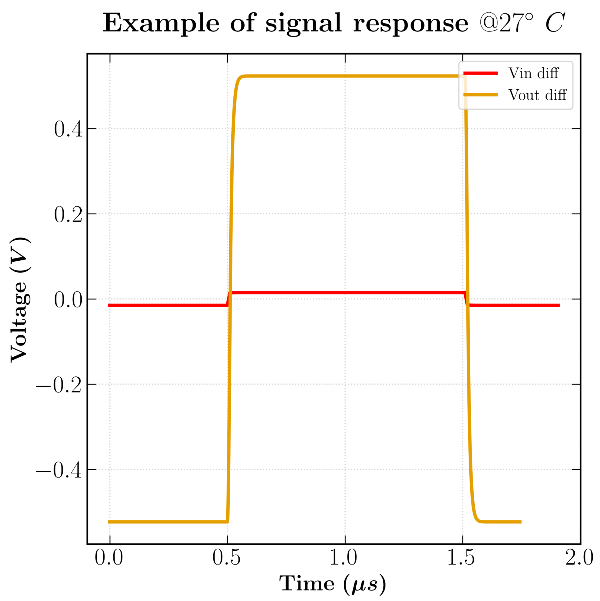


Figure 1: Output Response

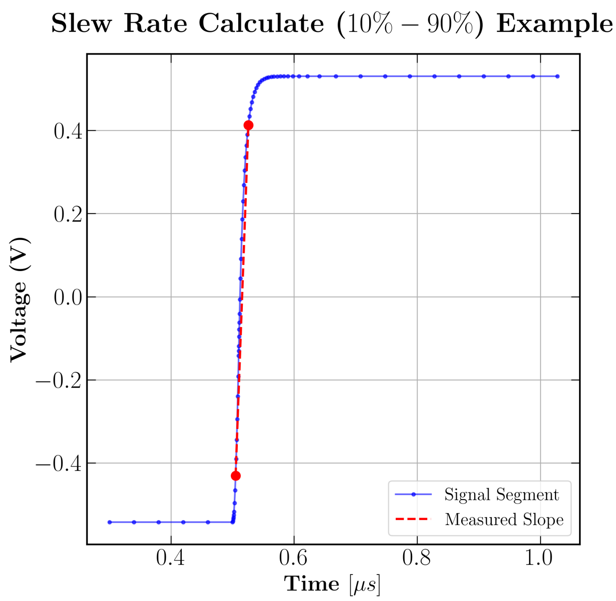


Figure 3: Slew Rate Estimation

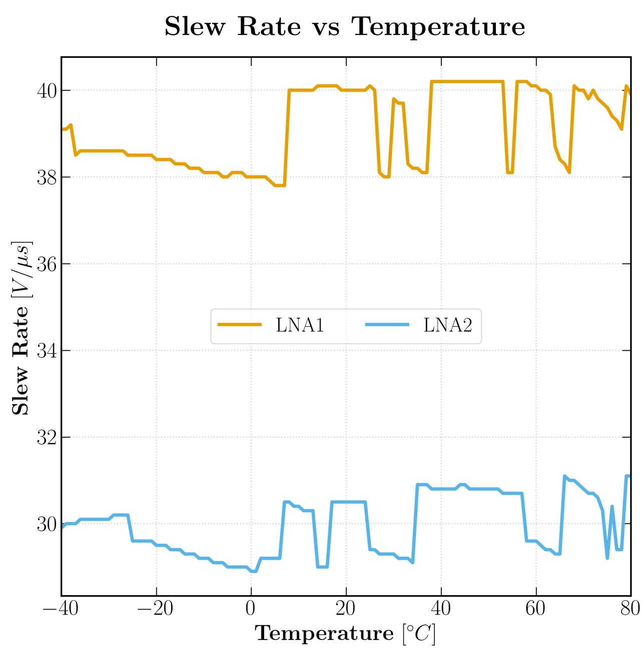


Figure 2: Slew Rate

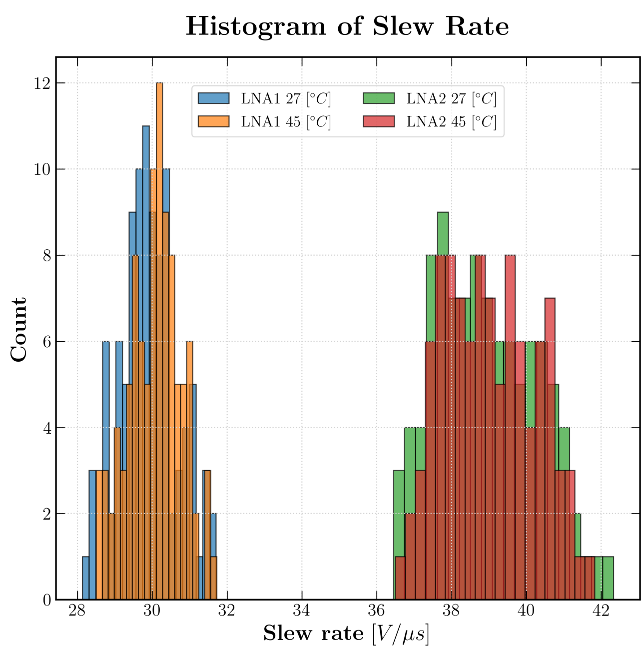


Figure 4: Slew Rate Histogram

Common-mode Rejection Ratio (CMRR)

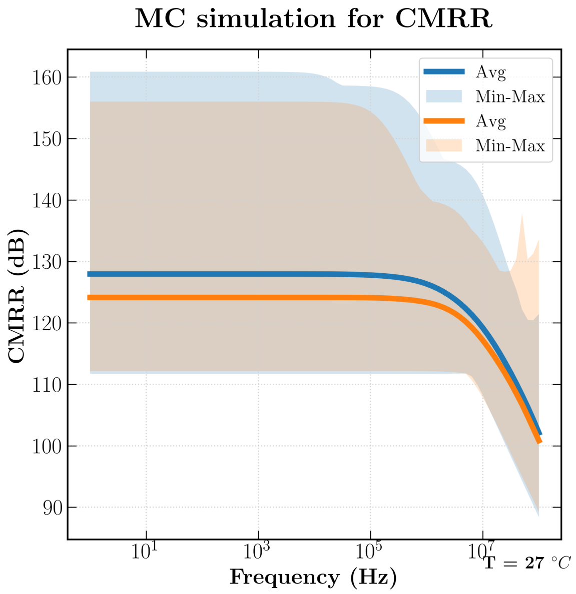


Figure 5: CMRR of LNA1/LNA2 vs Frequency (1 MHz to 100 MHz) at 27 °C

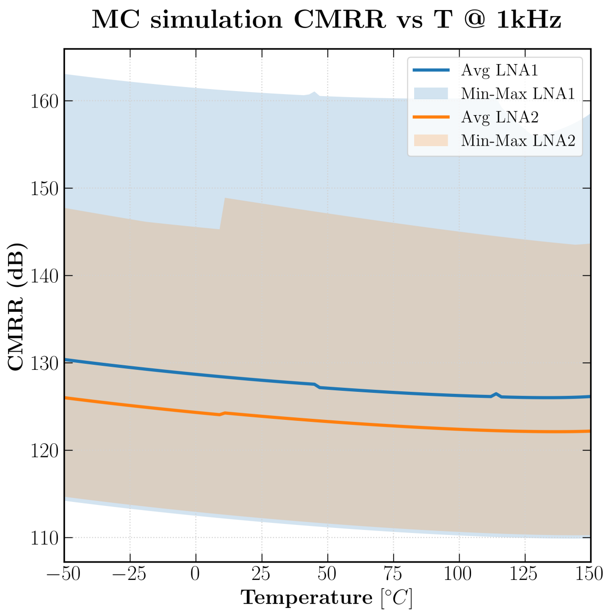


Figure 6: CMRR of LNA1/LNA2 vs Temperature (−50 °C to 150 °C) at 1 kHz

Power Suppy Rejection Ratio (PSRR)

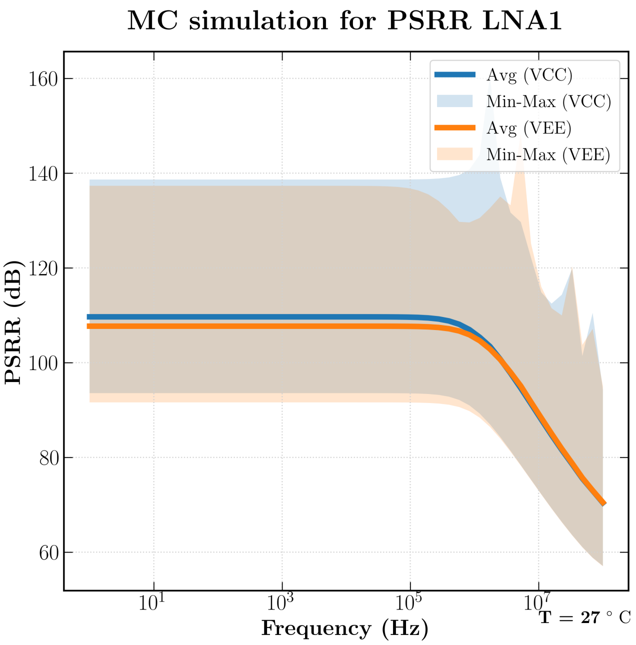


Figure 7: LNA1 PSRR (VCC, VEE) vs Frequency (1 MHz to 100 MHz) at 27 °C

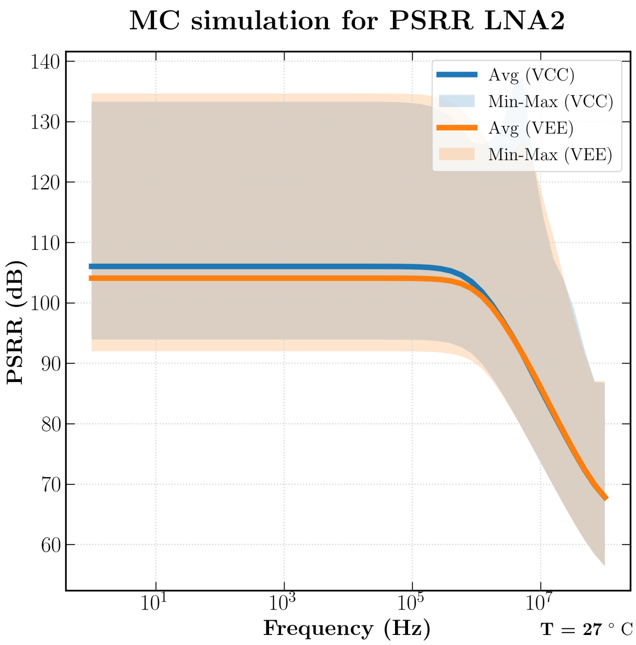


Figure 8: LNA2 PSRR (VCC, VEE) vs Frequency (1 MHz to 100 MHz) at 27 °C

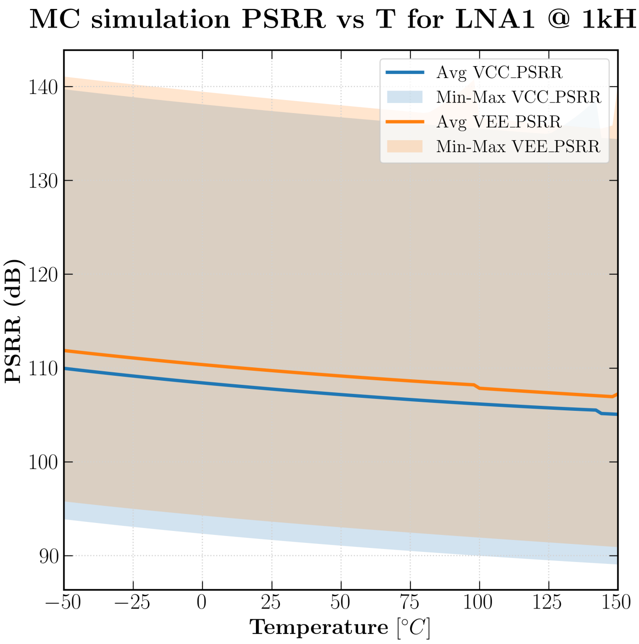


Figure 9: LNA1 PSRR (VCC, VEE) of LNA1 vs Frequency (1 MHz to 100 MHz) at 27 °C

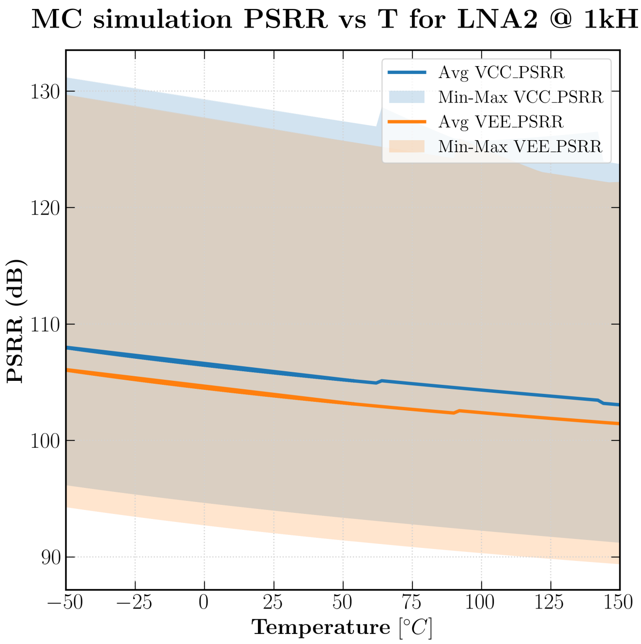


Figure 10: LNA2 PSRR (VCC, VEE) of LNA2 vs Frequency (1 MHz to 100 MHz) at 27 °C