**24Fall CMU 15-418 Asst1 Report**

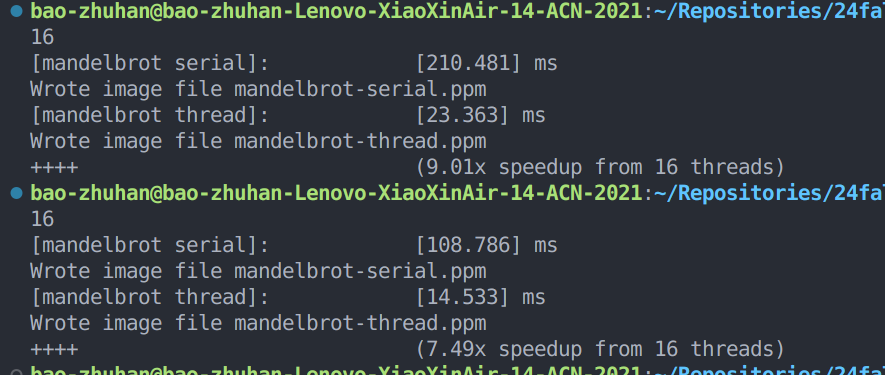
Bao Zhuhan 2024.11.07

Program1

The program ran successfully. Below is a graph of the number of threads and the time acceleration ratio. For all views, the performance gains become slower as the number of threads increases. The strange thing is that for view6, when the number of threads is 2, the time acceleration ratio will exceed 2, and even reach 2.5~3.

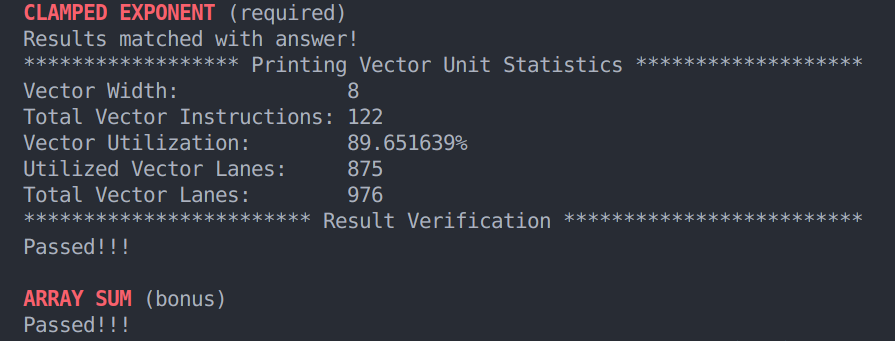
Each thread is assigned a different number of tasks, and in fact there is a clear normal distribution. Ideally, we want to get better performance with an equal number of tasks assigned to each thread.

I distribute the workload evenly by spacing the rows of images by the number of threads. Specifically, the number of rows processed by each thread is evenly distributed, avoiding a situation where some threads process more rows and others process fewer rows. The 16-thread parallel acceleration ratio of View1 reached 9.01, and the 16-thread parallel acceleration ratio of View2 reached 7.49.



Program2

My program executed successfully and matched the expected output. The vector unit statistics show high efficiency with a vector utilization rate of 89.65%. The result verification passed, confirming the correctness of my implementation. Additionally, the array sum (bonus) test also passed, demonstrating the accuracy of my array sum function. Overall, my implementation is both correct and efficient.

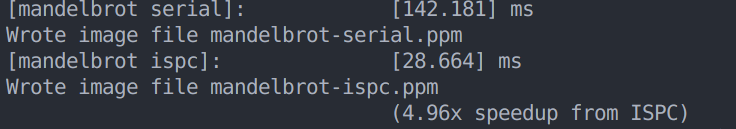


The decline in vector utilisation is due to factors such as data alignment and boundary effects, but the change is small (about 2%), indicating that my implementation has become relatively efficient. The utilisation rate is less sensitive to the width of the vector, which means that my data and computing tasks are more evenly distributed, and the vectorisation overhead is low.

As the vector width increases, the total number of vector instructions slowly increases

Program3

Baseline



**3.1 Problem 3, Part 1. A Few ISPC Basics**

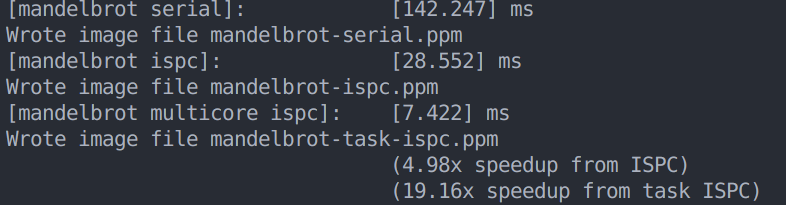
1. Ideally, an ISPC compiler using 8-wide AVX2 vector instructions can achieve up to 8x speedup, as each SIMD instruction can process 8 data elements simultaneously.In fact, only 4.96 times the acceleration was achieved.

2. The main reasons include: I. Load imbalance causes some processors in the SIMD unit to be idle, which reduces the overall efficiency. II. Discontinuous or misaligned memory access patterns can cause cache misses and memory access delays, impacting performance.

**3.2 Problem 3, Part 2: ISPC Tasks**

1. Baseline : 4.97x speedup from ISPC, 9.89x speedup from task ISPC.

2. Update: By setting the number of tasks to the same as the number of cores, a performance improvement of nearly 20 times was obtained.



Program4