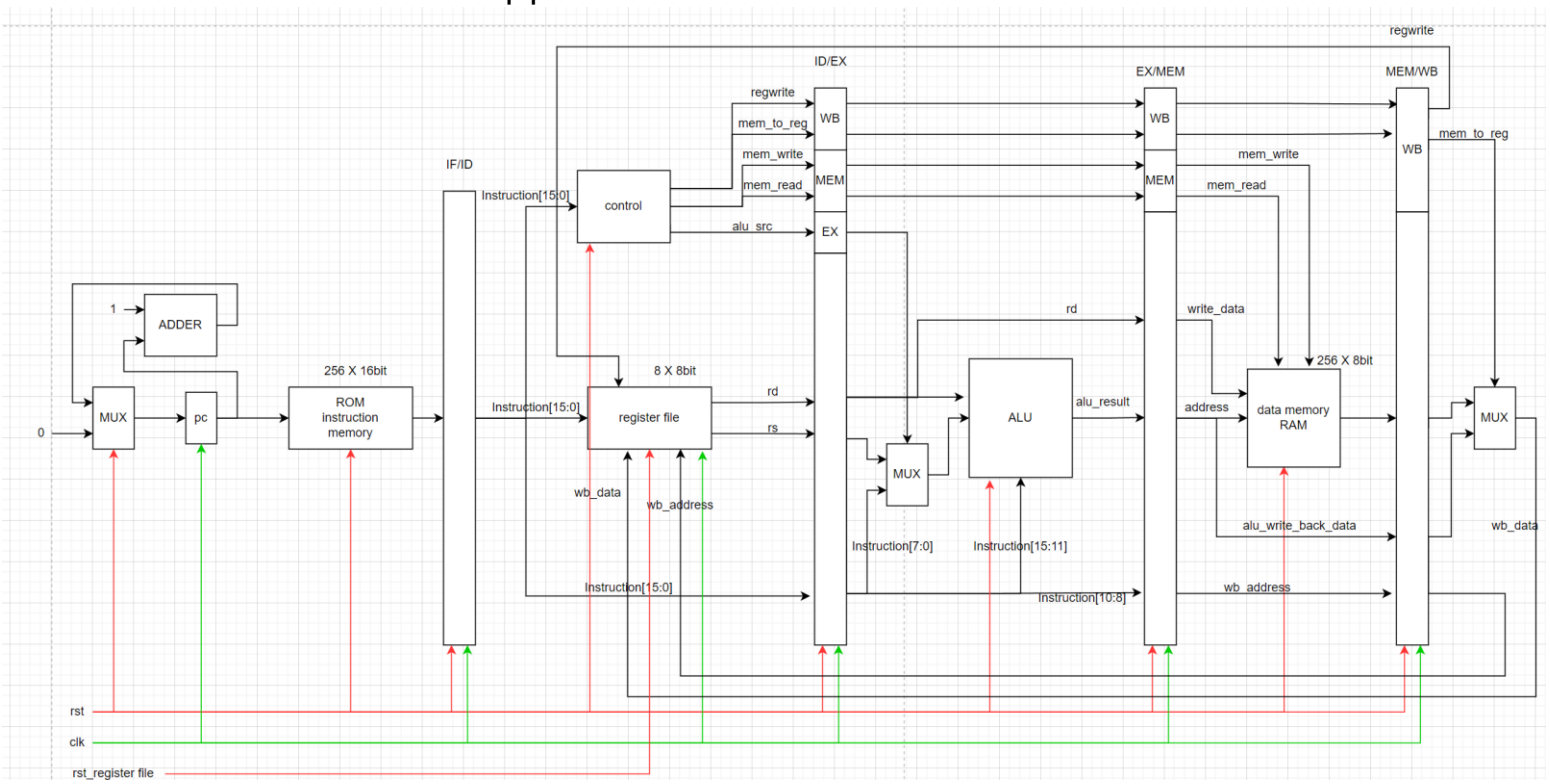
EESM5020 Final Report

Topic: 8 bits pipeline RISCV

Group: Xie Baohui, Huang Zhihong

1. Structure of 8 bits pipeline RISCV



2. Testing program, corresponding result and 16 bits instruction format [1]

```
//=========================R2 type============================
//LDI rd <- k       X[1] <- 51
//LDI rd <- k       X[2] <- 1
//ADD rd <- rd+rs       X[2] <- 51+1=52  52=0011_0100
//STD [A] <- rs         RAM[1] <- X[2]
//SUB rd <- rd-rs       X[2] <- 52-51=1  1=0000_0001
//STD [A] <- rs         RAM[2] <- X[2]
//AND rd <- rd&rs       X[2] <- 0000_0001       DEC 1
//STD [A] <- rs         RAM[3] <- X[2]
//OR rd <- rd|rs        X[2] <- 0011_0011       DEC 51
//STD [A] <- rs         RAM[4] <- X[2]
//EOR rd <- rd^rs       X[2] <- 0000_0000       DEC 0
//STD [A] <- rs         RAM[5] <- X[2]


//=========================I type=====================
//LDI rd <- k       X[3] <- 35
//LDI rd <- k       X[4] <- 6
//ADDI rd <- rd+k       X[3] <- X[3]+1 =36   BIN 0010_0100
//SUBI rd <- rd-k       X[4] <- X[4]-1 =5    BIN 0000_0101
//STD [A] <- rs         RAM[6] <- X[3]
//STD [A] <- rs         RAM[7] <- X[4]
//ANDI rd <- rd&k       X[3] <- X[3]&1=0     BIN 0000_0000
//ORI rd <- rd|k        X[4] <- X[4]|2=7     BIN 0000_0111
//STD [A] <- rs         RAM[8] <- X[3]
//STD [A] <- rs         RAM[9] <- X[4]

//=========================R1 type============================
//LDI rd <- k       X[4] <- 51
//LDI rd <- k       X[5] <- 2
//LDI rd <- k       X[6] <- 2


//NOT rd <- ~rd         X[4] <- ~X[4]=204    BIN 1100_1100
//SHL rd <- rd<<1       X[5] <- X[5]<<1=4    BIN 0000_0100
//SHR rd <- rd>>1       X[6] <- X[6]>>1=1        BIN 0000_0001


//STD [A] <- rs         RAM[10] <- X[4]
//STD [A] <- rs         RAM[11] <- X[5]
//STD [A] <- rs         RAM[12] <- X[6]

//----------------------------LDD and check result from output---------------
//LDD rd <- [A]     X[1] <- RAM[1]      52
//LDD rd <- [A]     X[2] <- RAM[2]      1
//LDD rd <- [A]     X[3] <- RAM[3]      1
//LDD rd <- [A]     X[4] <- RAM[4]      51
//LDD rd <- [A]     X[5] <- RAM[5]      0
//LDD rd <- [A]     X[6] <- RAM[6]      36
//LDD rd <- [A]     X[7] <- RAM[7]      5
//LDD rd <- [A]     X[1] <- RAM[8]      0
//LDD rd <- [A]     X[2] <- RAM[9]      7
//LDD rd <- [A]     X[3] <- RAM[10]     204
//LDD rd <- [A]     X[4] <- RAM[11]     4
//LDD rd <- [A]     X[5] <- RAM[12]     1
```

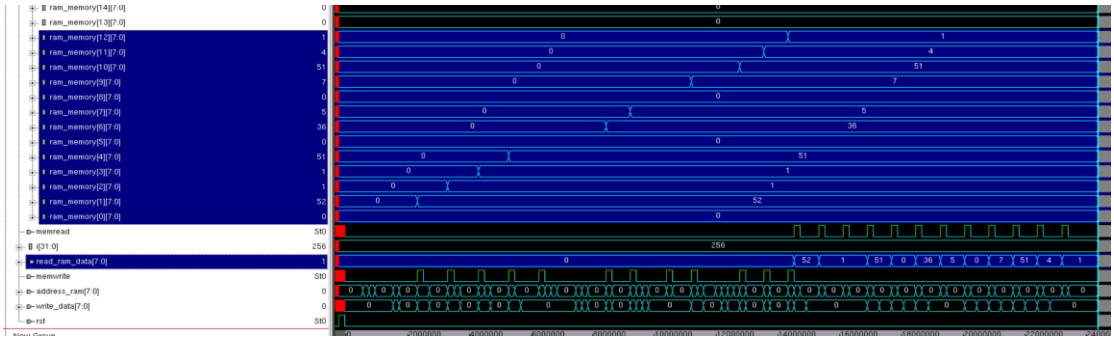
Table 1. Instruction set for the IPN-8 didactic soft processor

No.	Mnemonic	Description	Syntax	Micro-operation	16-bit Instruction Format: OPCODE / PARAMETERS (15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0)	CLK
				J - Type Instructions		
1	JMP	Direct Jump	JMP k	PC ← k	0 0 0 0 0 0 - - - k k k k k k k k	2
2	BRC	Branch if carry	BRC k	if (C = 1) then PC ← k Else if (C=0) then PC←PC+1	0 0 0 0 0 1 - - - k k k k k k k k	2
3	BRZ	Branch if zero	BRZ k	if (Z = 1) then PC ← k Else if (Z=0) then PC←PC+1	0 0 0 0 1 0 - - - k k k k k k k k	2
4	BRV	Branch if overflow	BRV k	if (V = 1) then PC ← k Else if (V=0) then PC←PC+1	0 0 0 0 1 1 - - - k k k k k k k k	2
5	JSR	Jump to Subroutine	JSR k	[SP] ← PC, SP←SP-1, PC← k	0 0 1 0 0 0 - - - k k k k k k k k	2
				I - Type Instructions		
6	ADDI	Immediate addition	ADDI Rd, k	Rd ← Rd + k	0 1 0 0 0 Rd Rd Rd k k k k k k k k	3
7	SUBI	Immediate subtraction	SUBI Rd, k	Rd ← Rd – k	0 1 0 0 1 Rd Rd Rd k k k k k k k k	3
8	ANDI	Immediate AND	ANDI Rd, k	Rd ←Rd AND k	0 1 0 1 0 Rd Rd Rd k k k k k k k k	3
9	ORI	Immediate OR	ORI Rd, k	Rd ←Rd OR k	0 1 0 1 1 Rd Rd Rd k k k k k k k k	3
10	LDI	Load immediate	LDI Rd, k	Rd ← k	0 1 1 0 0 Rd Rd Rd k k k k k k k k	2
11	LDD	Load direct from data memory	LDD Rd,[A]	Rd ← [A]	0 1 1 0 1 Rd Rd Rd A A A A A A A A	2
12	STD	Store direct to data memory	STD [A],Rs	[A] ← Rs	0 1 1 1 0 Rs Rs Rs A A A A A A A A	2
				R2 – Type Instructions		
13	ADD	Addition	ADD Rd, Rs	Rd ← Rd + Rs	1 0 0 0 0 Rd Rd Rd Rs Rs Rs - - - - - -	2
14	SUB	Subtraction	SUB Rd, Rs	Rd ← Rd - Rs	1 0 0 0 1 Rd Rd Rd Rs Rs Rs - - - - - -	2
15	AND	Logic AND	AND Rd, Rs	Rd ← Rd AND Rs	1 0 0 1 0 Rd Rd Rd Rs Rs Rs - - - - - -	2
16	OR	Logic OR	OR Rd, Rs	Rd ← Rd OR Rs	1 0 0 1 1 Rd Rd Rd Rs Rs Rs - - - - - -	2
17	LDX	Indirect load from memory	LDX Rd,[Rs]	Rd ← [Rs]	1 0 1 0 0 Rd Rd Rd Rs Rs Rs - - - - - -	2
18	STX	Indirect storage to memory	STX [Rd],Rs	[Rd] ←Rs	1 0 1 0 1 Rd Rd Rd Rs Rs Rs - - - - - -	2
				R1 – Type Instructions		
19	NOT	Logic NOT	NOT Rd	Rd←NOT Rd	1 1 1 0 0 Rd Rd Rd - - - - - - - -	2
20	SHL	Shift register left	SHL Rd	Rd(n+1)←Rd(n), Rd(0) ← 0	1 1 1 0 1 Rd Rd Rd - - - - - - - -	2
21	SHR	Shift register right	SHR Rd	Rd(n)←Rd(n+1), Rd(7) ← 0	1 1 1 1 0 Rd Rd Rd - - - - - - - -	2
22	SWAP	Swap nibbles	SWAP Rd	Rd7←Rd3, Rd6←Rd2, Rd5←Rd1, Rd4←Rd0	1 1 1 1 1 Rd Rd Rd - - - - - - - -	2
23	PUSH	Push data to stack	PUSH Rs	[SP] ← Rs, SP←SP-1	1 1 0 0 0 Rs Rs Rs - - - - - - - -	2
24	POP	Pop data from stack	POP Rd	Rd←[SP], SP←SP+1	1 1 0 0 1 Rd Rd Rd - - - - - - - -	3
				D – Type Instructions		
25	RET	Return from Routine	RET	PC←[SP]+1, SP←SP+1	0 0 1 0 1 - - - - - - - - - - - -	2

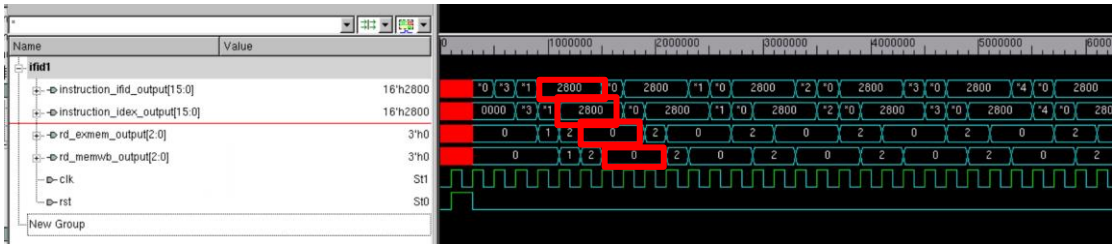
3. behavior simulation

Result

Check if the ALU result have been save in the RAM:



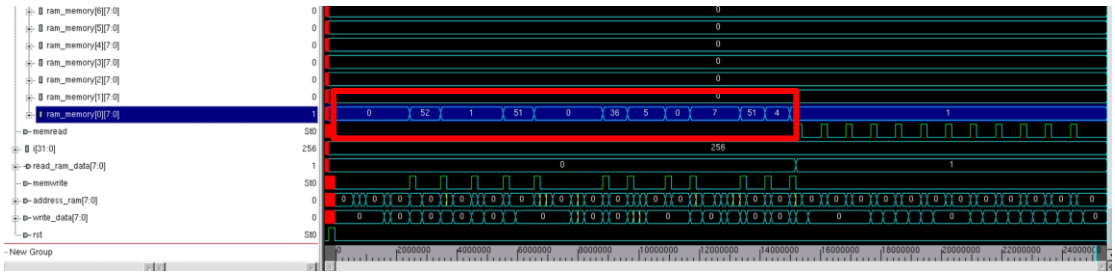
Check Pipelining:



Since only 3 bits are required in the last two stages, we reduce the number of bits passing through the last two stages. This is why the last two stages data is different.

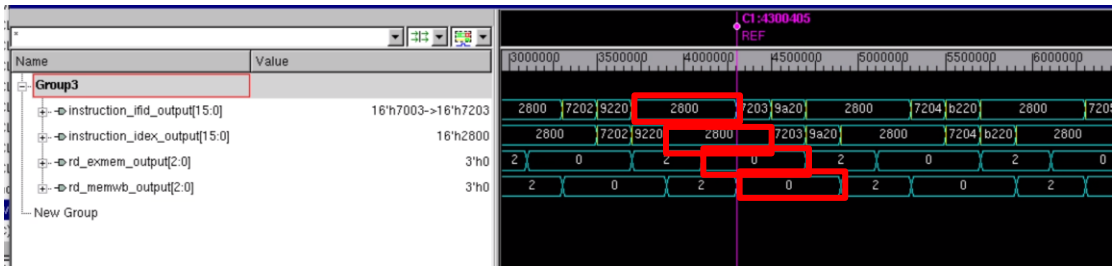
4. Synthesis

Result:



The result is same as the behavior simulation.

Check Pipeline:

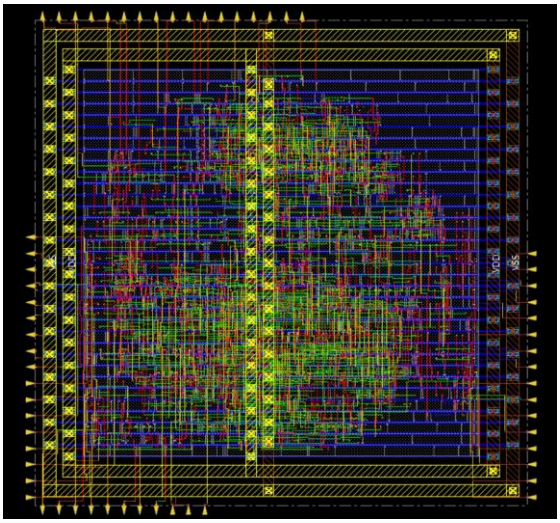


5. Layout

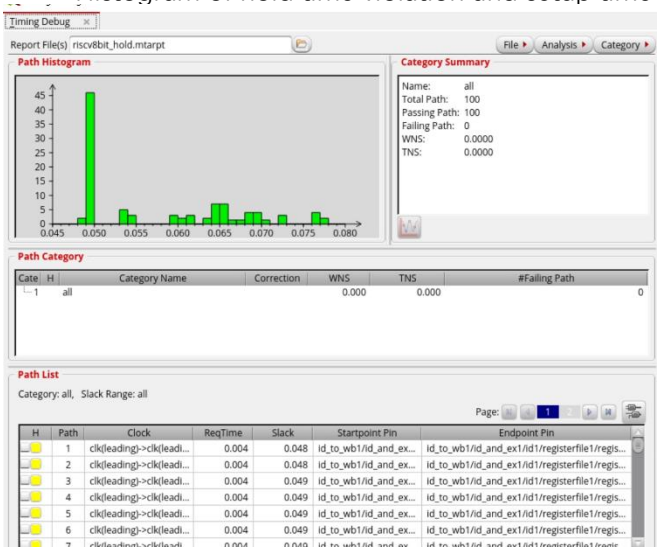
Verify connectivity and DRC

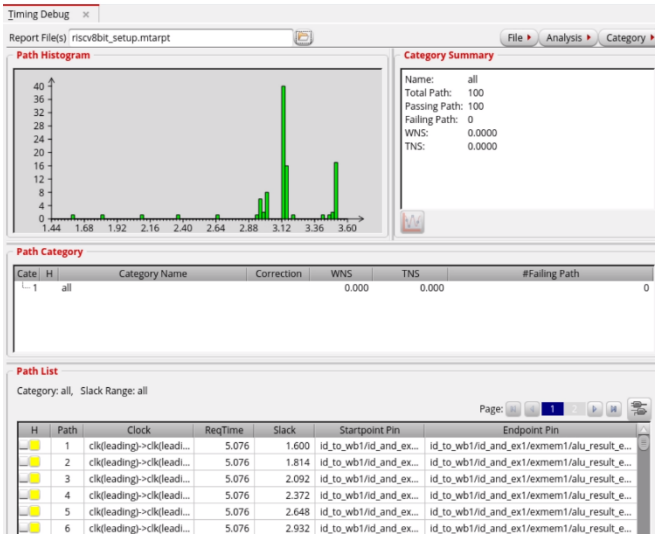
```
******** End: VERIFY CONNECTIVITY ********
  Verification Complete : 0 Viols.  0 Wrngs.
  (CPU Time: 0:00:00.1  MEM: 0.000M)

innovus 1> #-check_ndr_spacing auto                # enums={true false auto}, default=auto,  user setting
#-report riscv8bit.drc.rpt              # string, default="", user setting
 *** Starting Verify DRC (MEM: 1576.5) ***

  VERIFY DRC ..... Starting Verification
  VERIFY DRC ..... Initializing
  VERIFY DRC ..... Deleting Existing Violations
  VERIFY DRC ..... Creating Sub-Areas
  VERIFY DRC ..... Using new threading
  VERIFY DRC ..... Sub-Area: {0.000 0.000 60.800 59.640} 1 of 1
  VERIFY DRC ..... Sub-Area : 1 complete 0 Viols.

  Verification Complete : 0 Viols.

 *** End Verify DRC (CPU: 0:00:00.1  ELAPSED TIME: 1.00  MEM: 0.0M) ***
```

layout



Histogram of hold time violation and setup time violation:





6. Layout post simulation:

Result

7. Report

Synthesis area report

```
****************************************
Report : area
Design : riscv8bit
Version: P-2019.03-SP5
Date   : Sun May 29 21:54:33 2022
****************************************

Library(s) Used:

    NangateOpenCellLibrary (File: /afs/ee.ust.hk/staff/ee/dept/public/e

Number of ports:                          596
Number of nets:                          1321
Number of cells:                          705
Number of combinational cells:            517
Number of sequential cells:               169
Number of macros/black boxes:               0
Number of buf/inv:                        104
Number of references:                       2

Combinational area:               621.110006
Buf/Inv area:                      57.988000
Noncombinational area:            764.217972
Macro/Black Box area:               0.000000
Net Interconnect area:      undefined  (Wire load has zero net area)

Total cell area:                 1385.327978
Total area:                 undefined
1
```

Synthesis power report

```
Design        Wire Load Model            Library
------------------------------------------------
riscv8bit              5K_hvratio_1_1    NangateOpenCellLibrary

Global Operating Voltage = 0.95
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 1.000000ff
    Time Units = 1ns
    Dynamic Power Units = 1uW    (derived from V,C,T units)
    Leakage Power Units = 1nW


  Cell Internal Power  = 169.2236 uW   (92%)
  Net Switching Power  =  14.1995 uW    (8%)
                         ---------
Total Dynamic Power    = 183.4232 uW  (100%)

Cell Leakage Power     =  17.2393 uW


                 Internal         Switching           Leakage            Total
Power Group      Power            Power               Power              Power   (   %    )  Attrs
-----------------------------------------------------------------------------------------------
io_pad             0.0000           0.0000              0.0000             0.0000  (   0.00%)
memory             0.0000           0.0000              0.0000             0.0000  (   0.00%)
black_box          0.0000           0.0000              0.0000             0.0000  (   0.00%)
clock_network      0.0000           0.0000              0.0000             0.0000  (   0.00%)
register         162.2012           3.0951          8.9738e+03           174.2700  (  86.85%)
sequential         0.0000           0.0000              0.0000             0.0000  (   0.00%)
combinational      7.0224          11.1045          8.2655e+03            26.3924  (  13.15%)
-----------------------------------------------------------------------------------------------
Total            169.2236 uW       14.1995 uW       1.7239e+04 nW        200.6624 uW
1
```

Synthesis timing report

```
  Startpoint: ram_data[0]
              (input port clocked by clk)
  Endpoint: data_from_ram[0]
            (output port clocked by clk)

clock clk (rise edge)                                   5.00       5.00
clock network delay (ideal)                             0.00       5.00
output external delay                                  -1.00       4.00
data required time                                                 4.00
-----------------------------------------------------------------------------
data required time                                                 4.00
data arrival time                                                 -1.15
-----------------------------------------------------------------------------
slack (MET)                                                        2.85


 Startpoint: rst_registerfile
             (input port clocked by clk)
 Endpoint: id_to_wb1/id_and_ex1/id1/registerfile1/register_memory_reg_7__0_
           (rising edge-triggered flip-flop clocked by clk)

clock clk (rise edge)                                   5.00       5.00
clock network delay (ideal)                             0.00       5.00
id_to_wb1/id_and_ex1/id1/registerfile1/register_memory_reg_7__0_/CK (DFF_X1)     0.00     5.00 r
library setup time                                     -0.19       4.81
data required time                                                 4.81
-----------------------------------------------------------------------------
data required time                                                 4.81
data arrival time                                                 -2.24
-----------------------------------------------------------------------------
slack (MET)                                                        2.58
```

```
  Startpoint: pc1/pc_increment_address_reg_0_
              (rising edge-triggered flip-flop clocked by clk)
  Endpoint: pc_increment_address[0]
            (output port clocked by clk)
```

```
clock clk (rise edge)                                          5.00       5.00
clock network delay (ideal)                                    0.00       5.00
output external delay                                         -1.00       4.00
data required time                                                        4.00
-------------------------------------------------------------------------------
data required time                                                        4.00
data arrival time                                                        -0.35
-------------------------------------------------------------------------------
slack (MET)                                                               3.65
```

```
  Startpoint: id_to_wb1/id_and_ex1/id1/idex1/alu_src_idex_output_reg
              (rising edge-triggered flip-flop clocked by clk)
  Endpoint: id_to_wb1/id_and_ex1/exmem1/alu_result_exmem_output_reg_7_
            (rising edge-triggered flip-flop clocked by clk)
```

```
clock clk (rise edge)                                          5.00       5.00
clock network delay (ideal)                                    0.00       5.00
id_to_wb1/id_and_ex1/exmem1/alu_result_exmem_output_reg_7_/CK (DFF_X1)     0.00     5.00 r
library setup time                                            -0.16       4.84
data required time                                                        4.84
-------------------------------------------------------------------------------
data required time                                                        4.84
data arrival time                                                        -3.66
-------------------------------------------------------------------------------
slack (MET)                                                               1.18
```

Layout area report

```
  Hinst Name                          Module Name         Inst Count         Total Area
--------------------------------------------------------------------------------------
riscv8bit                                                        673           1379.742
 id_to_wb1                            id_to_wb                   647           1315.104
  id_to_wb1/id_and_ex1                id_and_ex                  595           1185.296
   id_to_wb1/id_and_ex1/alu1          alu                        117            176.890
    id_to_wb1/id_and_ex1/alu1/r367    alu_DW01_add_0               9             32.452
    id_to_wb1/id_and_ex1/alu1/r368    alu_DW01_sub_0               9             32.186
   id_to_wb1/id_and_ex1/exmem1        exmem                       47            129.010
   id_to_wb1/id_and_ex1/id1           id                         430            878.066
    id_to_wb1/id_and_ex1/id1/control1 control                     13             11.970
    id_to_wb1/id_and_ex1/id1/idex1    idex                        75            207.214
    id_to_wb1/id_and_ex1/id1/ifid1    ifid                        33             89.908
    id_to_wb1/id_and_ex1/id1/registerfile1 registerfile           307            566.314
  id_to_wb1/memwb1                    memwb                       51            128.478
pc1                                   pc                          25             63.308
 pc1/add_20                           pc_DW01_inc_0                8             18.088
```

Layout power report

```
Total Power
-----------------------------------------------------------------------------------
Total Internal Power:        0.18871216      62.6092%
Total Switching Power:       0.09486360      31.4730%
Total Leakage Power:         0.01783714       5.9178%
Total Power:                 0.30141290
-----------------------------------------------------------------------------------


Group                          Internal   Switching     Leakage       Total  Percentage
                               Power      Power         Power         Power  (%)
-----------------------------------------------------------------------------------
Sequential                       0.1371     0.01659     0.00914     0.1628       54.03
Macro                                 0          0           0          0           0
IO                                    0          0           0          0           0
Combinational                    0.04358    0.04261    0.008582    0.09477       31.44
Clock (Combinational)            0.00802    0.03566   0.0001149      0.0438       14.53
Clock (Sequential)                    0          0           0          0           0
-----------------------------------------------------------------------------------
Total                            0.1887     0.09486     0.01784      0.3014         100
-----------------------------------------------------------------------------------


Rail                 Voltage   Internal   Switching     Leakage       Total  Percentage
                               Power      Power         Power         Power  (%)
-----------------------------------------------------------------------------------
VDD                     0.95     0.1887     0.09486     0.01784      0.3014         100


Clock                          Internal   Switching     Leakage       Total  Percentage
                               Power      Power         Power         Power  (%)
-----------------------------------------------------------------------------------
clk                              0.00802    0.03566   0.0001149      0.0438       14.53
-----------------------------------------------------------------------------------
Total (excluding duplicates)     0.00802    0.03566   0.0001149      0.0438       14.53
-----------------------------------------------------------------------------------
```

Layout setup time violation timing report

```
-------------------------------------------------------------
     optDesign Final SI Timing Summary
-------------------------------------------------------------

+-----------------+--------+--------+---------+
|    Setup mode   |   all  | reg2reg | default |
+-----------------+--------+--------+---------+
|          WNS (ns):| 1.599  |  1.599  |  2.969  |
|          TNS (ns):| 0.000  |  0.000  |  0.000  |
|    Violating Paths:|   0    |    0    |    0    |
|         All Paths:|  203   |   145   |   203   |
+-----------------+--------+--------+---------+

+---------------+-------------------------------+-------------------+
|               |             Real              |       Total       |
|    DRVs       +---------------+---------------+-------------------|
|               | Nr nets(terms) | Worst Vio  | Nr nets(terms)  |
+---------------+---------------+---------------+-------------------+
|   max_cap     |      0 (0)    |     0.000     |      0 (0)      |
|   max_tran    |      0 (0)    |     0.000     |      0 (0)      |
|   max_fanout  |      0 (0)    |       0       |      0 (0)      |
|   max_length  |      0 (0)    |       0       |      0 (0)      |
+---------------+---------------+---------------+-------------------+

Density: 59.593%
Total number of glitch violations: 0
-------------------------------------------------------------
```

Layout hold time violation timing report

```
-------------------------------------------------------------
     optDesign Final SI Timing Summary
-------------------------------------------------------------

+-----------------+--------+--------+---------+
|    Hold mode    |   all  | reg2reg | default |
+-----------------+--------+--------+---------+
|          WNS (ns):| 0.048  |  0.048  |  0.977  |
|          TNS (ns):| 0.000  |  0.000  |  0.000  |
|    Violating Paths:|   0    |    0    |    0    |
|         All Paths:|  203   |   145   |   203   |
+-----------------+--------+--------+---------+

+---------------+-------------------------------+-------------------+
|               |             Real              |       Total       |
|    DRVs       +---------------+---------------+-------------------|
|               | Nr nets(terms) | Worst Vio  | Nr nets(terms)  |
+---------------+---------------+---------------+-------------------+
|   max_cap     |      0 (0)    |     0.000     |      0 (0)      |
|   max_tran    |      0 (0)    |     0.000     |      0 (0)      |
|   max_fanout  |      0 (0)    |       0       |      0 (0)      |
|   max_length  |      0 (0)    |       0       |      0 (0)      |
+---------------+---------------+---------------+-------------------+

Density: 59.593%
Total number of glitch violations: 0
-------------------------------------------------------------
```

Reference: [1] Hernandez Zavala, A., Camacho Nieto, O., Huerta Ruelas, J.A., Carvallo Dominguez, A.R., 2015. Design of a General Purpose 8-bit RISC Processor for Computer Architecture Learning. Computación y Sistemas 19. doi:10.13053/cys-19-2-1941