EESM 5020 Digital VLSI System Design and Design Automation (Spring, 2022)

Design Assignment 2: Design a Programmable FIR Filter

Due Date: 2 May, 2022

Baohui Xie

Objective

This assignment will guide you to be more familiar with writing Verilog code. In this assignment, you are going to use the most basic arithmetic units in a typical ALU (i.e. adder and multiplier) to implement a simple programmable 6-tap FIR filter based on the given structure.

Hand In

The full design flow, including synthesis and P&R, is required to be done. Please submit all the materials listed at the end of this assignment.

Synopsys Setup and Template Project

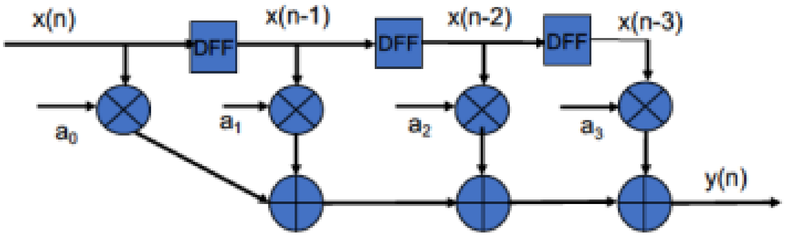
You can use the same template project as that in the last assignment. You need to write your own Verilog code and modify the sample scripts in the template project to cater for your design.

Assignment: A simple Programmable 6-tap FIR Filter Design using pipelined structure

A 4-tap low pass FIR filter can be represented as follows:

$$y(n) = a_0 * x(n) + a_1 * x(n-1) + a_2 * x(n-2) + a_3 * x(n-3)$$

where both the coefficient a_i and the input *x(i)* are 16-bit 2s complement number. The direct implementation of this filter is shown in the following figure:



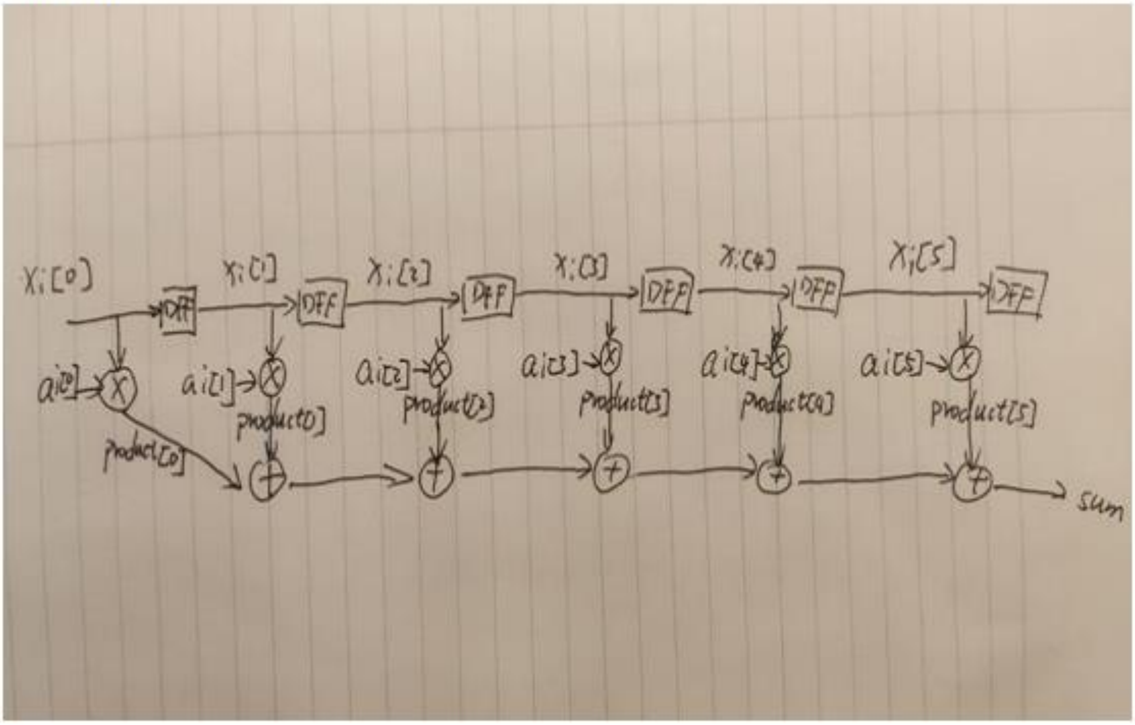
where DFF represents the delay element. It can be a D flip flop controlled by the clock signal. In this section, you need to implement a programmable 6-tap FIR filter based on the pipeline structure. The user can control the number of taps, which is ranging from 2 to 6, by sending a 3-bit control word. In this filter design, you need to decide the bit width of the intermediate data and the output such that there is no overflow in the computation. The adder and multiplier can be implemented using simple + and * syntax, i.e. using Synopsys DesignWare IP.

Things to be submitted:

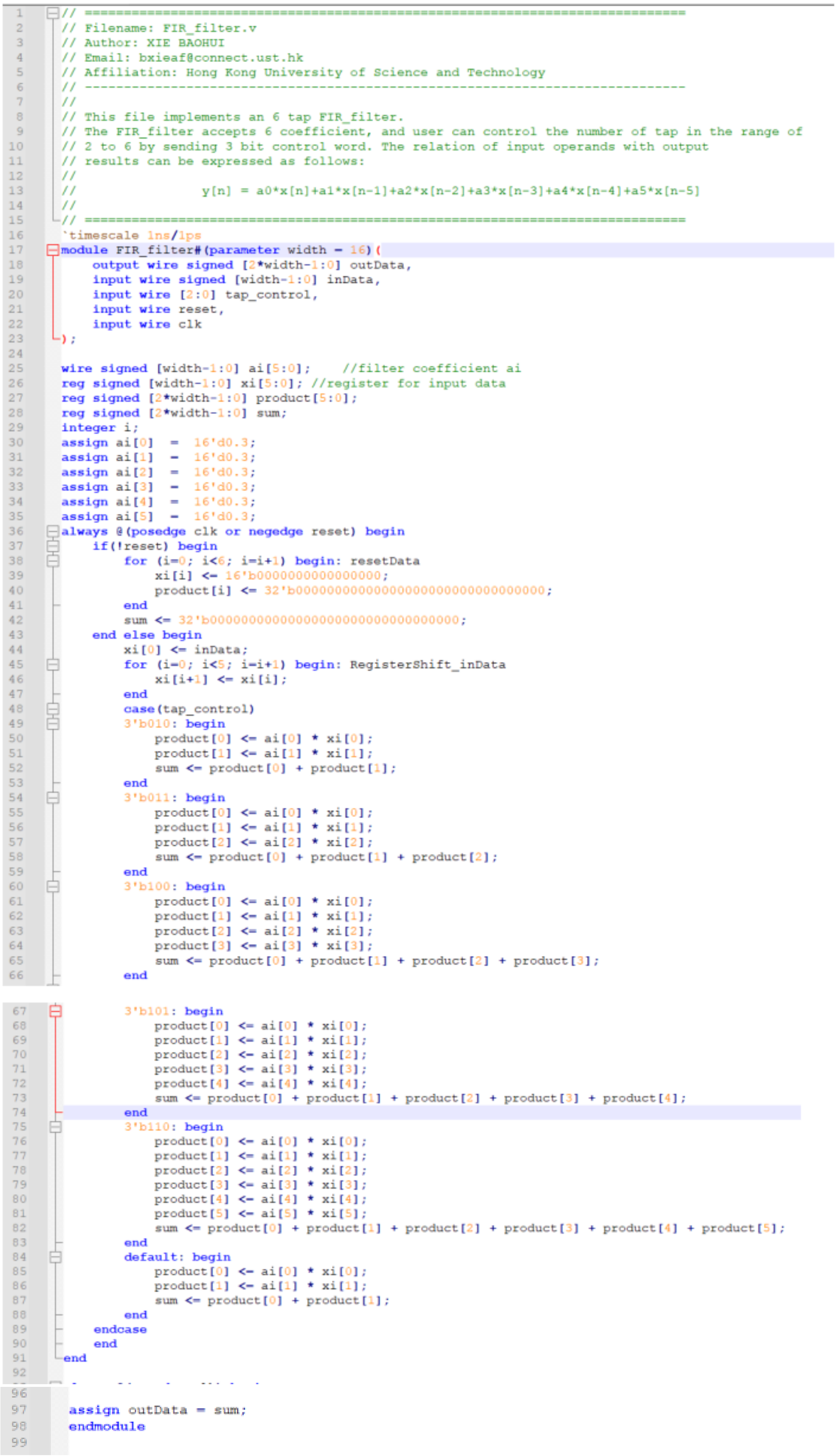
1. Plot the structure of your design, and hand in the verilog source code (.v)
2. Behavior simulation of the FIR filter.
3. Synthesized area, critical path, and power consumption reports.
4. Screenshot of the post-synthesized simulation.
5. Screenshot of the layout. The area, timing, and power reports of the layout.
6. Screenshot of the post-layout simulation.

1. Plot the structure of your design, and hand in the verilog source code (.v)

Structure:

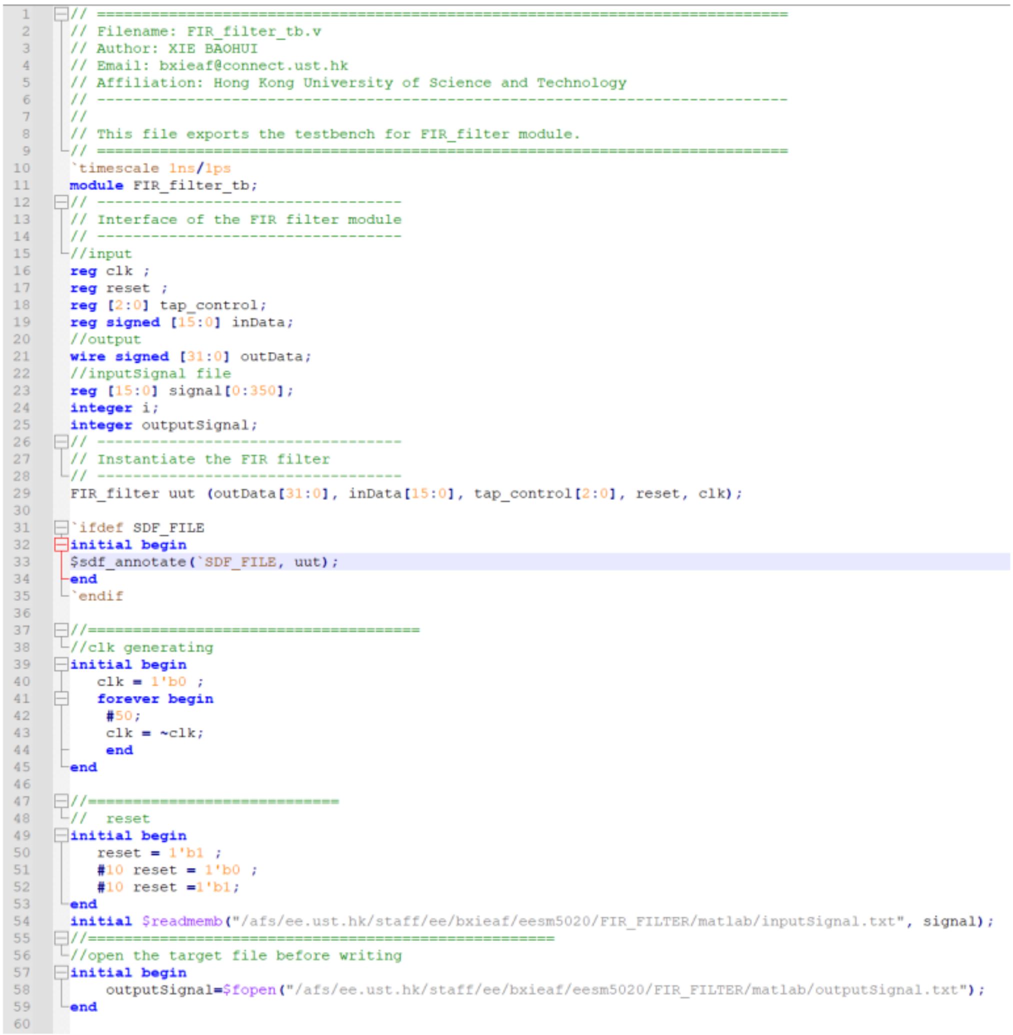


Verilog source code:

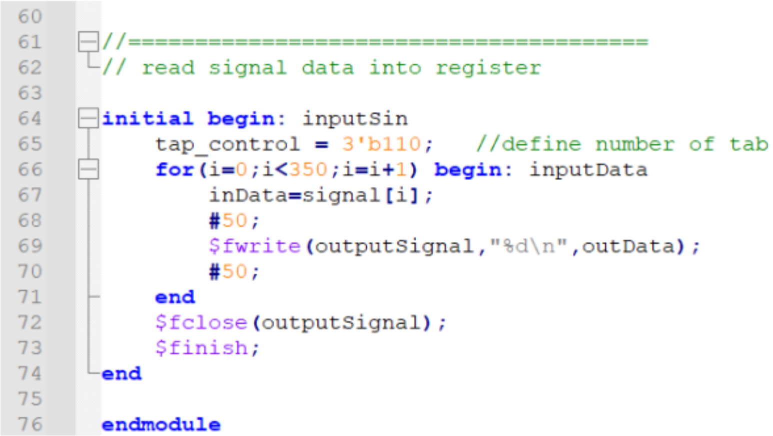


```verilog
// ============================================================================
// Filename: FIR_filter.v
// Author: XIE BAOHUI
// Email: bxieaf@connect.ust.hk
// Affiliation: Hong Kong University of Science and Technology
// ----------------------------------------------------------------------------
//
// This file implements an 6 tap FIR_filter.
// The FIR_filter accepts 6 coefficient, and user can control the number of tap in the range of
// 2 to 6 by sending 3 bit control word. The relation of input operands with output
// results can be expressed as follows:
//
//                  y[n] = a0*x[n]+a1*x[n-1]+a2*x[n-2]+a3*x[n-3]+a4*x[n-4]+a5*x[n-5]
//
// ============================================================================
`timescale 1ns/1ps
module FIR_filter#(parameter width = 16)(
    output wire signed [2*width-1:0] outData,
    input wire signed [width-1:0] inData,
    input wire [2:0] tap_control,
    input wire reset,
    input wire clk
);

wire signed [width-1:0] ai[5:0];    //filter coefficient ai
reg signed [width-1:0] xi[5:0]; //register for input data
reg signed [2*width-1:0] product[5:0];
reg signed [2*width-1:0] sum;
integer i;
assign ai[0]  =  16'd0.3;
assign ai[1]  =  16'd0.3;
assign ai[2]  =  16'd0.3;
assign ai[3]  =  16'd0.3;
assign ai[4]  =  16'd0.3;
assign ai[5]  =  16'd0.3;
always @(posedge clk or negedge reset) begin
    if(!reset) begin
        for (i=0; i<6; i=i+1) begin: resetData
            xi[i] <= 16'b0000000000000000;
            product[i] <= 32'b00000000000000000000000000000000;
        end
        sum <= 32'b00000000000000000000000000000000;
    end else begin
        xi[0] <= inData;
        for (i=0; i<5; i=i+1) begin: RegisterShift_inData
            xi[i+1] <= xi[i];
        end
        case(tap_control)
        3'b010: begin
            product[0] <= ai[0] * xi[0];
            product[1] <= ai[1] * xi[1];
            sum <= product[0] + product[1];
        end
        3'b011: begin
            product[0] <= ai[0] * xi[0];
            product[1] <= ai[1] * xi[1];
            product[2] <= ai[2] * xi[2];
            sum <= product[0] + product[1] + product[2];
        end
        3'b100: begin
            product[0] <= ai[0] * xi[0];
            product[1] <= ai[1] * xi[1];
            product[2] <= ai[2] * xi[2];
            product[3] <= ai[3] * xi[3];
            sum <= product[0] + product[1] + product[2] + product[3];
        end
        3'b101: begin
            product[0] <= ai[0] * xi[0];
            product[1] <= ai[1] * xi[1];
            product[2] <= ai[2] * xi[2];
            product[3] <= ai[3] * xi[3];
            product[4] <= ai[4] * xi[4];
            sum <= product[0] + product[1] + product[2] + product[3] + product[4];
        end
        3'b110: begin
            product[0] <= ai[0] * xi[0];
            product[1] <= ai[1] * xi[1];
            product[2] <= ai[2] * xi[2];
            product[3] <= ai[3] * xi[3];
            product[4] <= ai[4] * xi[4];
            product[5] <= ai[5] * xi[5];
            sum <= product[0] + product[1] + product[2] + product[3] + product[4] + product[5];
        end
        default: begin
            product[0] <= ai[0] * xi[0];
            product[1] <= ai[1] * xi[1];
            sum <= product[0] + product[1];
        end
    endcase
    end
end


assign outData = sum;
endmodule

```

Verilog testbench:

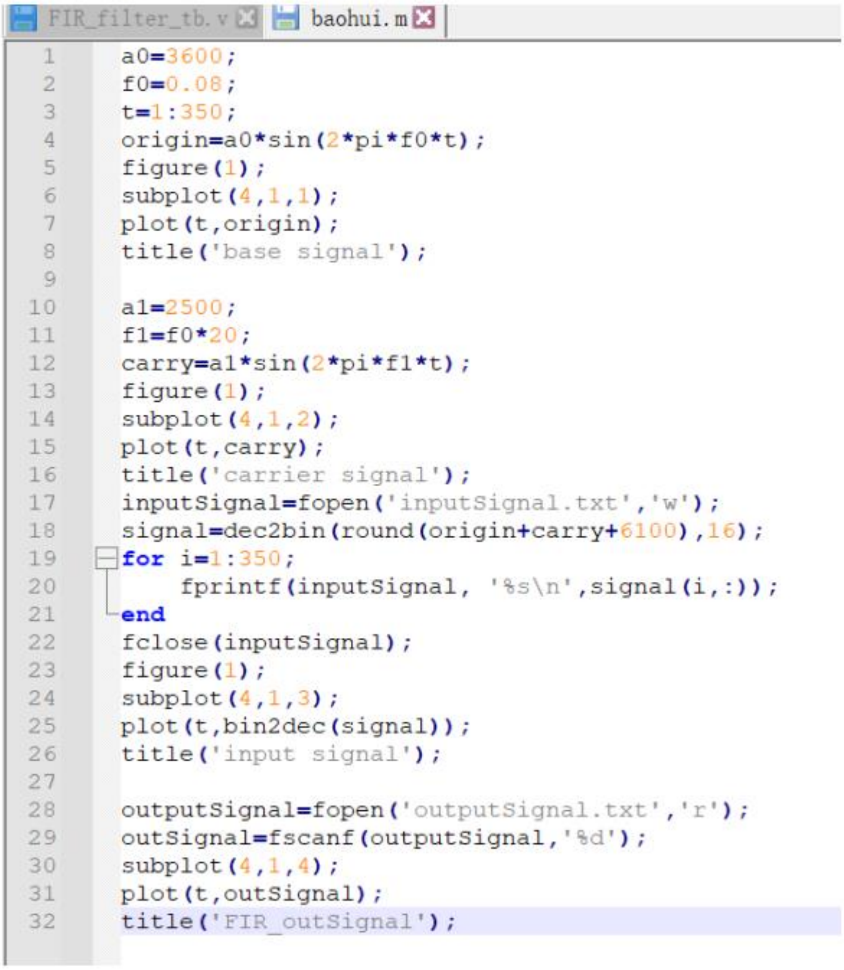


```verilog
// ==============================================================================
// Filename: FIR_filter_tb.v
// Author: XIE BAOHUI
// Email: bxieaf@connect.ust.hk
// Affiliation: Hong Kong University of Science and Technology
// ------------------------------------------------------------------------------
//
// This file exports the testbench for FIR_filter module.
// ==============================================================================
`timescale 1ns/1ps
module FIR_filter_tb;
// ---------------------------------
// Interface of the FIR filter module
// ---------------------------------
//input
reg clk ;
reg reset ;
reg [2:0] tap_control;
reg signed [15:0] inData;
//output
wire signed [31:0] outData;
//inputSignal file
reg [15:0] signal[0:350];
integer i;
integer outputSignal;
// ---------------------------------
// Instantiate the FIR filter
// ---------------------------------
FIR_filter uut (outData[31:0], inData[15:0], tap_control[2:0], reset, clk);

`ifdef SDF_FILE
initial begin
$sdf_annotate(`SDF_FILE, uut);
end
`endif

//====================================
//clk generating
initial begin
   clk = 1'b0 ;
   forever begin
    #50;
    clk = ~clk;
    end
end

//===========================
//  reset
initial begin
   reset = 1'b1 ;
   #10 reset = 1'b0 ;
   #10 reset =1'b1;
end
initial $readmemb("/afs/ee.ust.hk/staff/ee/bxieaf/eesm5020/FIR_FILTER/matlab/inputSignal.txt", signal);
//=================================================
//open the target file before writing
initial begin
    outputSignal=$fopen("/afs/ee.ust.hk/staff/ee/bxieaf/eesm5020/FIR_FILTER/matlab/outputSignal.txt");
end

```



```verilog

//========================================
// read signal data into register

initial begin: inputSin
    tap_control = 3'b110;   //define number of tab
    for(i=0;i<350;i=i+1) begin: inputData
        inData=signal[i];
        #50;
        $fwrite(outputSignal,"%d\n",outData);
        #50;
    end
    $fclose(outputSignal);
    $finish;
end

endmodule
```

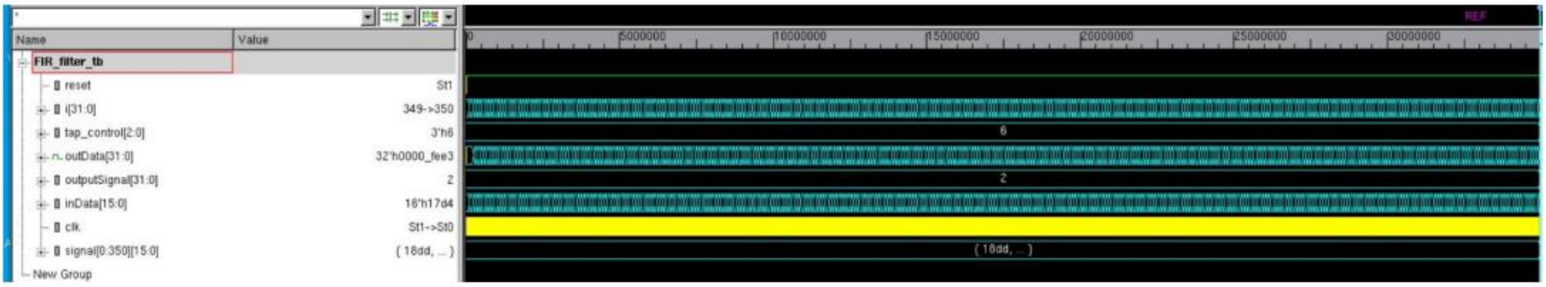
MATLAB code for generating signal with noise



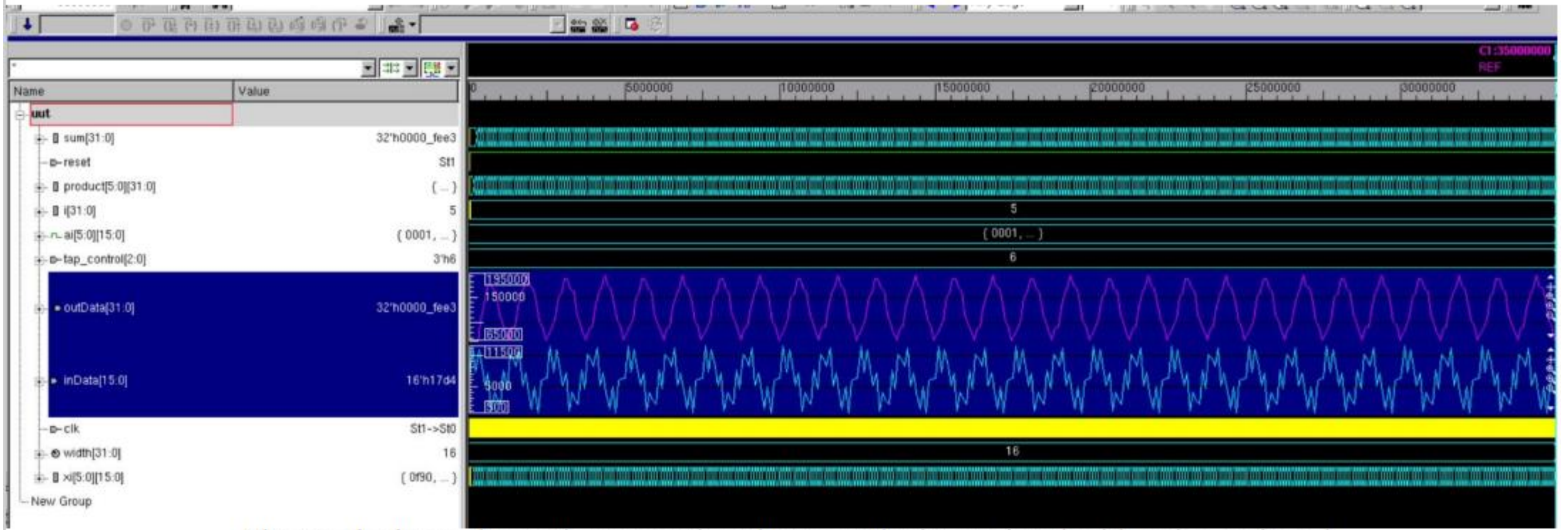
```
a0=3600;
f0=0.08;
t=1:350;
origin=a0*sin(2*pi*f0*t);
figure(1);
subplot(4,1,1);
plot(t,origin);
title('base signal');

a1=2500;
f1=f0*20;
carry=a1*sin(2*pi*f1*t);
figure(1);
subplot(4,1,2);
plot(t,carry);
title('carrier signal');
inputSignal=fopen('inputSignal.txt','w');
signal=dec2bin(round(origin+carry+6100),16);
for i=1:350;
    fprintf(inputSignal, '%s\n',signal(i,:));
end
fclose(inputSignal);
figure(1);
subplot(4,1,3);
plot(t,bin2dec(signal));
title('input signal');

outputSignal=fopen('outputSignal.txt','r');
outSignal=fscanf(outputSignal,'%d');
subplot(4,1,4);
plot(t,outSignal);
title('FIR_outSignal');
```

Comment:
In this design, MATLAB is used as a signal generator. As shown in the above MATLAB source code, the main signal is a sin function waveform with a very low frequency about 0.08 and the magnitude is around 3600, while the carry noise is about 20 times higher frequency than the main signal, and the magnitude is 2500. After the filtering, the output signal with be packaged to the file “outputSignal.txt” and read by the MATLAB. For the control signal of number of tap, I did not write the process to change the tap control signal. If the user want to test the filter under the other tap condition, they should change the tap setup under the testbench file directly.

2. Behavior simulation of the FIR filter.

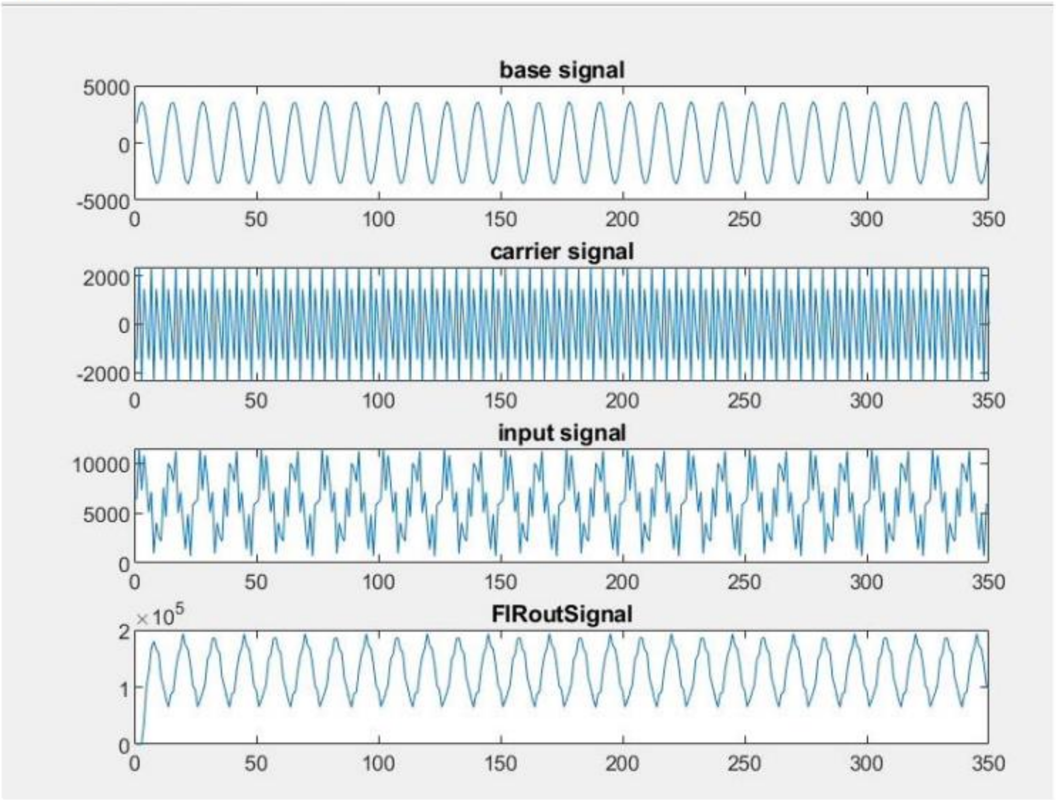


Name	Value
FIR_filter_tb	
reset	St1
i[31:0]	349->350
tap_control[2:0]	3'h6
outData[31:0]	32'h0000_fee3
outputSignal[31:0]	2
inData[15:0]	16'h17d4
clk	St1->St0
signal[0:350][15:0]	(18dd, ...)
New Group	



Name	Value
uut	
sum[31:0]	32'h0000_fee3
reset	St1
product[5:0][31:0]	(...)
i[31:0]	5
ai[5:0][15:0]	(0001, ...)
tap_control[2:0]	3'h6
outData[31:0]	32'h0000_fee3
inData[15:0]	16'h17d4
clk	St1->St0
width[31:0]	16
xi[5:0][15:0]	(0f90, ...)
New Group	

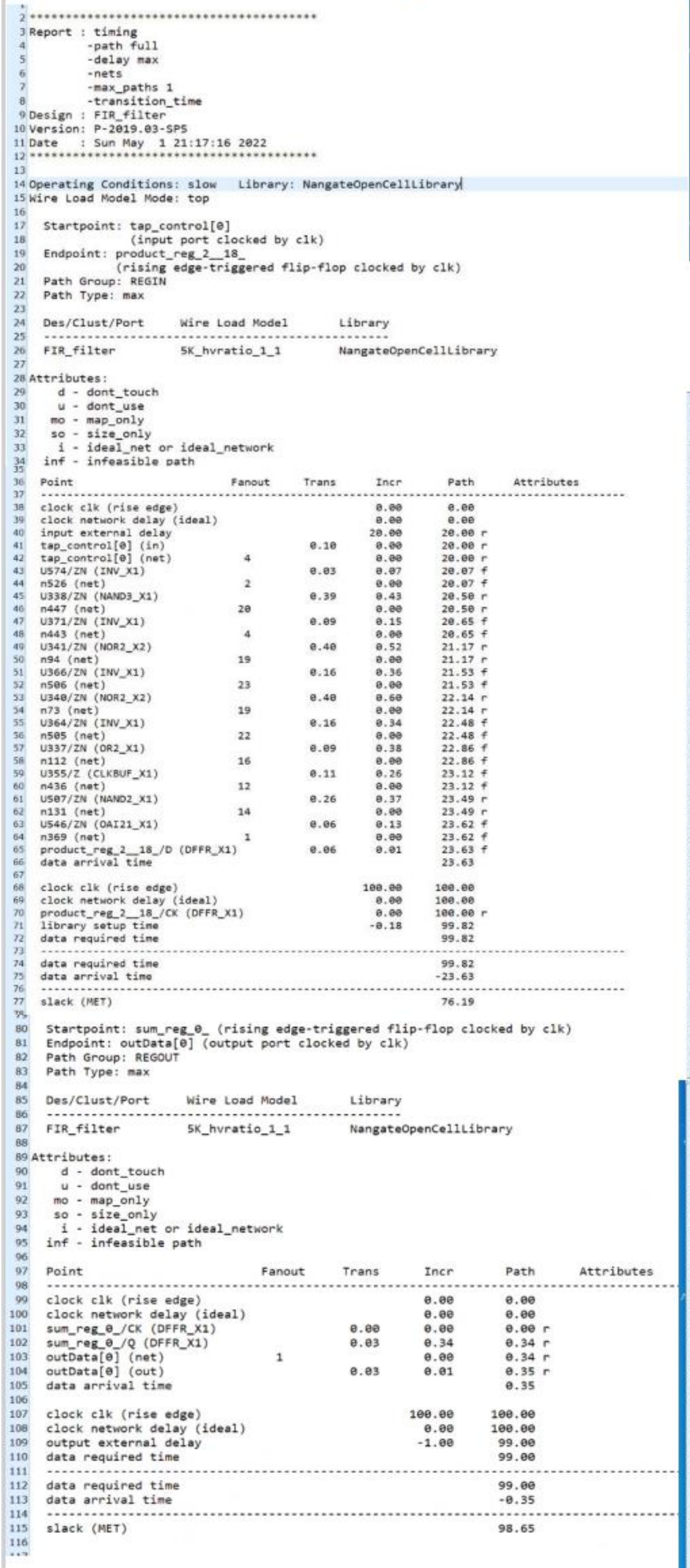
The graph above shows the comparison between the input signal with noise on it and the relatively clean output signal. And, the following is the signal observe from MATLAB.



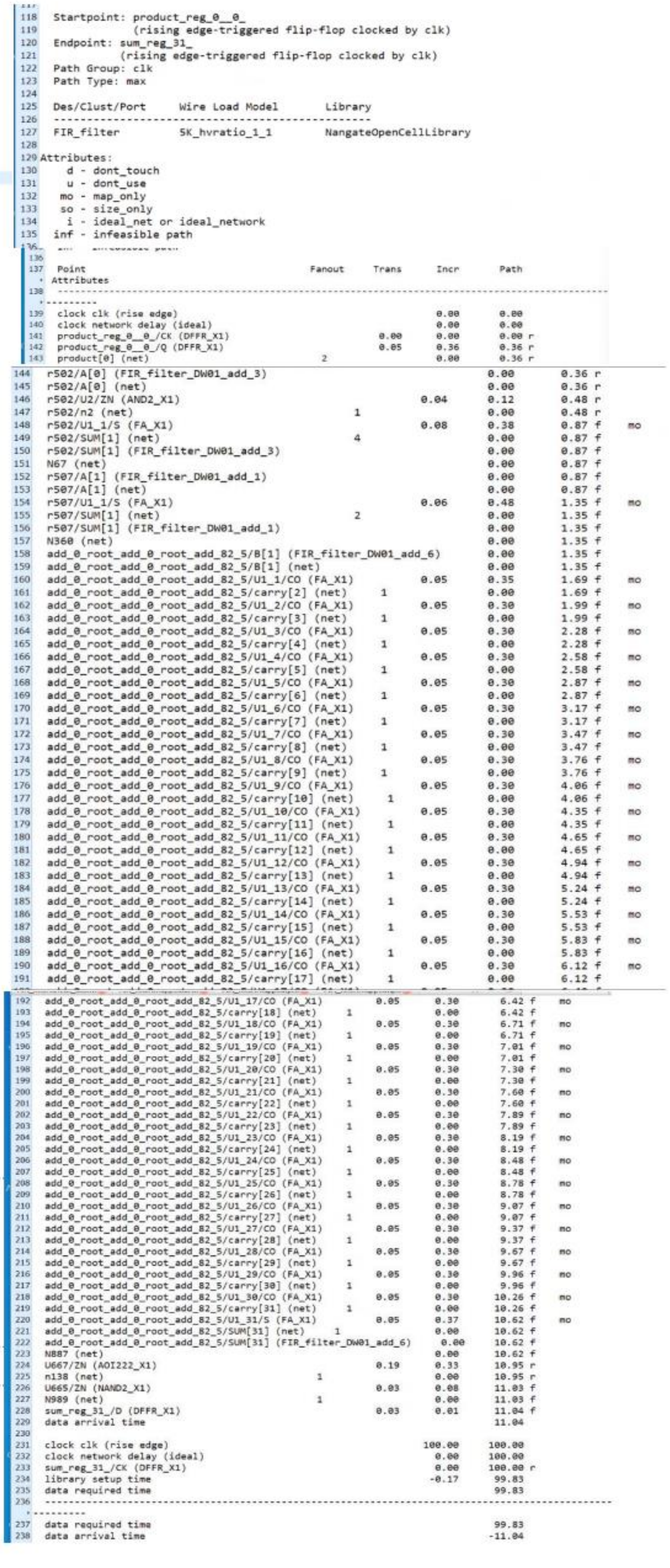
Comment:
From the above graph, it is easy to observe the difference between signal with noise and the output signal after the filtering.

3. Synthesized area, critical path, and power consumption reports.

Critical path report:



```
****************************************
Report : timing
        -path full
        -delay max
        -nets
        -max_paths 1
        -transition_time
Design : FIR_filter
Version: P-2019.03-SP5
Date   : Sun May  1 21:17:16 2022
****************************************

Operating Conditions: slow   Library: NangateOpenCellLibrary
Wire Load Model Mode: top

  Startpoint: tap_control[0]
              (input port clocked by clk)
  Endpoint: product_reg_2__18_
            (rising edge-triggered flip-flop clocked by clk)
  Path Group: REGIN
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  FIR_filter         5K_hvratio_1_1        NangateOpenCellLibrary

Attributes:
    d - dont_touch
    u - dont_use
   mo - map_only
   so - size_only
    i - ideal_net or ideal_network
  inf - infeasible path

  Point                       Fanout     Trans      Incr       Path      Attributes
  ---------------------------------------------------------------------------------
  clock clk (rise edge)                             0.00       0.00
  clock network delay (ideal)                       0.00       0.00
  input external delay                             20.00      20.00 r
  tap_control[0] (in)                     0.10      0.00      20.00 r
  tap_control[0] (net)          4                   0.00      20.00 r
  U574/ZN (INV_X1)                        0.03      0.07      20.07 f
  n526 (net)                    2                   0.00      20.07 f
  U338/ZN (NAND3_X1)                      0.39      0.43      20.50 r
  n447 (net)                   20                   0.00      20.50 r
  U371/ZN (INV_X1)                        0.09      0.15      20.65 f
  n443 (net)                    4                   0.00      20.65 f
  U341/ZN (NOR2_X2)                       0.40      0.52      21.17 r
  n94 (net)                    19                   0.00      21.17 r
  U366/ZN (INV_X1)                        0.16      0.36      21.53 f
  n506 (net)                   23                   0.00      21.53 f
  U340/ZN (NOR2_X2)                       0.40      0.60      22.14 r
  n73 (net)                    19                   0.00      22.14 r
  U364/ZN (INV_X1)                        0.16      0.34      22.48 f
  n505 (net)                   22                   0.00      22.48 f
  U337/ZN (OR2_X1)                        0.09      0.38      22.86 f
  n112 (net)                   16                   0.00      22.86 f
  U355/Z (CLKBUF_X1)                      0.11      0.26      23.12 f
  n436 (net)                   12                   0.00      23.12 f
  U507/ZN (NAND2_X1)                      0.26      0.37      23.49 r
  n131 (net)                   14                   0.00      23.49 r
  U546/ZN (OAI21_X1)                      0.06      0.13      23.62 f
  n369 (net)                    1                   0.00      23.62 f
  product_reg_2__18_/D (DFFR_X1)          0.06      0.01      23.63 f
  data arrival time                                           23.63

  clock clk (rise edge)                           100.00     100.00
  clock network delay (ideal)                       0.00     100.00
  product_reg_2__18_/CK (DFFR_X1)                   0.00     100.00 r
  library setup time                               -0.18      99.82
  data required time                                          99.82
  ---------------------------------------------------------------------------------
  data required time                                          99.82
  data arrival time                                          -23.63
  ---------------------------------------------------------------------------------
  slack (MET)                                                 76.19

  Startpoint: sum_reg_0_ (rising edge-triggered flip-flop clocked by clk)
  Endpoint: outData[0] (output port clocked by clk)
  Path Group: REGOUT
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  FIR_filter         5K_hvratio_1_1        NangateOpenCellLibrary

Attributes:
    d - dont_touch
    u - dont_use
   mo - map_only
   so - size_only
    i - ideal_net or ideal_network
  inf - infeasible path

  Point                       Fanout     Trans      Incr       Path      Attributes
  ---------------------------------------------------------------------------------
  clock clk (rise edge)                             0.00       0.00
  clock network delay (ideal)                       0.00       0.00
  sum_reg_0_/CK (DFFR_X1)                 0.00      0.00       0.00 r
  sum_reg_0_/Q (DFFR_X1)                  0.03      0.34       0.34 r
  outData[0] (net)              1                   0.00       0.34 r
  outData[0] (out)                        0.03      0.01       0.35 r
  data arrival time                                            0.35

  clock clk (rise edge)                           100.00     100.00
  clock network delay (ideal)                       0.00     100.00
  output external delay                            -1.00      99.00
  data required time                                          99.00
  ---------------------------------------------------------------------------------
  data required time                                          99.00
  data arrival time                                           -0.35
  ---------------------------------------------------------------------------------
  slack (MET)                                                 98.65
```

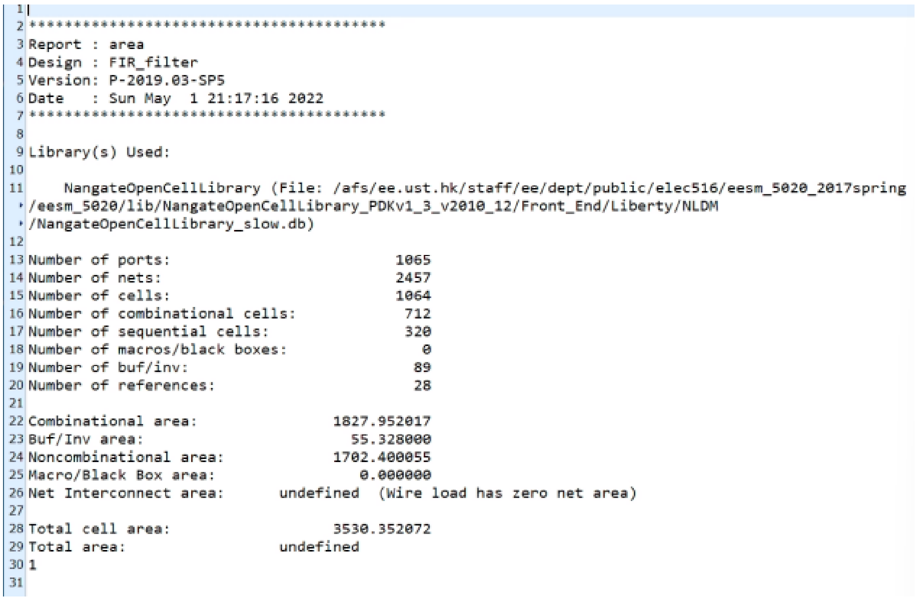


```
  Startpoint: product_reg_0__0_
              (rising edge-triggered flip-flop clocked by clk)
  Endpoint: sum_reg_31_
            (rising edge-triggered flip-flop clocked by clk)
  Path Group: clk
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  FIR_filter         5K_hvratio_1_1        NangateOpenCellLibrary

Attributes:
    d - dont_touch
    u - dont_use
   mo - map_only
   so - size_only
    i - ideal_net or ideal_network
  inf - infeasible path

  Point                                                  Fanout     Trans      Incr       Path
 Attributes
  ----------------------------------------------------------------------------------------------
---------
  clock clk (rise edge)                                                        0.00       0.00
  clock network delay (ideal)                                                  0.00       0.00
  product_reg_0__0_/CK (DFFR_X1)                                    0.00       0.00       0.00 r
  product_reg_0__0_/Q (DFFR_X1)                                     0.05       0.36       0.36 r
  product[0] (net)                                        2                    0.00       0.36 r
  r502/A[0] (FIR_filter_DW01_add_3)                                   0.00       0.36 r
  r502/A[0] (net)                                                     0.00       0.36 r
  r502/U2/ZN (AND2_X1)                                      0.04      0.12       0.48 r
  r502/n2 (net)                                 1                     0.00       0.48 r
  r502/U1_1/S (FA_X1)                                       0.08      0.38       0.87 f    mo
  r502/SUM[1] (net)                             4                     0.00       0.87 f
  r502/SUM[1] (FIR_filter_DW01_add_3)                                 0.00       0.87 f
  N67 (net)                                                           0.00       0.87 f
  r507/A[1] (FIR_filter_DW01_add_1)                                   0.00       0.87 f
  r507/A[1] (net)                                                     0.00       0.87 f
  r507/U1_1/S (FA_X1)                                       0.06      0.48       1.35 f    mo
  r507/SUM[1] (net)                             2                     0.00       1.35 f
  r507/SUM[1] (FIR_filter_DW01_add_1)                                 0.00       1.35 f
  N360 (net)                                                          0.00       1.35 f
  add_0_root_add_0_root_add_82_5/B[1] (FIR_filter_DW01_add_6)         0.00       1.35 f
  add_0_root_add_0_root_add_82_5/B[1] (net)                           0.00       1.35 f
  add_0_root_add_0_root_add_82_5/U1_1/CO (FA_X1)            0.05      0.35       1.69 f    mo
  add_0_root_add_0_root_add_82_5/carry[2] (net)     1                 0.00       1.69 f
  add_0_root_add_0_root_add_82_5/U1_2/CO (FA_X1)            0.05      0.30       1.99 f    mo
  add_0_root_add_0_root_add_82_5/carry[3] (net)     1                 0.00       1.99 f
  add_0_root_add_0_root_add_82_5/U1_3/CO (FA_X1)            0.05      0.30       2.28 f    mo
  add_0_root_add_0_root_add_82_5/carry[4] (net)     1                 0.00       2.28 f
  add_0_root_add_0_root_add_82_5/U1_4/CO (FA_X1)            0.05      0.30       2.58 f    mo
  add_0_root_add_0_root_add_82_5/carry[5] (net)     1                 0.00       2.58 f
  add_0_root_add_0_root_add_82_5/U1_5/CO (FA_X1)            0.05      0.30       2.87 f    mo
  add_0_root_add_0_root_add_82_5/carry[6] (net)     1                 0.00       2.87 f
  add_0_root_add_0_root_add_82_5/U1_6/CO (FA_X1)            0.05      0.30       3.17 f    mo
  add_0_root_add_0_root_add_82_5/carry[7] (net)     1                 0.00       3.17 f
  add_0_root_add_0_root_add_82_5/U1_7/CO (FA_X1)            0.05      0.30       3.47 f    mo
  add_0_root_add_0_root_add_82_5/carry[8] (net)     1                 0.00       3.47 f
  add_0_root_add_0_root_add_82_5/U1_8/CO (FA_X1)            0.05      0.30       3.76 f    mo
  add_0_root_add_0_root_add_82_5/carry[9] (net)     1                 0.00       3.76 f
  add_0_root_add_0_root_add_82_5/U1_9/CO (FA_X1)            0.05      0.30       4.06 f    mo
  add_0_root_add_0_root_add_82_5/carry[10] (net)     1                0.00       4.06 f
  add_0_root_add_0_root_add_82_5/U1_10/CO (FA_X1)           0.05      0.30       4.35 f    mo
  add_0_root_add_0_root_add_82_5/carry[11] (net)     1                0.00       4.35 f
  add_0_root_add_0_root_add_82_5/U1_11/CO (FA_X1)           0.05      0.30       4.65 f    mo
  add_0_root_add_0_root_add_82_5/carry[12] (net)     1                0.00       4.65 f
  add_0_root_add_0_root_add_82_5/U1_12/CO (FA_X1)           0.05      0.30       4.94 f    mo
  add_0_root_add_0_root_add_82_5/carry[13] (net)     1                0.00       4.94 f
  add_0_root_add_0_root_add_82_5/U1_13/CO (FA_X1)           0.05      0.30       5.24 f    mo
  add_0_root_add_0_root_add_82_5/carry[14] (net)     1                0.00       5.24 f
  add_0_root_add_0_root_add_82_5/U1_14/CO (FA_X1)           0.05      0.30       5.53 f    mo
  add_0_root_add_0_root_add_82_5/carry[15] (net)     1                0.00       5.53 f
  add_0_root_add_0_root_add_82_5/U1_15/CO (FA_X1)           0.05      0.30       5.83 f    mo
  add_0_root_add_0_root_add_82_5/carry[16] (net)     1                0.00       5.83 f
  add_0_root_add_0_root_add_82_5/U1_16/CO (FA_X1)           0.05      0.30       6.12 f    mo
  add_0_root_add_0_root_add_82_5/carry[17] (net)     1                0.00       6.12 f
  add_0_root_add_0_root_add_82_5/U1_17/CO (FA_X1)          0.05       0.30       6.42 f    mo
  add_0_root_add_0_root_add_82_5/carry[18] (net)     1                0.00       6.42 f
  add_0_root_add_0_root_add_82_5/U1_18/CO (FA_X1)          0.05       0.30       6.71 f    mo
  add_0_root_add_0_root_add_82_5/carry[19] (net)     1                0.00       6.71 f
  add_0_root_add_0_root_add_82_5/U1_19/CO (FA_X1)          0.05       0.30       7.01 f    mo
  add_0_root_add_0_root_add_82_5/carry[20] (net)     1                0.00       7.01 f
  add_0_root_add_0_root_add_82_5/U1_20/CO (FA_X1)          0.05       0.30       7.30 f    mo
  add_0_root_add_0_root_add_82_5/carry[21] (net)     1                0.00       7.30 f
  add_0_root_add_0_root_add_82_5/U1_21/CO (FA_X1)          0.05       0.30       7.60 f    mo
  add_0_root_add_0_root_add_82_5/carry[22] (net)     1                0.00       7.60 f
  add_0_root_add_0_root_add_82_5/U1_22/CO (FA_X1)          0.05       0.30       7.89 f    mo
  add_0_root_add_0_root_add_82_5/carry[23] (net)     1                0.00       7.89 f
  add_0_root_add_0_root_add_82_5/U1_23/CO (FA_X1)          0.05       0.30       8.19 f    mo
  add_0_root_add_0_root_add_82_5/carry[24] (net)     1                0.00       8.19 f
  add_0_root_add_0_root_add_82_5/U1_24/CO (FA_X1)          0.05       0.30       8.48 f    mo
  add_0_root_add_0_root_add_82_5/carry[25] (net)     1                0.00       8.48 f
  add_0_root_add_0_root_add_82_5/U1_25/CO (FA_X1)          0.05       0.30       8.78 f    mo
  add_0_root_add_0_root_add_82_5/carry[26] (net)     1                0.00       8.78 f
  add_0_root_add_0_root_add_82_5/U1_26/CO (FA_X1)          0.05       0.30       9.07 f    mo
  add_0_root_add_0_root_add_82_5/carry[27] (net)     1                0.00       9.07 f
  add_0_root_add_0_root_add_82_5/U1_27/CO (FA_X1)          0.05       0.30       9.37 f    mo
  add_0_root_add_0_root_add_82_5/carry[28] (net)     1                0.00       9.37 f
  add_0_root_add_0_root_add_82_5/U1_28/CO (FA_X1)          0.05       0.30       9.67 f    mo
  add_0_root_add_0_root_add_82_5/carry[29] (net)     1                0.00       9.67 f
  add_0_root_add_0_root_add_82_5/U1_29/CO (FA_X1)          0.05       0.30       9.96 f    mo
  add_0_root_add_0_root_add_82_5/carry[30] (net)     1                0.00       9.96 f
  add_0_root_add_0_root_add_82_5/U1_30/CO (FA_X1)          0.05       0.30      10.26 f    mo
  add_0_root_add_0_root_add_82_5/carry[31] (net)     1                0.00      10.26 f
  add_0_root_add_0_root_add_82_5/U1_31/S (FA_X1)           0.05       0.37      10.62 f    mo
  add_0_root_add_0_root_add_82_5/SUM[31] (net)     1                  0.00      10.62 f
  add_0_root_add_0_root_add_82_5/SUM[31] (FIR_filter_DW01_add_6)       0.00      10.62 f
  N887 (net)                                                          0.00      10.62 f
  U667/ZN (AOI222_X1)                                      0.19       0.33      10.95 r
  n138 (net)                                      1                   0.00      10.95 r
  U665/ZN (NAND2_X1)                                       0.03       0.08      11.03 f
  N989 (net)                                      1                   0.00      11.03 f
  sum_reg_31_/D (DFFR_X1)                                  0.03       0.01      11.04 f
  data arrival time                                                             11.04

  clock clk (rise edge)                                             100.00     100.00
  clock network delay (ideal)                                         0.00     100.00
  sum_reg_31_/CK (DFFR_X1)                                            0.00     100.00 r
  library setup time                                                 -0.17      99.83
  data required time                                                            99.83
  ----------------------------------------------------------------------------------------------
---------
  data required time                                                            99.83
  data arrival time                                                            -11.04
```

Comment:

The above timing report shows the critical path of the circuit. The critical path should be tap_control[0] to product_reg_2_18, which is 23.63 us of logic time delay.

Area report:

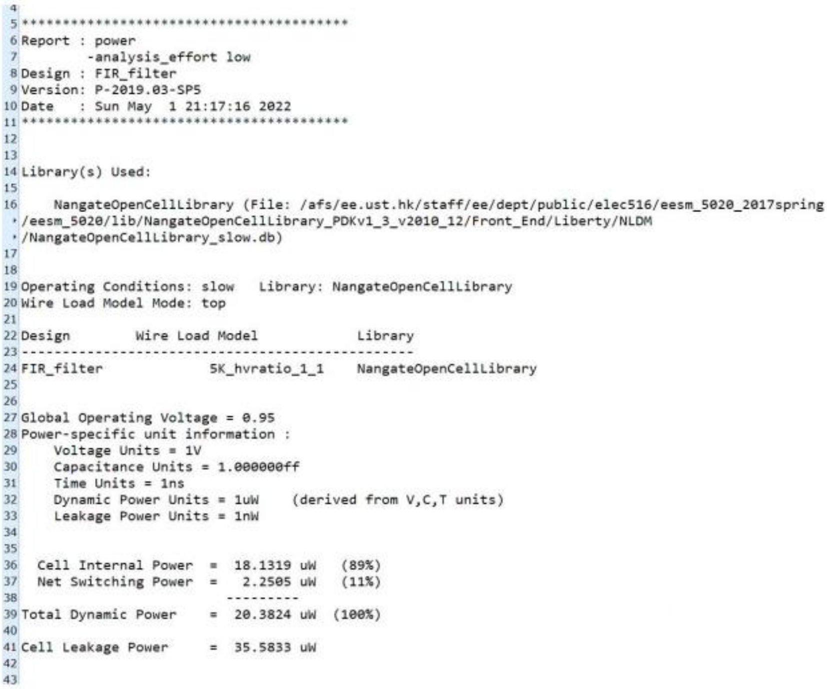


```
****************************************
Report : area
Design : FIR_filter
Version: P-2019.03-SP5
Date   : Sun May  1 21:17:16 2022
****************************************

Library(s) Used:

    NangateOpenCellLibrary (File: /afs/ee.ust.hk/staff/ee/dept/public/elec516/eesm_5020_2017spring
/eesm_5020/lib/NangateOpenCellLibrary_PDKv1_3_v2010_12/Front_End/Liberty/NLDM
/NangateOpenCellLibrary_slow.db)

Number of ports:                         1065
Number of nets:                          2457
Number of cells:                         1064
Number of combinational cells:            712
Number of sequential cells:               320
Number of macros/black boxes:               0
Number of buf/inv:                         89
Number of references:                      28

Combinational area:               1827.952017
Buf/Inv area:                       55.328000
Noncombinational area:            1702.400055
Macro/Black Box area:                0.000000
Net Interconnect area:      undefined  (Wire load has zero net area)

Total cell area:                  3530.352072
Total area:                 undefined
1
```

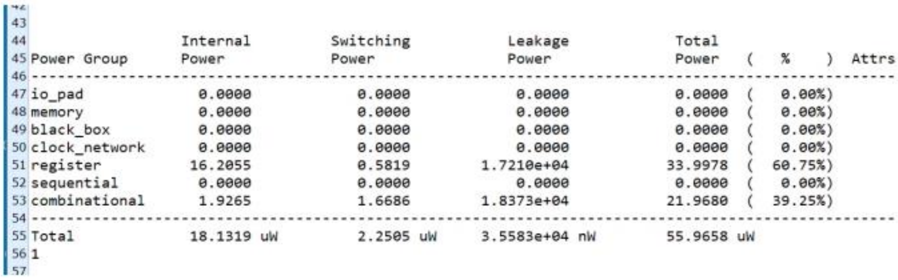
Comment:

The area of the filter is about 3530.

Power consumption report:



```
****************************************
Report : power
        -analysis_effort low
Design : FIR_filter
Version: P-2019.03-SP5
Date   : Sun May  1 21:17:16 2022
****************************************


Library(s) Used:

    NangateOpenCellLibrary (File: /afs/ee.ust.hk/staff/ee/dept/public/elec516/eesm_5020_2017spring
/eesm_5020/lib/NangateOpenCellLibrary_PDKv1_3_v2010_12/Front_End/Liberty/NLDM
/NangateOpenCellLibrary_slow.db)


Operating Conditions: slow   Library: NangateOpenCellLibrary
Wire Load Model Mode: top

Design        Wire Load Model            Library
------------------------------------------------
FIR_filter             5K_hvratio_1_1    NangateOpenCellLibrary


Global Operating Voltage = 0.95
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 1.000000ff
    Time Units = 1ns
    Dynamic Power Units = 1uW    (derived from V,C,T units)
    Leakage Power Units = 1nW


  Cell Internal Power  =  18.1319 uW   (89%)
  Net Switching Power  =   2.2505 uW   (11%)
                         ---------
Total Dynamic Power    =  20.3824 uW  (100%)

Cell Leakage Power     =  35.5833 uW
```



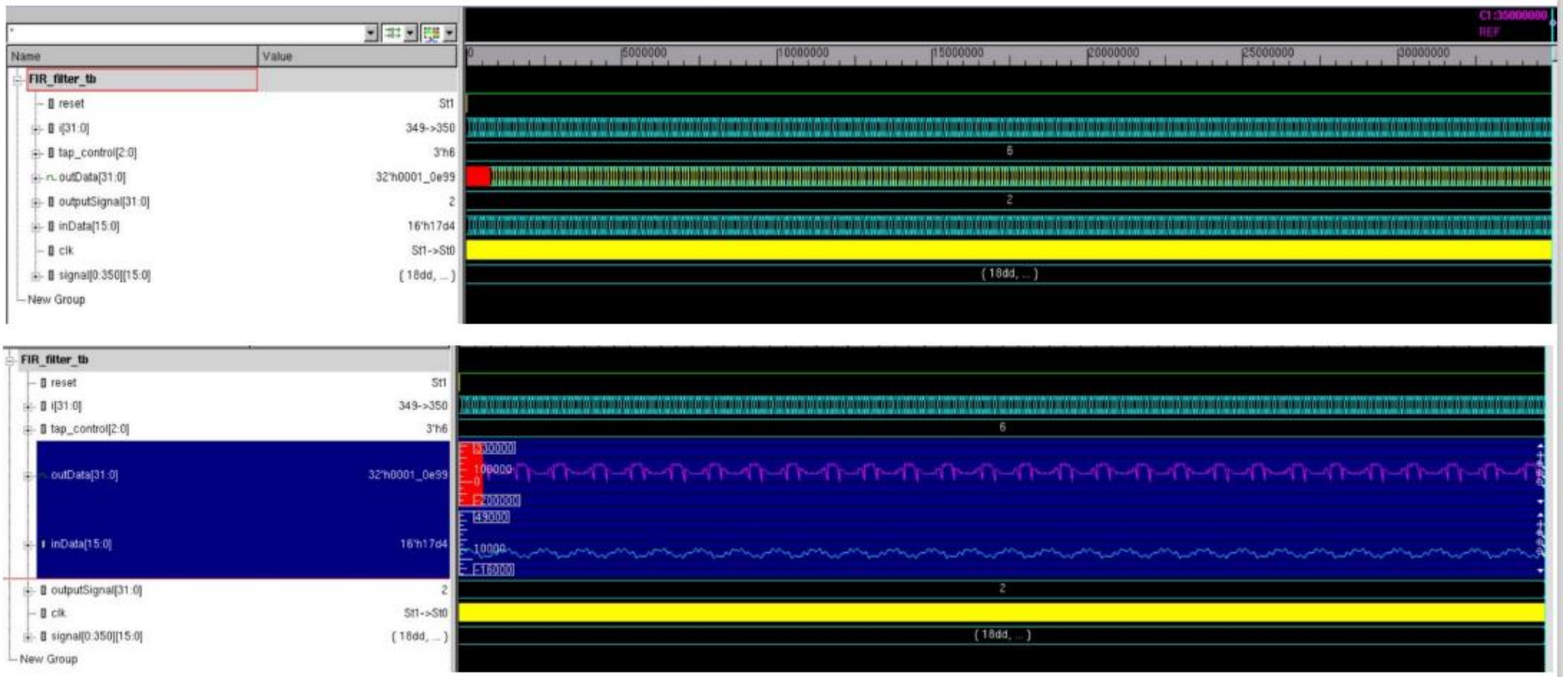
```
                   Internal         Switching           Leakage            Total
Power Group        Power            Power               Power              Power   (   %    )  Attrs
--------------------------------------------------------------------------------------------------
io_pad              0.0000           0.0000            0.0000            0.0000  (   0.00%)
memory              0.0000           0.0000            0.0000            0.0000  (   0.00%)
black_box           0.0000           0.0000            0.0000            0.0000  (   0.00%)
clock_network       0.0000           0.0000            0.0000            0.0000  (   0.00%)
register           16.2055           0.5819        1.7210e+04           33.9978  (  60.75%)
sequential          0.0000           0.0000            0.0000            0.0000  (   0.00%)
combinational       1.9265           1.6686        1.8373e+04           21.9680  (  39.25%)
--------------------------------------------------------------------------------------------------
Total              18.1319 uW        2.2505 uW     3.5583e+04 nW        55.9658 uW
1
```

Comment:

The total power consumption is 55.9658uW. Meanwhile, Register occupied 60% of power consumption, and this will be a good point to optimize the filter in terms of power less. Another thing to be noticed is the leakages power of cell, which is about 35.58uW

4. Screenshot of the post-synthesized simulation.

Post-Synthesis simulation



Name	Value
FIR_filter_tb	
reset	St1
i[31:0]	349->350
tap_control[2:0]	3'h6
outData[31:0]	32'h0001_0e99
outputSignal[31:0]	2
inData[15:0]	16'h17d4
clk	St1->St0
signal[0:350][15:0]	{18dd, ...}
New Group	

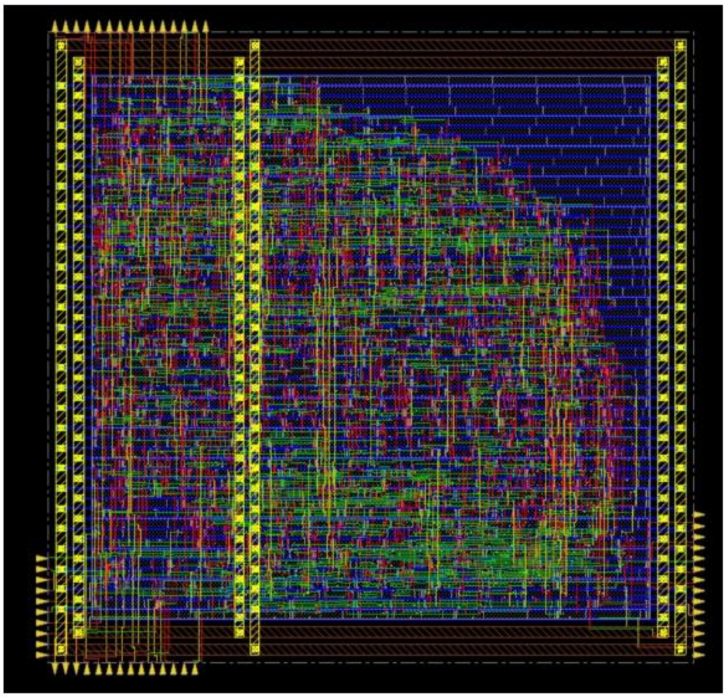
FIR_filter_tb	
reset	St1
i[31:0]	349->350
tap_control[2:0]	3'h6
outData[31:0]	32'h0001_0e99
inData[15:0]	16'h17d4
outputSignal[31:0]	2
clk	St1->St0
signal[0:350][15:0]	{18dd, ...}
New Group	

Comment:

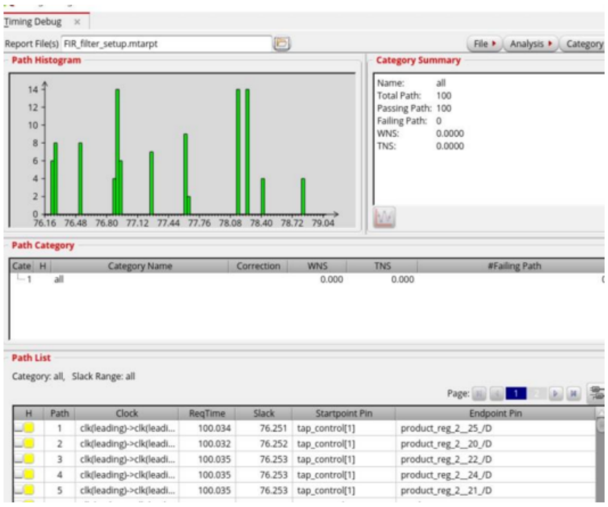
From the waveform, the main difference between the behavior simulation is the signal burr. It is mainly because the delay of the circuit.

5. Screenshot of the layout. The area, timing, and power reports of the layout.

Layout:



Histogram:



Report File(s) FIR_filter_setup.mtarpt

Path Histogram

Category Summary

Name: all
Total Path: 100
Passing Path: 100
Failing Path: 0
WNS: 0.0000
TNS: 0.0000

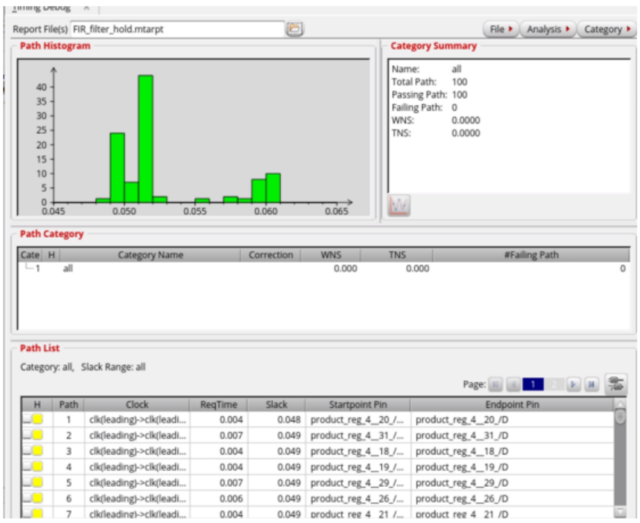
Path Category

Cate	H	Category Name	Correction	WNS	TNS	#Failing Path
1		all		0.000	0.000	(

Path List

Category: all, Slack Range: all

H	Path	Clock	ReqTime	Slack	Startpoint Pin	Endpoint Pin
🟨	1	clk(leading)->clk(leadi...	100.034	76.251	tap_control[1]	product_reg_2__25_/D
🟨	2	clk(leading)->clk(leadi...	100.032	76.252	tap_control[1]	product_reg_2__20_/D
🟨	3	clk(leading)->clk(leadi...	100.035	76.253	tap_control[1]	product_reg_2__22_/D
🟨	4	clk(leading)->clk(leadi...	100.035	76.253	tap_control[1]	product_reg_2__24_/D
🟨	5	clk(leading)->clk(leadi...	100.035	76.253	tap_control[1]	product_reg_2__21_/D



Report File(s) FIR_filter_hold.mtarpt

Path Histogram

Category Summary

Name: all
Total Path: 100
Passing Path: 100
Failing Path: 0
WNS: 0.0000
TNS: 0.0000

Path Category

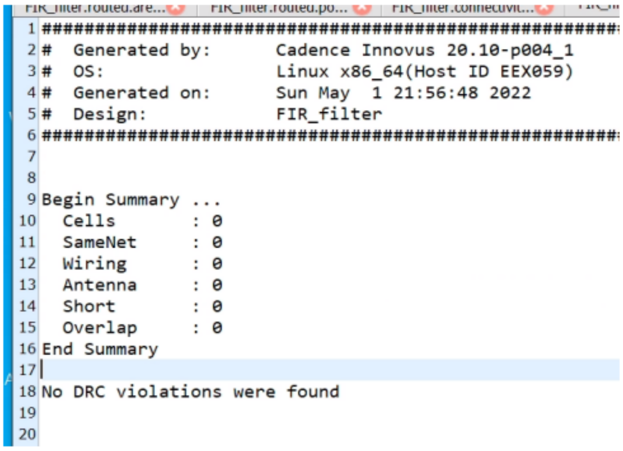
Cate	H	Category Name	Correction	WNS	TNS	#Failing Path
1		all		0.000	0.000	0

Path List

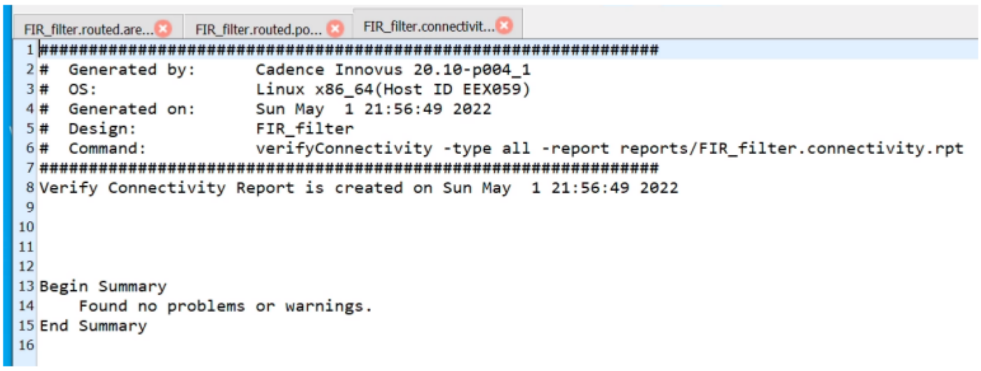
Category: all, Slack Range: all

H	Path	Clock	ReqTime	Slack	Startpoint Pin	Endpoint Pin
🟨	1	clk(leading)->clk(leadi...	0.004	0.048	product_reg_4__20_/...	product_reg_4__20_/D
🟨	2	clk(leading)->clk(leadi...	0.007	0.049	product_reg_4__31_/...	product_reg_4__31_/D
🟨	3	clk(leading)->clk(leadi...	0.004	0.049	product_reg_4__18_/...	product_reg_4__18_/D
🟨	4	clk(leading)->clk(leadi...	0.004	0.049	product_reg_4__19_/...	product_reg_4__19_/D
🟨	5	clk(leading)->clk(leadi...	0.007	0.049	product_reg_4__29_/...	product_reg_4__29_/D
🟨	6	clk(leading)->clk(leadi...	0.006	0.049	product_reg_4__26_/...	product_reg_4__26_/D
🟨	7	clk(leading)->clk(leadi...	0.004	0.049	product_reg_4__21_/...	product_reg_4__21_/D

Connection and DRC verification:



```
#############################################################
#   Generated by:       Cadence Innovus 20.10-p004_1
#   OS:                 Linux x86_64(Host ID EEX059)
#   Generated on:       Sun May  1 21:56:48 2022
#   Design:             FIR_filter
#############################################################


Begin Summary ...
  Cells        : 0
  SameNet      : 0
  Wiring       : 0
  Antenna      : 0
  Short        : 0
  Overlap      : 0
End Summary

No DRC violations were found


```

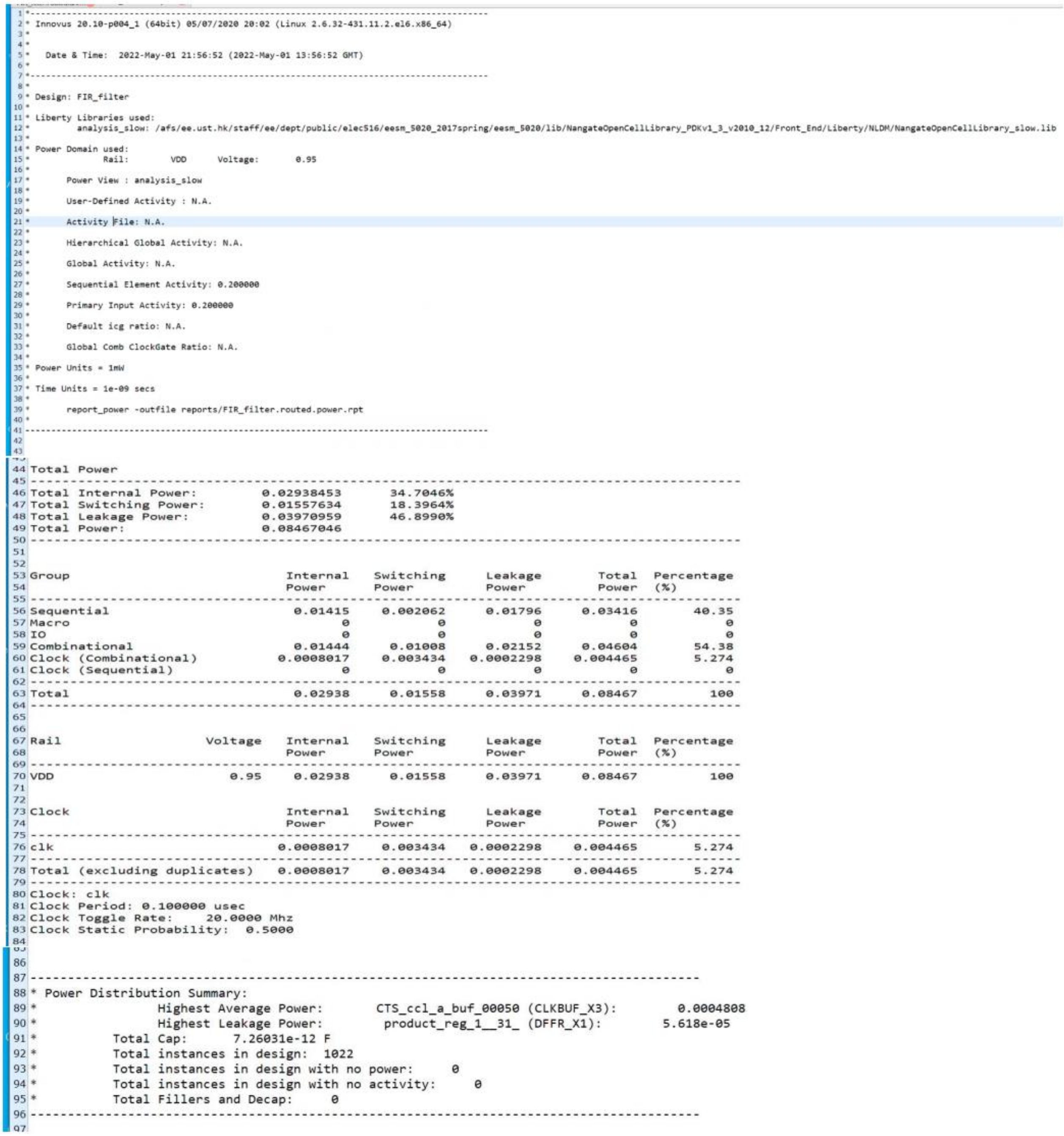


```
###############################################################
#   Generated by:       Cadence Innovus 20.10-p004_1
#   OS:                 Linux x86_64(Host ID EEX059)
#   Generated on:       Sun May  1 21:56:49 2022
#   Design:             FIR_filter
#   Command:            verifyConnectivity -type all -report reports/FIR_filter.connectivity.rpt
###############################################################
Verify Connectivity Report is created on Sun May  1 21:56:49 2022




Begin Summary
    Found no problems or warnings.
End Summary

```

Comment:

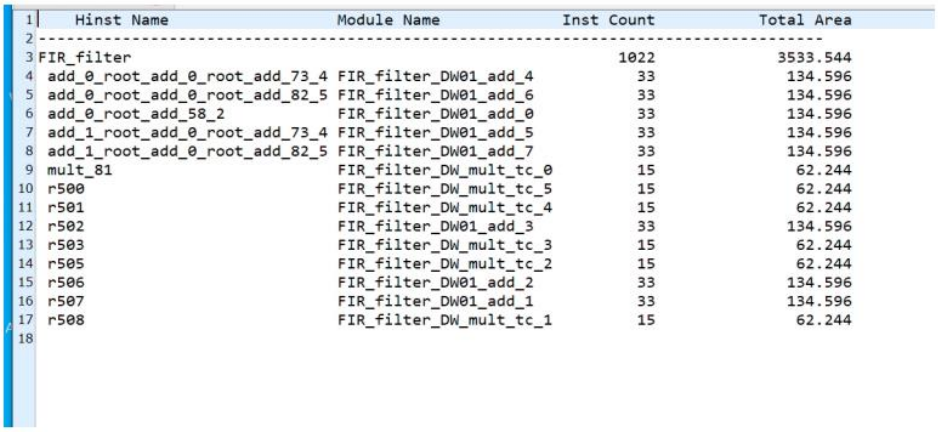
The layout is shown above, meanwhile, the histogram of hold time and setup time analysis also attach above. There is no hold time violation and setup time violation. Also, the variation of LVS and DRC are correct.

Power consumption report:



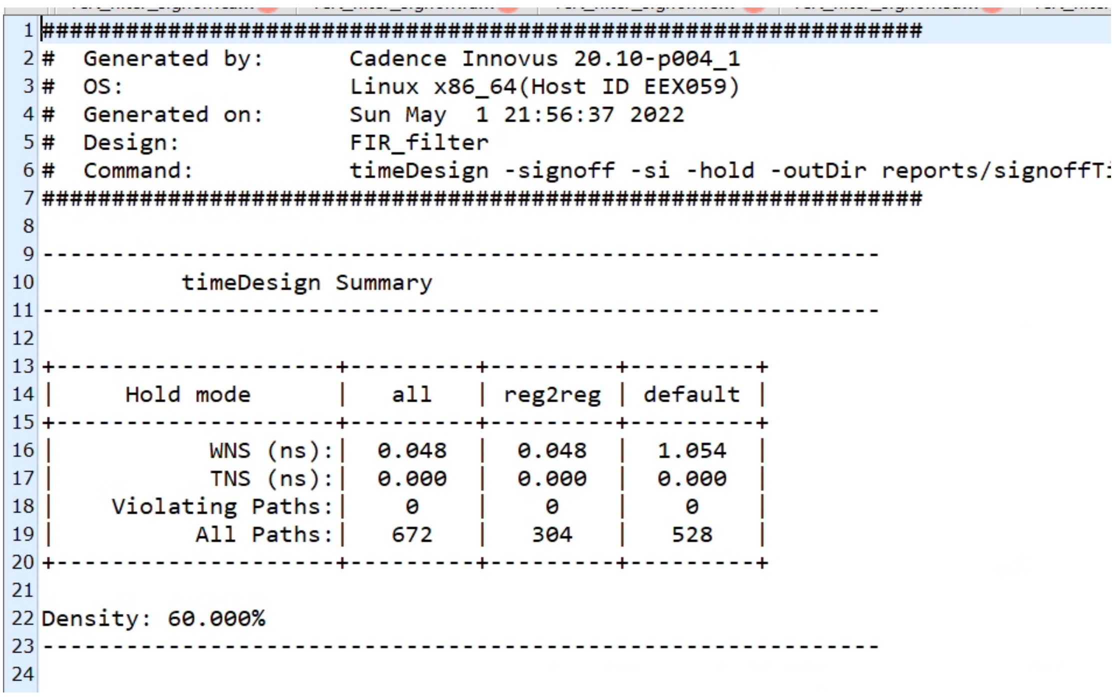
```
*---------------------------------------------------------------------------------
* Innovus 20.10-p004_1 (64bit) 05/07/2020 20:02 (Linux 2.6.32-431.11.2.el6.x86_64)
*
*
*   Date & Time:  2022-May-01 21:56:52 (2022-May-01 13:56:52 GMT)
*
*---------------------------------------------------------------------------------
*
* Design: FIR_filter
*
* Liberty Libraries used:
*         analysis_slow: /afs/ee.ust.hk/staff/ee/dept/public/elec516/eesm_5020_2017spring/eesm_5020/lib/NangateOpenCellLibrary_PDKv1_3_v2010_12/Front_End/Liberty/NLDM/NangateOpenCellLibrary_slow.lib
*
* Power Domain used:
*               Rail:        VDD      Voltage:       0.95
*
*       Power View : analysis_slow
*
*       User-Defined Activity : N.A.
*
*       Activity File: N.A.
*
*       Hierarchical Global Activity: N.A.
*
*       Global Activity: N.A.
*
*       Sequential Element Activity: 0.200000
*
*       Primary Input Activity: 0.200000
*
*       Default icg ratio: N.A.
*
*       Global Comb ClockGate Ratio: N.A.
*
* Power Units = 1mW
*
* Time Units = 1e-09 secs
*
*       report_power -outfile reports/FIR_filter.routed.power.rpt
*
-----------------------------------------------------------------------------------


Total Power
-----------------------------------------------------------------------------------------
Total Internal Power:          0.02938453      34.7046%
Total Switching Power:         0.01557634      18.3964%
Total Leakage Power:           0.03970959      46.8990%
Total Power:                   0.08467046
-----------------------------------------------------------------------------------------


Group                           Internal   Switching     Leakage       Total  Percentage
                                Power      Power         Power         Power  (%)
-----------------------------------------------------------------------------------------
Sequential                       0.01415    0.002062     0.01796     0.03416       40.35
Macro                                  0           0           0           0           0
IO                                     0           0           0           0           0
Combinational                    0.01444     0.01008     0.02152     0.04604       54.38
Clock (Combinational)          0.0008017    0.003434   0.0002298    0.004465       5.274
Clock (Sequential)                     0           0           0           0           0
-----------------------------------------------------------------------------------------
Total                            0.02938     0.01558     0.03971     0.08467         100
-----------------------------------------------------------------------------------------


Rail                  Voltage   Internal   Switching     Leakage       Total  Percentage
                                Power      Power         Power         Power  (%)
-----------------------------------------------------------------------------------------
VDD                      0.95    0.02938     0.01558     0.03971     0.08467         100


Clock                           Internal   Switching     Leakage       Total  Percentage
                                Power      Power         Power         Power  (%)
-----------------------------------------------------------------------------------------
clk                            0.0008017    0.003434   0.0002298    0.004465       5.274
-----------------------------------------------------------------------------------------
Total (excluding duplicates)   0.0008017    0.003434   0.0002298    0.004465       5.274
-----------------------------------------------------------------------------------------
Clock: clk
Clock Period: 0.100000 usec
Clock Toggle Rate:    20.0000 Mhz
Clock Static Probability:  0.5000


-----------------------------------------------------------------------------------------
* Power Distribution Summary:
*              Highest Average Power:      CTS_ccl_a_buf_00050 (CLKBUF_X3):        0.0004808
*              Highest Leakage Power:       product_reg_1__31_ (DFFR_X1):        5.618e-05
*         Total Cap:      7.26031e-12 F
*         Total instances in design:  1022
*         Total instances in design with no power:    0
*         Total instances in design with no activity:    0
*         Total Fillers and Decap:     0
-----------------------------------------------------------------------------------------
```

Area report:



```
  Hinst Name                  Module Name              Inst Count         Total Area
-------------------------------------------------------------------------------------
FIR_filter                                                   1022           3533.544
 add_0_root_add_0_root_add_73_4 FIR_filter_DW01_add_4          33            134.596
 add_0_root_add_0_root_add_82_5 FIR_filter_DW01_add_6          33            134.596
 add_0_root_add_58_2            FIR_filter_DW01_add_0          33            134.596
 add_1_root_add_0_root_add_73_4 FIR_filter_DW01_add_5          33            134.596
 add_1_root_add_0_root_add_82_5 FIR_filter_DW01_add_7          33            134.596
 mult_81                        FIR_filter_DW_mult_tc_0        15             62.244
 r500                           FIR_filter_DW_mult_tc_5        15             62.244
 r501                           FIR_filter_DW_mult_tc_4        15             62.244
 r502                           FIR_filter_DW01_add_3          33            134.596
 r503                           FIR_filter_DW_mult_tc_3        15             62.244
 r505                           FIR_filter_DW_mult_tc_2        15             62.244
 r506                           FIR_filter_DW01_add_2          33            134.596
 r507                           FIR_filter_DW01_add_1          33            134.596
 r508                           FIR_filter_DW_mult_tc_1        15             62.244
```

Timing report:

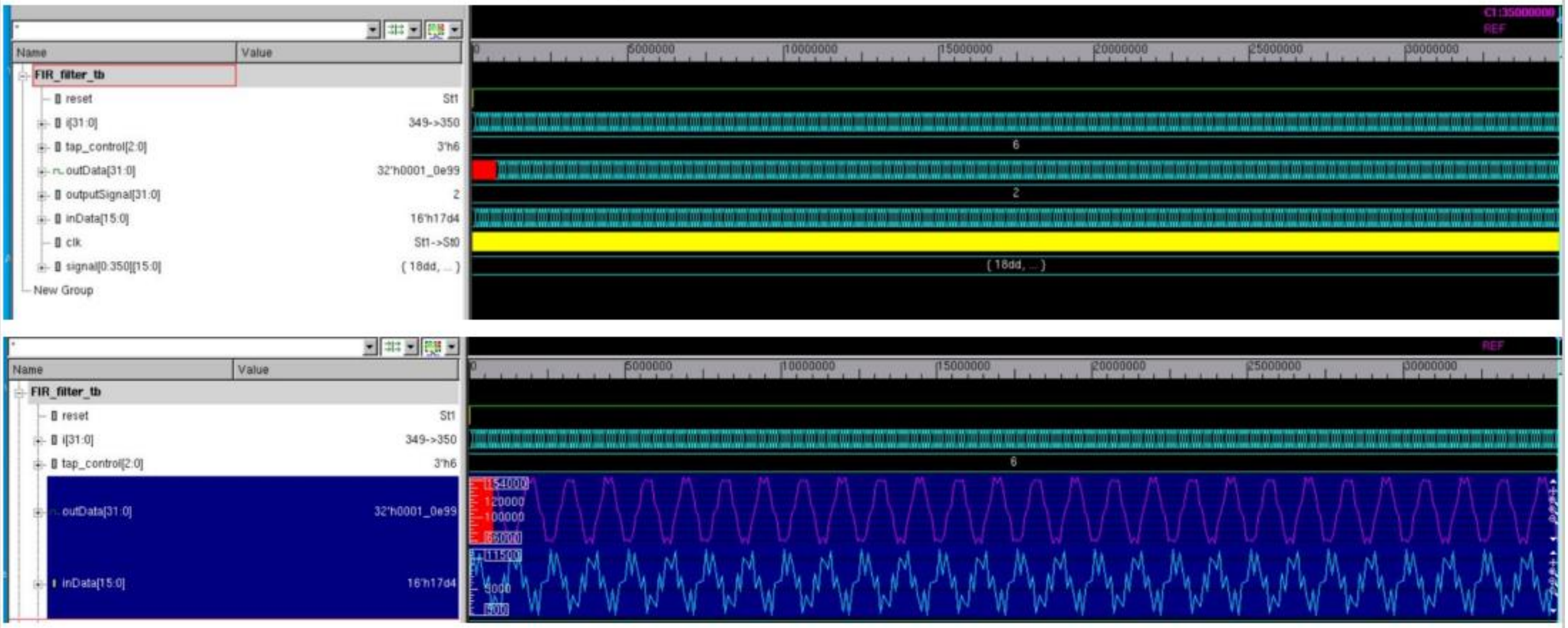


```
#################################################################
#   Generated by:       Cadence Innovus 20.10-p004_1
#   OS:                 Linux x86_64(Host ID EEX059)
#   Generated on:       Sun May  1 21:56:37 2022
#   Design:             FIR_filter
#   Command:            timeDesign -signoff -si -hold -outDir reports/signoffT:
#################################################################

------------------------------------------------------------
          timeDesign Summary
------------------------------------------------------------

+--------------------+---------+---------+---------+
|     Hold mode      |   all   | reg2reg | default |
+--------------------+---------+---------+---------+
|           WNS (ns):|  0.048  |  0.048  |  1.054  |
|           TNS (ns):|  0.000  |  0.000  |  0.000  |
|    Violating Paths:|    0    |    0    |    0    |
|          All Paths:|   672   |   304   |   528   |
+--------------------+---------+---------+---------+

Density: 60.000%
------------------------------------------------------------
```

Comment:

From the above report, there is no hold time violation and setup time violation for layout. The total area of the layout is 3533, and the power is illustrate clearly in the report above.

6. Screenshot of the post-layout simulation.



7. Path to the design assignment:

/afs/ee.ust.hk/staff/ee/bxieaf/eesm5020/FIR_FILTER/