BIRZEIT UNIVERSITY

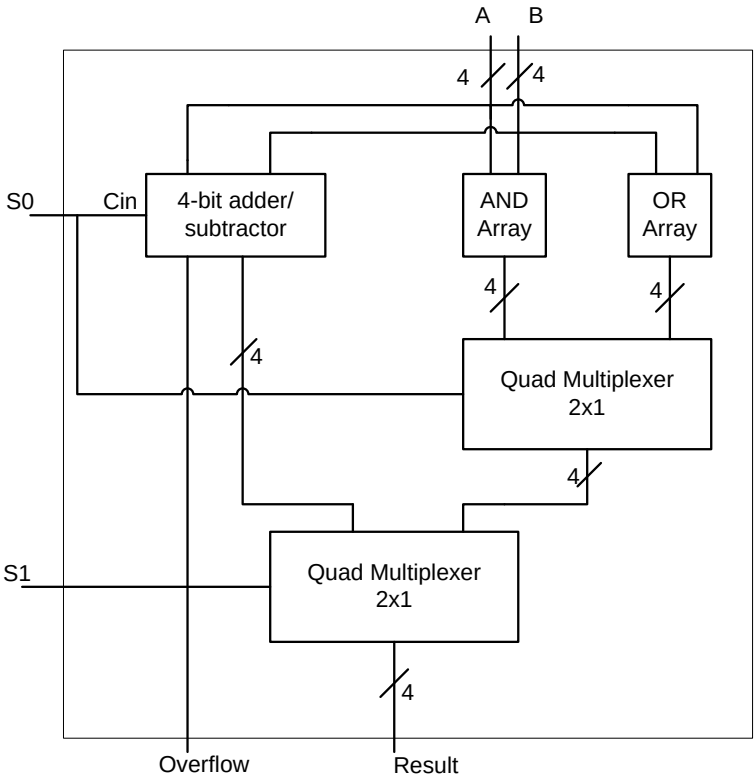
Faculty of Engineering and Technology – Electrical and Computer Engineering Department

First Semester 2017/2018 ENCS234 – Verilog Assignment

Deadline: 3 (for SMW) or 4 (for TR) /1/2018 (During the class)

Given the following Combinational circuit, Use Verilog HDL on Quartus tool to

a. Implement the 1-bit adder and use it to build 4-bit adder structurally
b. Implement the MUX2x1 and then use it to build the Quad MUX 2x1 structurally.
c. Implement the 4-bit OR Array
d. Implement the 4-bit AND Array
e. Use the blocks you implemented in the parts above to build the final system shown in the figure.
f. You should show simulation results for each of the above parts



In addition to building the Quartus project, you need to write down one report for **each student** that includes the following items:

1. System Design.
2. Verilog code.
3. Simulation results.

There would be a discussion for each project with date allocated by the instructors.

Note: There is no group work