Full-Custom Design *8-bit CAM using 9T SRAM*

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***Abstract*—**CAM memory, also known as Content-Addressable Memory, is a specialized type of computer memory that allows for quick and efficient searching and retrieval of data. Unlike traditional memory systems that require specific addresses to access stored information, cam memory enables data to be retrieved based on its content. It stores data in a way that associates each item with a unique identifier, allowing for direct and immediate retrieval without the need for time-consuming searches. 9T SRAM refers to a specific design variant of Static Random Access Memory (SRAM), a type of volatile computer memory that stores data as long as power is supplied. The 9T SRAM design is notable for its reduced power consumption and improved stability compared to traditional 6T SRAM cells. The additional transistors in the 9T SRAM cell allow for enhanced read and write operations, reducing the risk of data corruption due to various noise sources. The 8-bit Full-Custom Design CAM will be designed and implemented in this paper using 9T SRAM and a 22 nm process file. Additionally, we will walk through the process of developing the schematics and the architecture of each component needed to create the final 8-bit CAM, which has been optimized for area and power without compromising the CAM's searching capabilities.

Keywords— *CAM,SRAM, Power, Layout, Schematic*.

I. INTRODUCTION

RAM, which stands for Random Access Memory, is a fundamental component of computer systems that provides fast and temporary storage for data and instructions. It serves as the working memory where the CPU can quickly access and manipulate information by giving it target address during computer operations ,when searching in RAM, it accepts the data's address as an input and returns the address's content, this technique take many clocks until the necessary data that saved in RAM is obtained [1].

CAM stands for Content-Addressable Memory. It is a specialized type of computer memory that allows for rapid searching and retrieval of data based on its content. Unlike RAM, where data is accessed by specifying memory addresses, CAM memory allows data to be retrieved by matching its content with the desired search criteria [2] .

CAM memory is organized in a way that associates each stored item with a unique identifier or tag. When a search is performed, the search data is compared in parallel with the stored content across all memory locations. The memory returns the address or location where a match is found, enabling direct and immediate retrieval of the desired data in one clock cycle , that make it useful in applications that require fast and efficient data retrieval and pattern matching. It finds applications in areas such as database management, network routing, cache memory, and associative computing tasks.

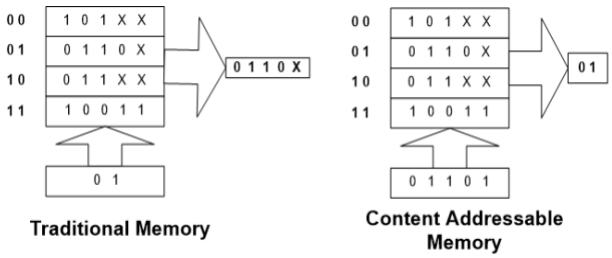

Figure 1: RAM versus CAM in read operation

8-bit Content-Addressable Memory (CAM) designed using a 9T SRAM (Static Random Access Memory) cell. The 9T SRAM cell design shown in (Figure 2) is known for its improved stability and reduced power consumption compared to traditional 6T SRAM cells. This can be advantageous for implementing a CAM because stability is crucial for accurate content-based matching , but it might introduce additional complexity and area overhead compared to CAM designs using 6T or 8T SRAM [3].

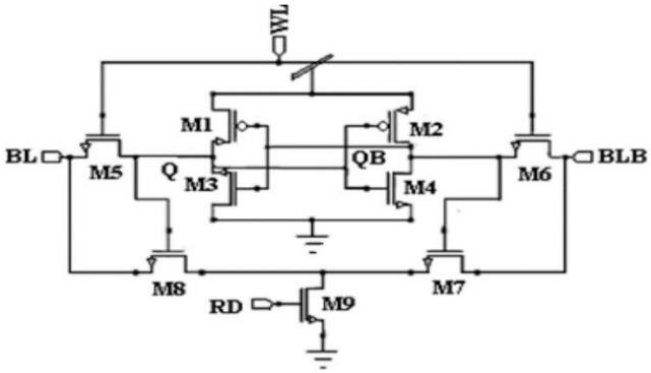

Figure 2: 9T SRAM circuit

II. DESIGN AND IMPLEMENTATION

In order to build 8-bit CAM using 9T SRAM, a number of components must first be designed and tested

independently before being combined as one block in the 8-bit CAM scheme. The following are these components:

A. Invertor

The simplest part needed to make the overall CAM memory design is the invertor , it made from one CMOS and one NMOS , the design and layout of invertor shown in the following figures.

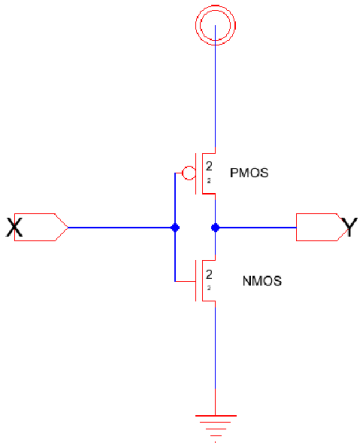

Figure 3: Invertor schematic

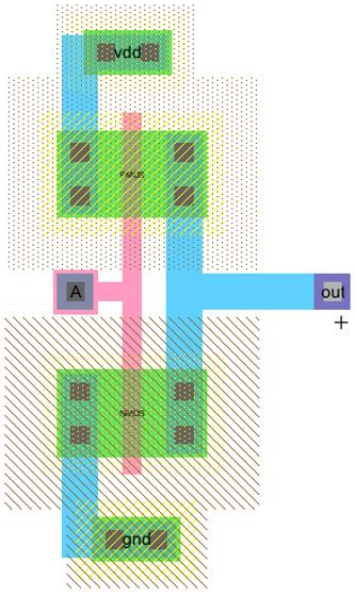

Figure 4: Invertor Layout

B. 9T SRAM

9T SRAM designed as Figure 5 , it consists of two cross-coupled inverters and five additional access transistors so it used 9 transistors .

9T SRAM has the following pins :

1. LB and BLB : these are the input lines that connect to the storage node of the SRAM cell.
2. Wordline (WL) : The wordline is the control line that activates or selects the SRAM cell during read and write operations. When the wordline is activated, it allows access to the storage .
3. RD : it is control input that determines whether a read operation is performed on the SRAM cell , it isolate data in SRAM during reading operation.
4. Q and QB : These outputs indicate the logical state stored in the SRAM cell.

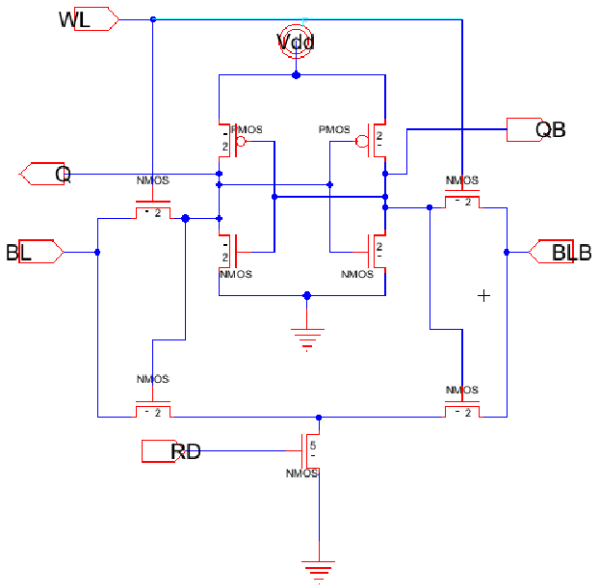

Figure 5: 9T SRAM schematic

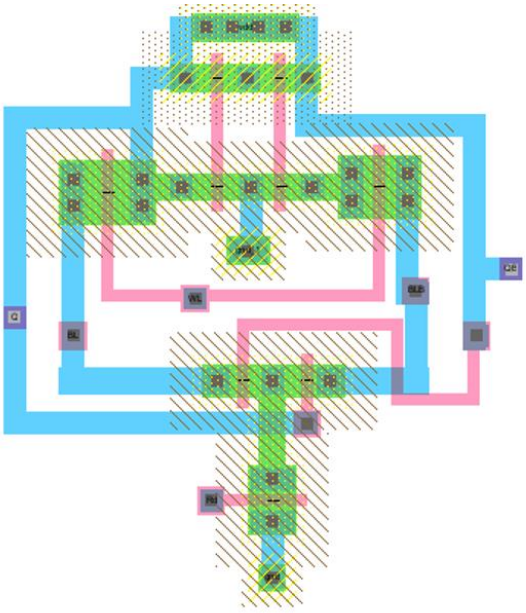

Figure 6: 9T SRAM Layout

C. 1-Bit CAM

A 1-Bit Content-Addressable Memory (CAM) is capable of performing parallel search operations and determining whether a given input data (CAM_data) pattern exists within its memory cells (Q).

1-Bit CAM schematic and layout shown as the following figures , it compare CAM_data and Q of SRAM as the following equation :

Output= (CAM_data **XOR** Q)'

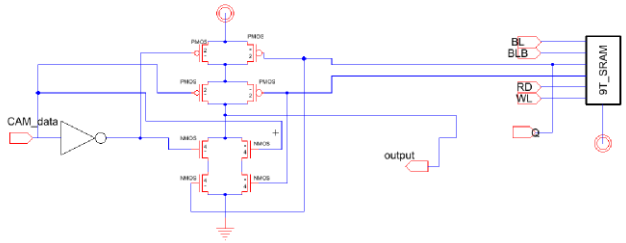

Figure 7: 1-Bit CAM schematic

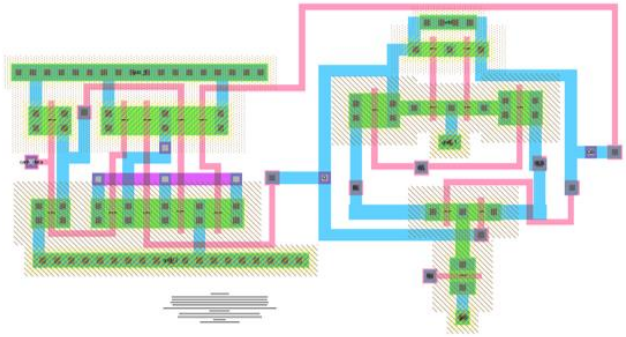

Figure 8: 1-Bit CAM Layout

D. 3-Bit NOR

The 3-Bit NOR gate implementation used to build 3x8 decoder , NOR gate used in decoder instead of AND gate to reduce the number of transistors in the overall design .The following figures show schematic and layout of 3-Bit NOR.

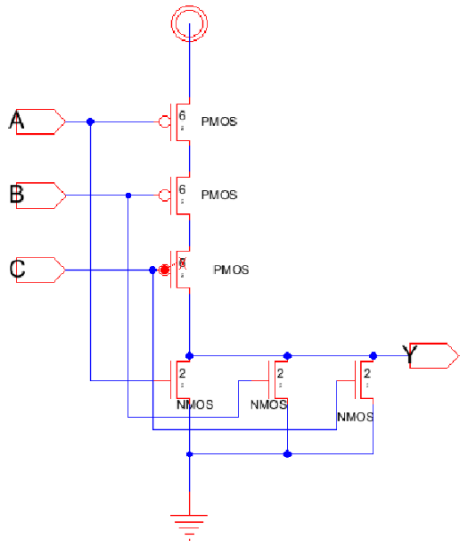

Figure 9: 3-Bit NOR schematic

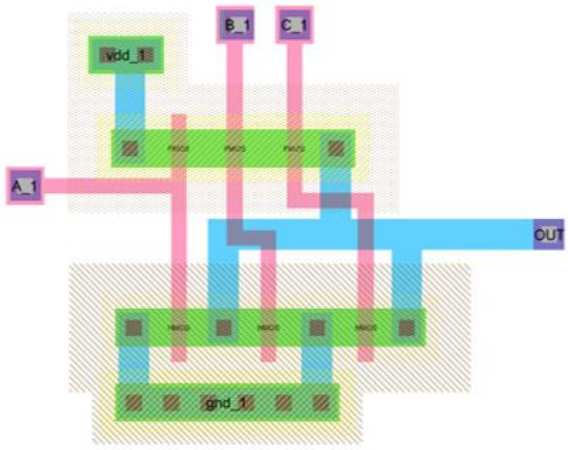

Figure 10: 3-Bit NOR Layout

E. 3x8 Decoder

This piece is used in the overall design to specify the address of the cell that wanted to write the data on it, and since the memory consists of eight cells, this means that it needs three bits to express its addresses. The following figures show the schematic and layout of 3x8 decoder.

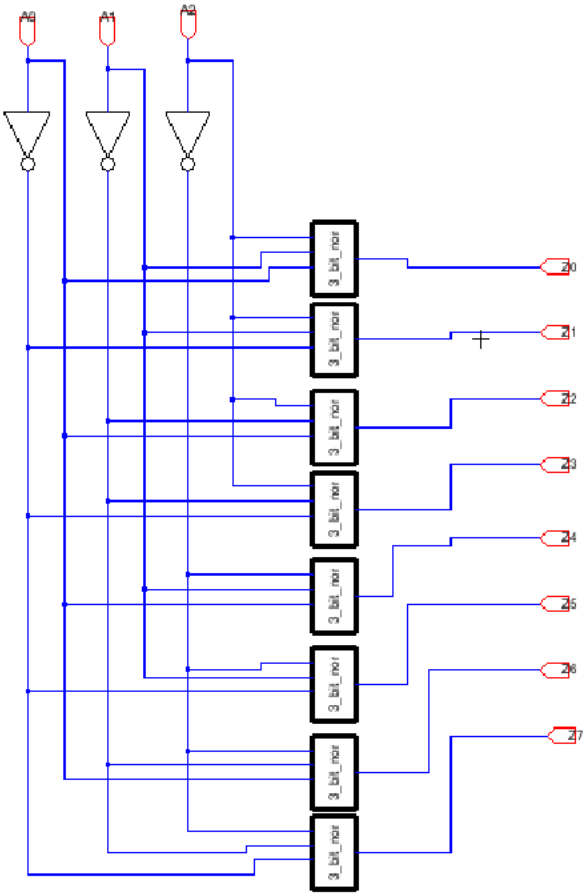

Figure 11: 3x8 decoder schematic

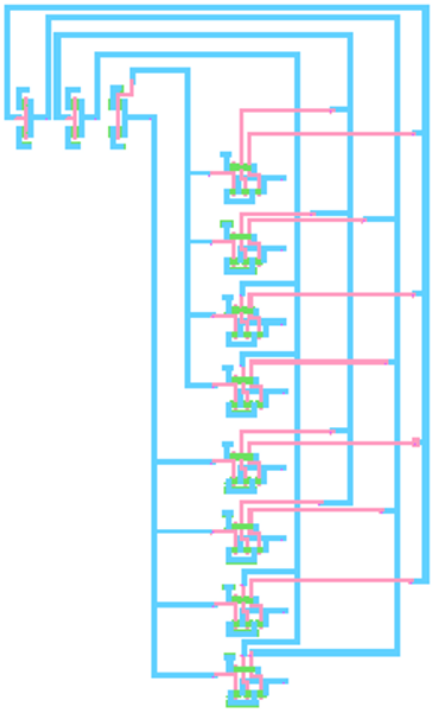

Figure 12: 3x8 decoder Layout

F. 8-Bit NAND

The 8-Bit NAND gate implementation used in the overall design for two thing , the first one to detect if the all 8-bit data that we want to search for are in the cell 1-Bit CAMs , if all input data equal cell 1-bit CAMs , NAND will return zero , the second one to detect if at least one cell of the memory has the input data it will return one. The following figures show schematic and layout of 8-Bit NAND.

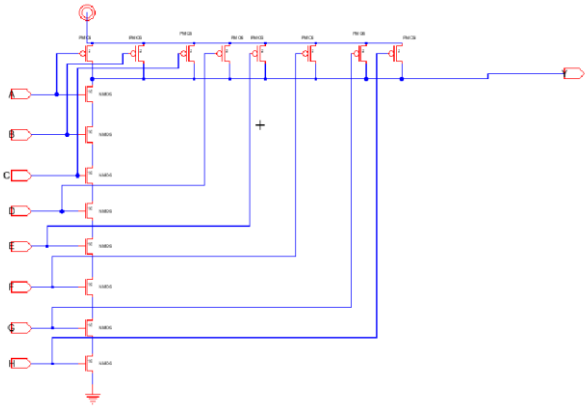

Figure 13: 8-Bit NAND schematic

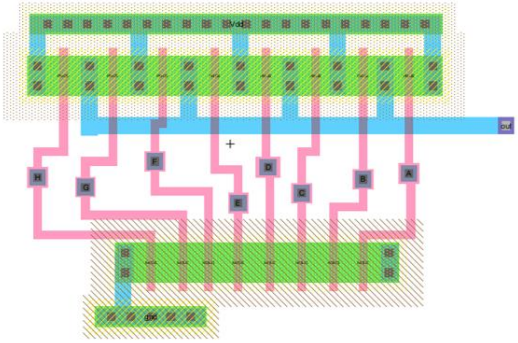

Figure 14: 8-Bit NAND Layout

G. 8-Bit CAM

The Full-Custom design of 8-bit CAM using 9T RAM was designed using all the previous components and connecting them properly, to write 8-bit on one of the memory cells and enter 8-bit through the CAM data to search for it if it exists or not in the CAM memory. The following figures show the schematic and layout of 8-bit CAM.

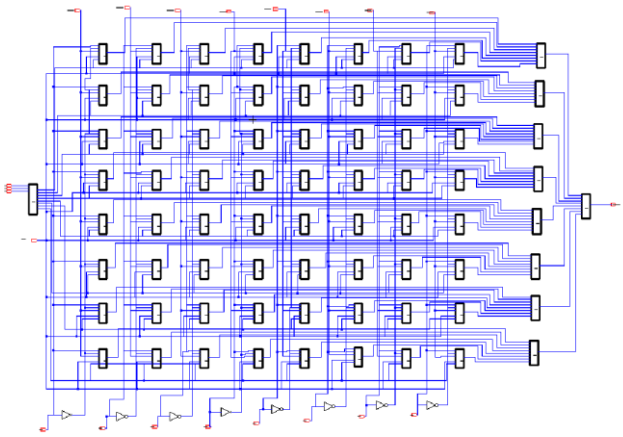

Figure 15: 8-Bit CAM schematic

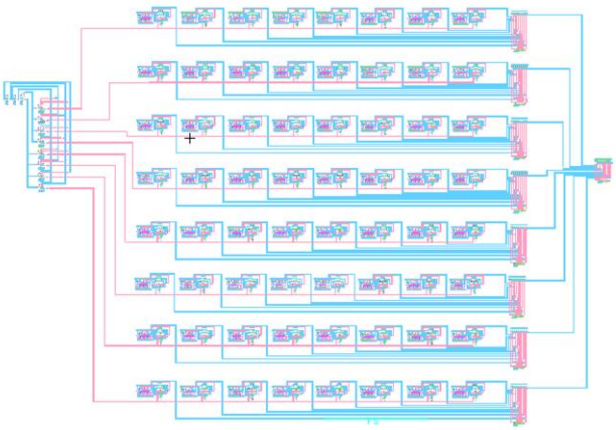

Figure 16: 8-Bit CAM Layout

III. AREA, POWER, AND DELAY OPTIMIZATION

After reading about the power consumption and delay and experimenting with many values for the transistor width, we reached the table shown below, so we took the value of two as the best value for the transistor width due to the circuit's uses as a compromise for delay and power consumption.

Table 1 : power consumption and delay for different size of cmos

width	power	Delay
2	7nw	0.612ns
5	20nw	0.587ns
6	30nw	0.463ns
12	50nw	0.322ns
8	40nw	0.411ns
1	4nw	0.677ns

In terms of space optimization and therefore cost, we initially built the decoder with the circuit shown in the following figure but then found better output equations to reduce the number of transistors that used.

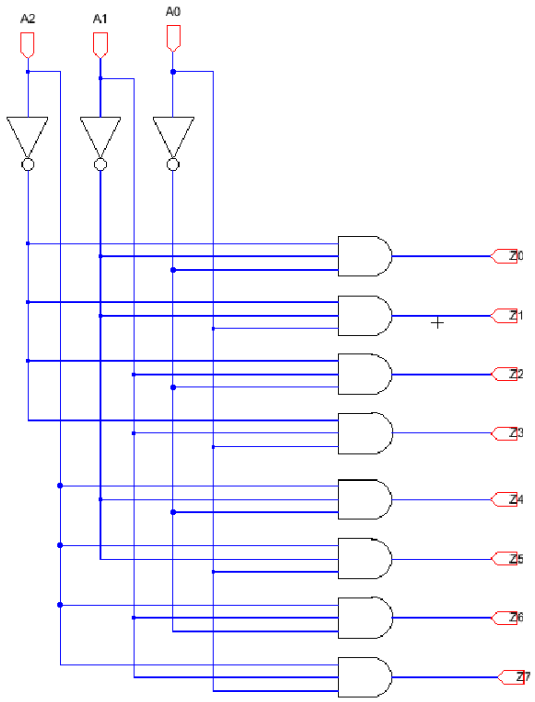

Figure 17:old decoder design

The following decoder design reduce number of transistors from 64 to 48 transistors.

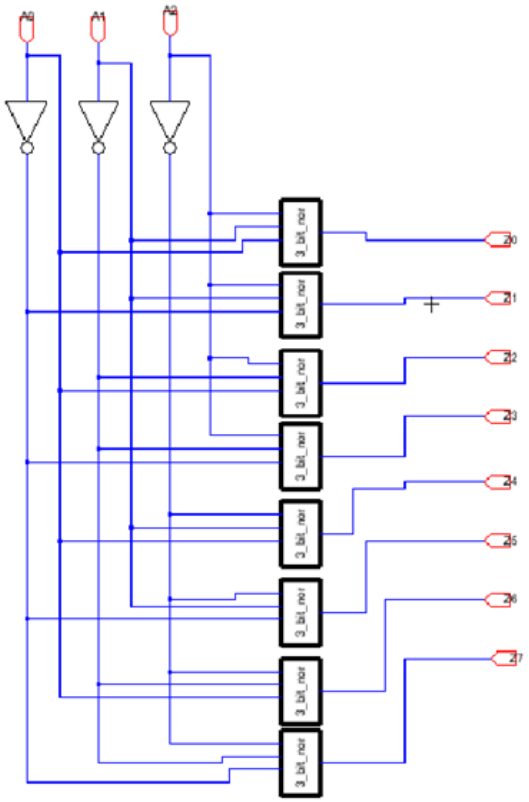

Figure 18 :new decoder design

We also trying to minimize the area and cost based on layout designs , by finding the best design, it reduces the distance between the materials .

IV. SIMULATION AND RESULTS

A. Invertor Simulation

An inverter is a fundamental digital electronic circuit that performs the logical operation of inversion. It takes an input signal and produces the complement of that signal at its output. In other words, if the input is high, the output will be low, and if the input is low, the output will be high. The following figure show the correct simulation of invertor.

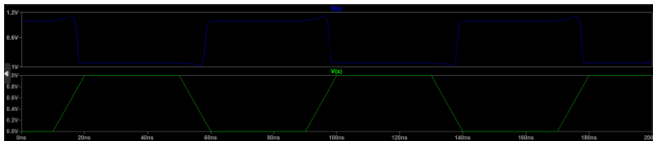

Figure 19: Invertor simulation

B. 9T SRAM Simulation

9T SRAM has two signals (WL , RD) that control it , when WL is high the value of LB will save on it in Q , in this way we can write and refresh the value that saved in memory , when RD is high that mean the SRAM will isolate the value of Q from any change whenever LB change or not , stability and integrity of the stored data , this way

increased the stability of SRAM. The following figure show the simulation of 9T SRAM.

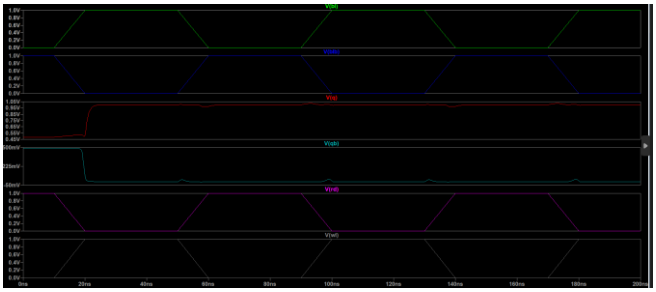

Figure 20: 9T SRAM simulation

C. 1-Bit CAM Simulation

A 1-bit Content-Addressable Memory (CAM) is a memory unit that will return 0 if the 1-bit input of it not equal the bit that stored in SRAM and it will return 1 if 1-bit input of it equal the data that stored in SRAM . The following figure show the simulation of 1-Bit CAM .

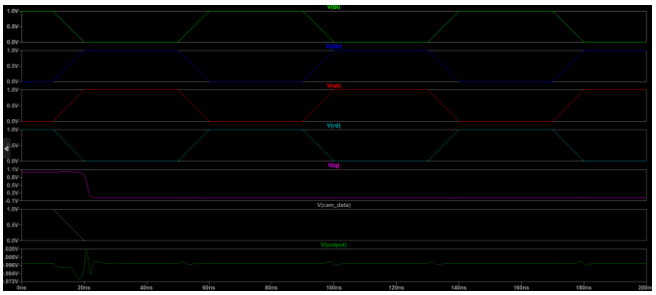

Figure 21: 1-Bit CAM simulation(input equal SRAM data)

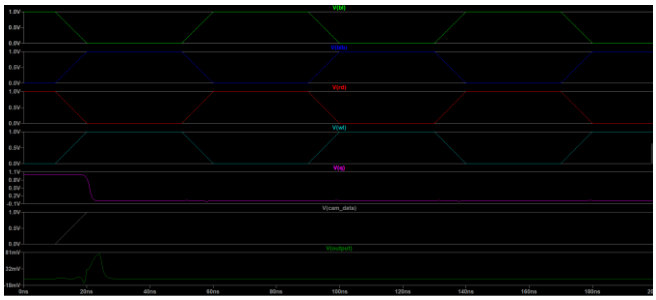

Figure 22: 1-Bit CAM simulation(input not equal SRAM data)

D. 3-Bit NOR Simulation

A 3-bit NOR gate is a logic circuit that takes three input signals and produces a single output based on the NOR (logical NOT OR) operation. The output of a 3-bit NOR gate will be low (logic 0) if any of the input signals are high (logic 1), and it will be high (logic 1) only if all three input signals are low (logic 0). The following figure show the simulation of 3-Bit NOR gate .

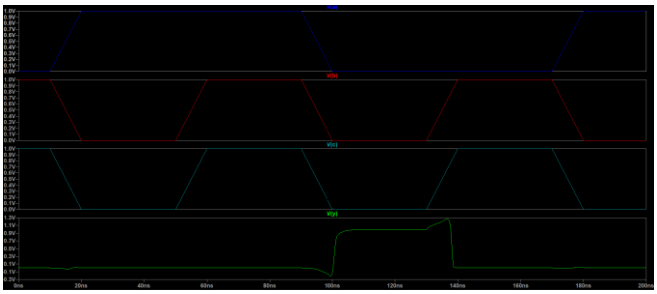

Figure 23: 3-Bit NOR simulation

E. 3x8 Decoder Simulation

A 3x8 decoder is a combinational logic circuit that takes a 3-bit input and generates 8 outputs. Each input combination corresponds to a unique output line and other lines will be zero . For example, when A2A1A0 is 000, the output Z0 is asserted (logic 1), and all other output lines are de-asserted (logic 0). Similarly, for each input combination, the corresponding output line is asserted, and all other output lines are de-asserted. The following figure show the simulation of 3x8 decoder for different cases .

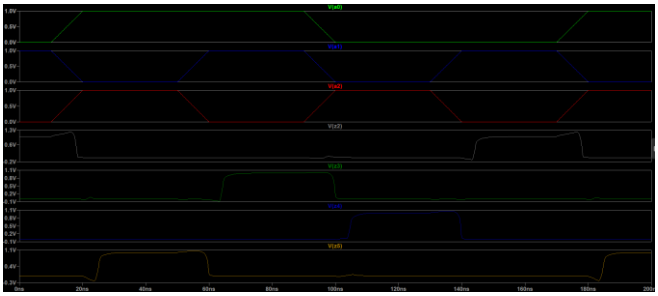

Figure 24: 3x8 decoder simulation

F. 8-Bit NAND Simulation

An 8-bit NAND gate is a logic circuit that takes eight input signals and produces a single output based on the NAND (logical NOT AND) operation. The output of an 8-bit NAND gate will be high (logic 1) unless all eight input signals are high (logic 1), in which case the output will be low (logic 0). The following figure show 8-bit NAND simulation .

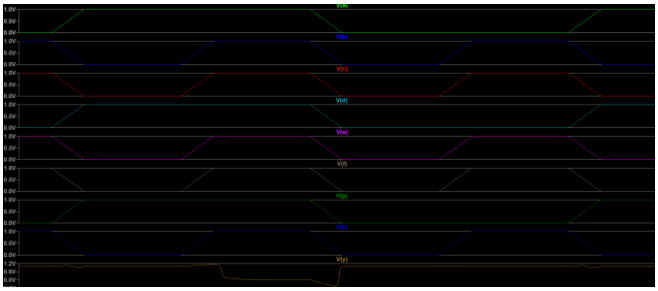

Figure 25 : 8-Bit NAND simulation

G. 8-Bit CAM Simulation

The overall design of Full-Custom 8-bit CAM will return 1 if we write value at specific cell of memory and give the same value for CAM data , that's because at least one cell has the same data , and it will return 0 if we write value on the specific cell of the memory but give different value to CAM data . The following figure show the simulation of 8-Bit CAM .

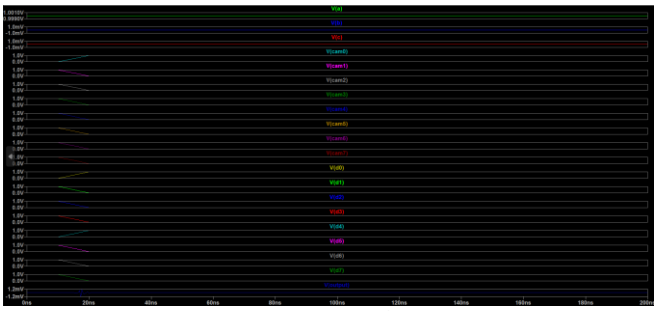

Figure 26: Miss simulation for 8-Bit CAM

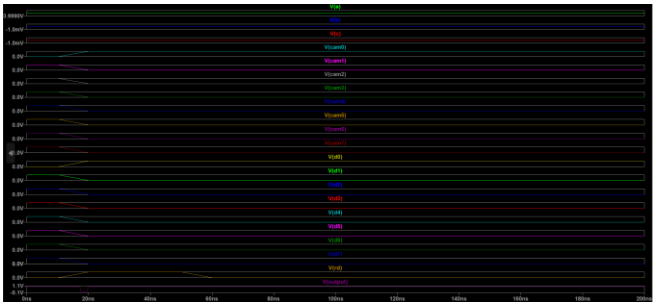

Figure 27: Hit simulation for 8-Bit CAM

V. Conclusion

In this project, the 8-bit CAM cell was designed first, then the 1-bit CAM cell was used to develop 8x8 bit CAM cells, with a decoder to control which row will be used to compare it with the eight bits cam data input. This was done by first designing the 9t SRAM using 9 transistors . After finishing , we switched to the Binary Electric program to design and simulate each component and do the necessary area, power, and delay optimization .

VI. References

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