



Faculty of Engineering & Technology
Electrical & Computer Engineering Department

DIGITAL INTEGRATED CIRCUITS- ENCS3330

Assignment 2

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N-LATCH

Schematic & Layout & Simulation

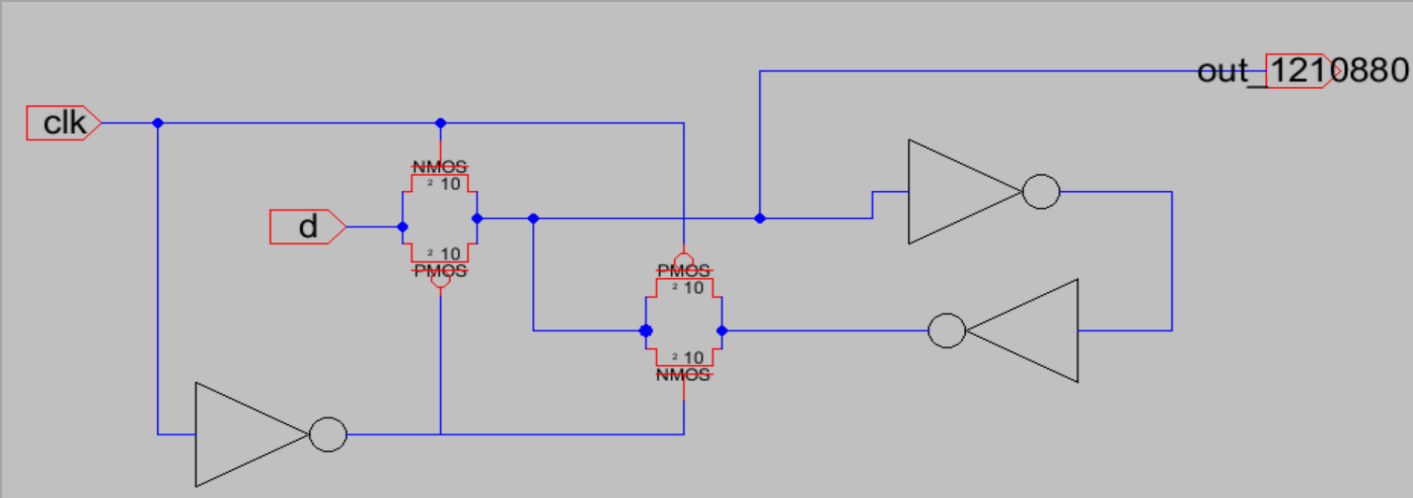


Figure 1: N-LATCH schematic

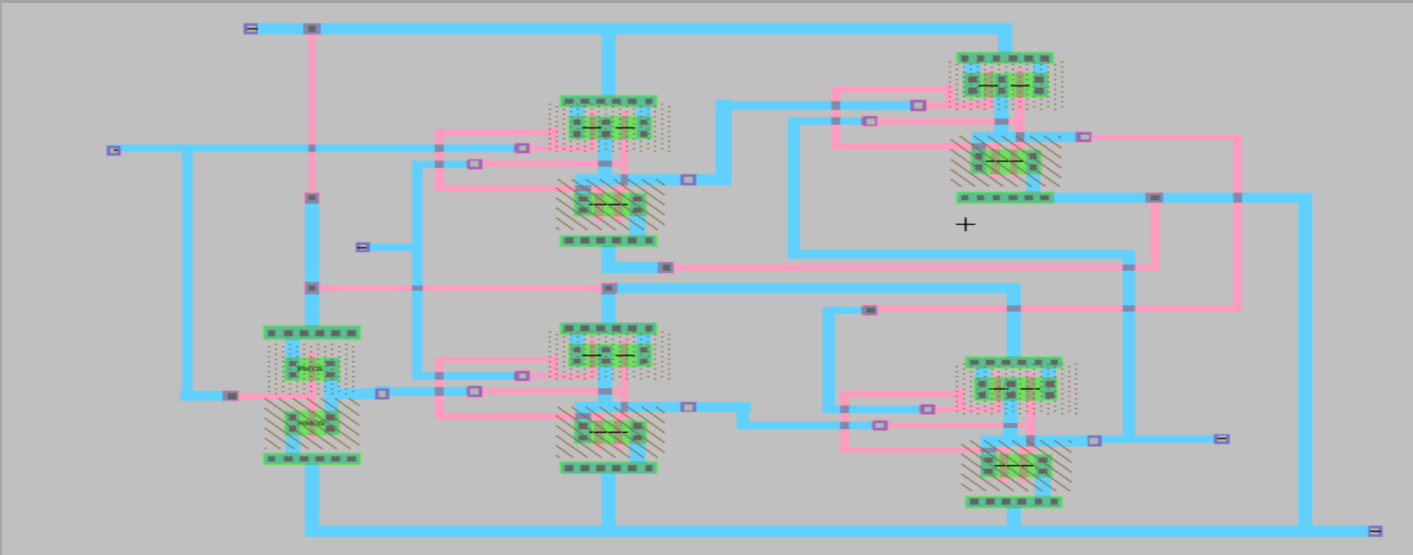


Figure 2: N-LATCH layout

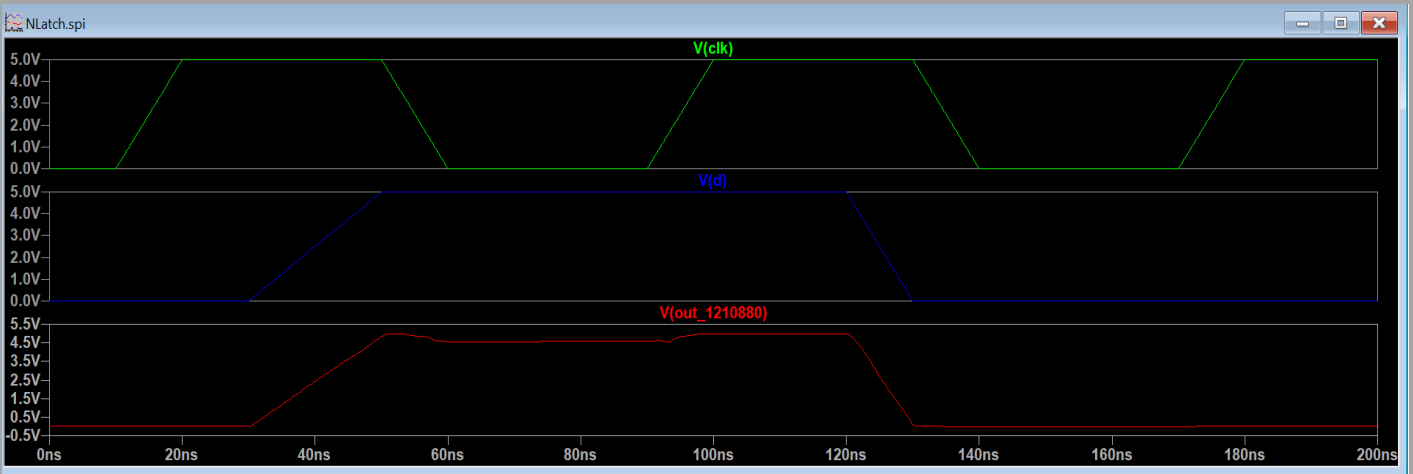


Figure 3: Simulation results for N-LATCH based on schematic

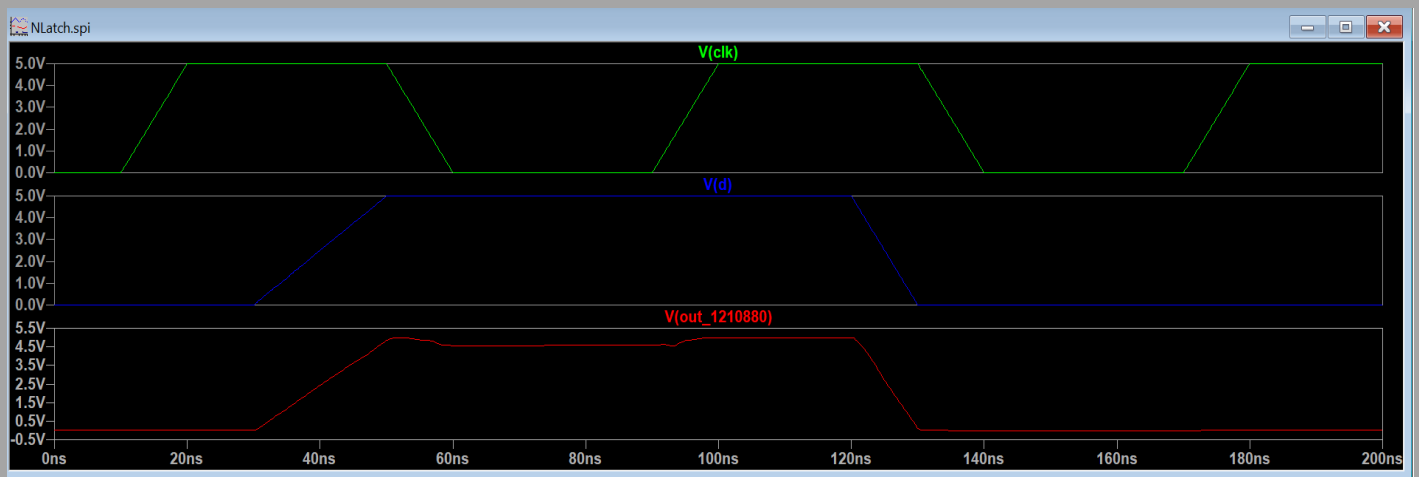


Figure 4: Simulation results for N-LATCH based on layout

P-LATCH

Schematic & Layout & Simulation

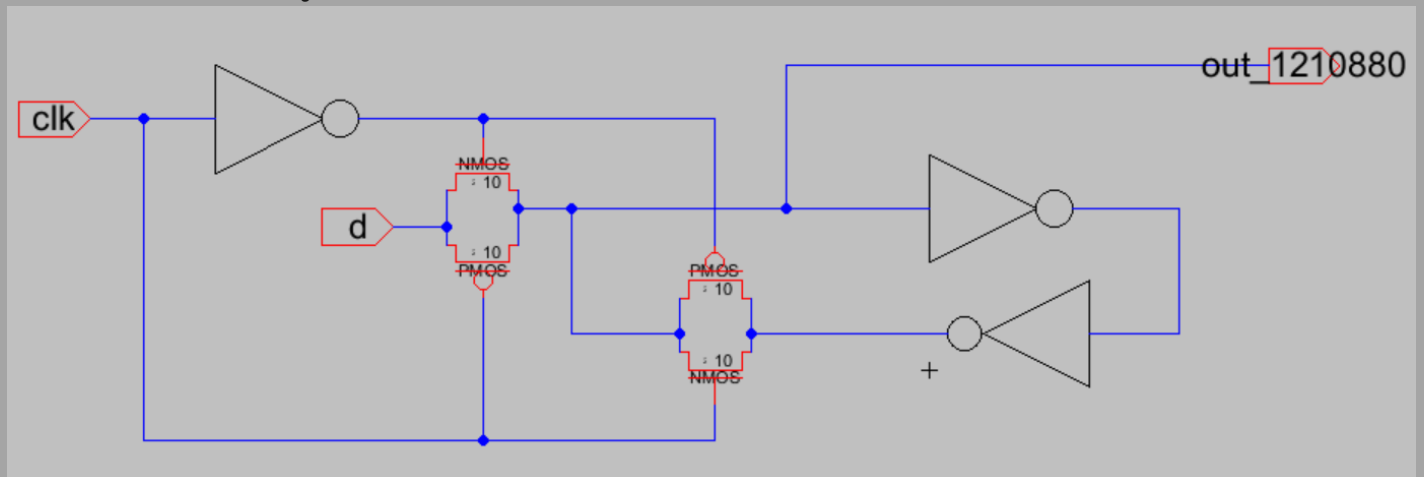


Figure 5: P-LATCH schematic

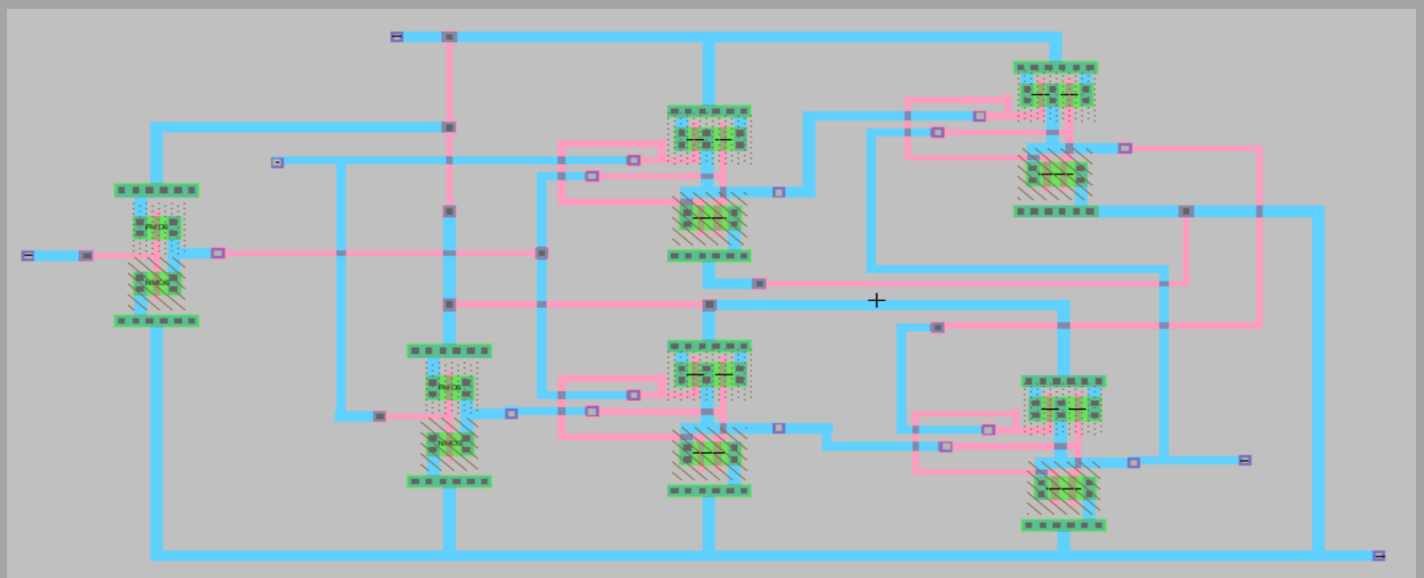


Figure 6: P-LATCH layout

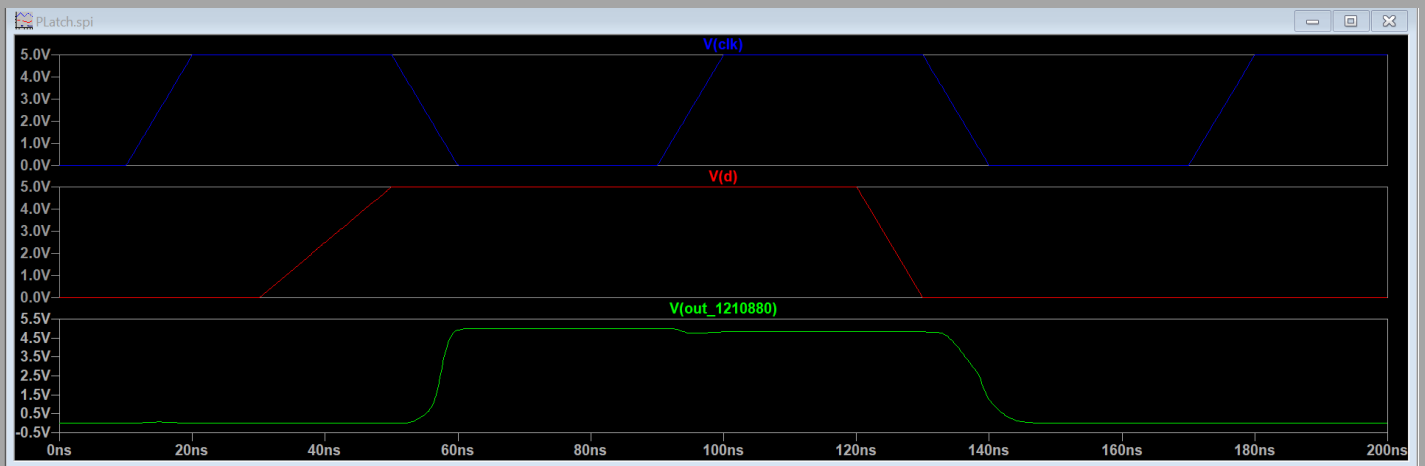


Figure 7: Simulation results for P-LATCH based on schematic

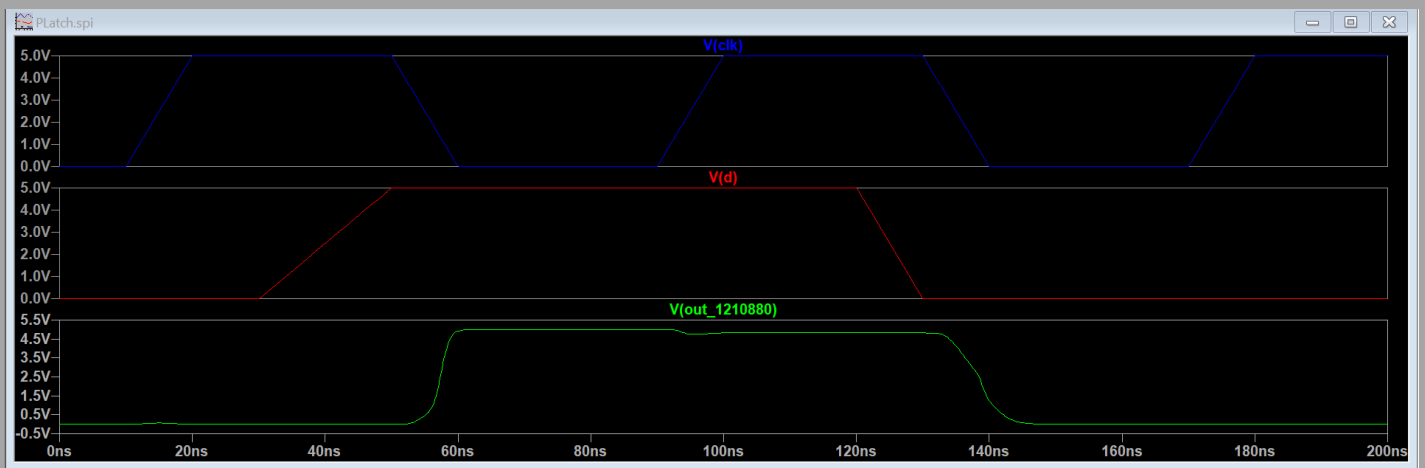


Figure 8: Simulation results for P-LATCH based on layout

Rising edge flip-flop

Schematic & Layout & Simulation

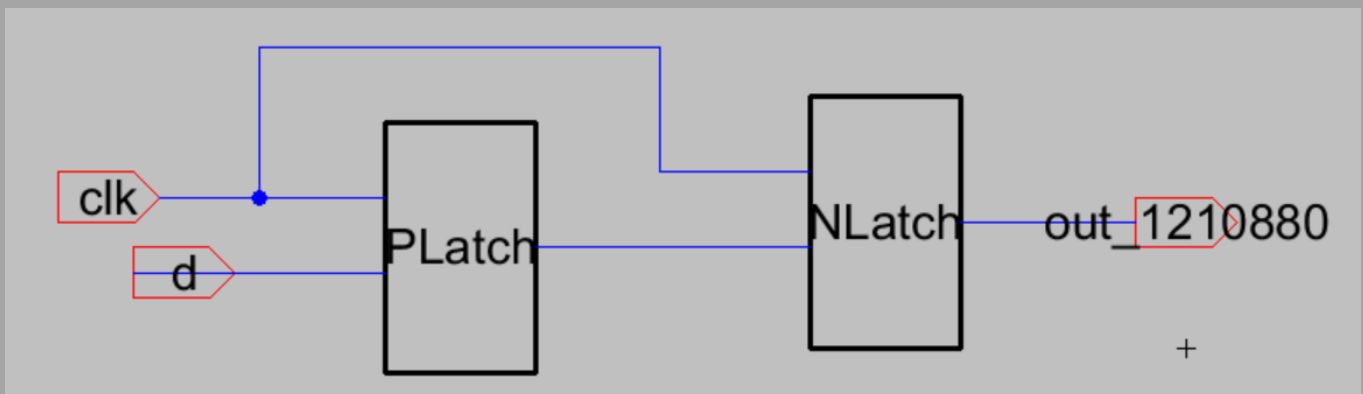


Figure 9: Rising edge flip-flop schematic

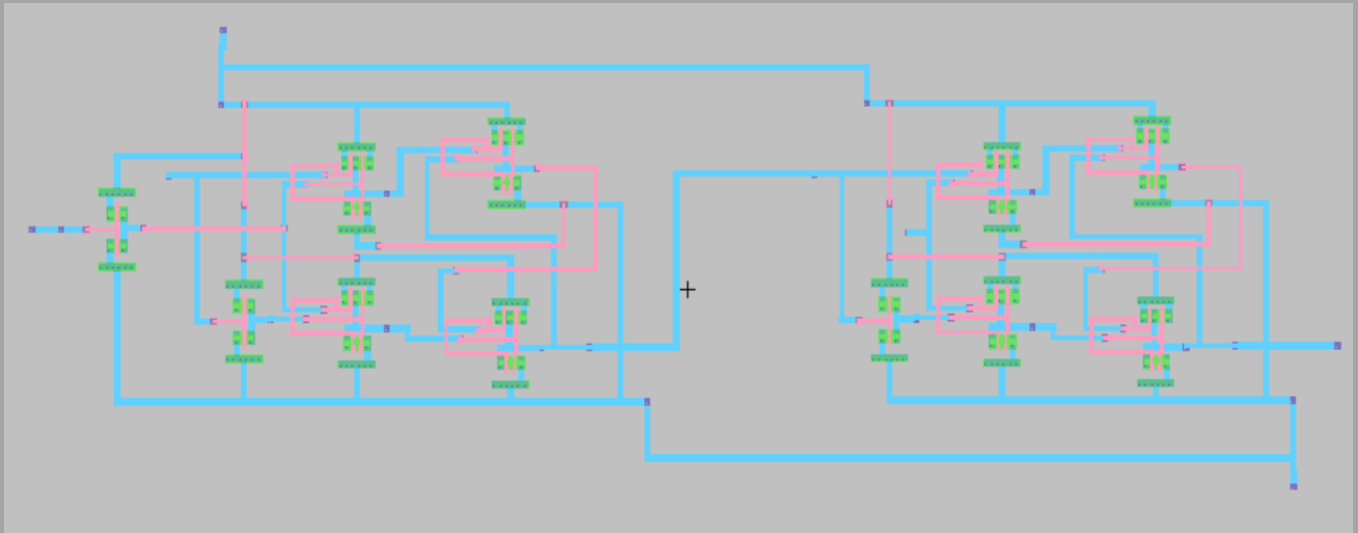


Figure 10: Rising edge flip-flop layout

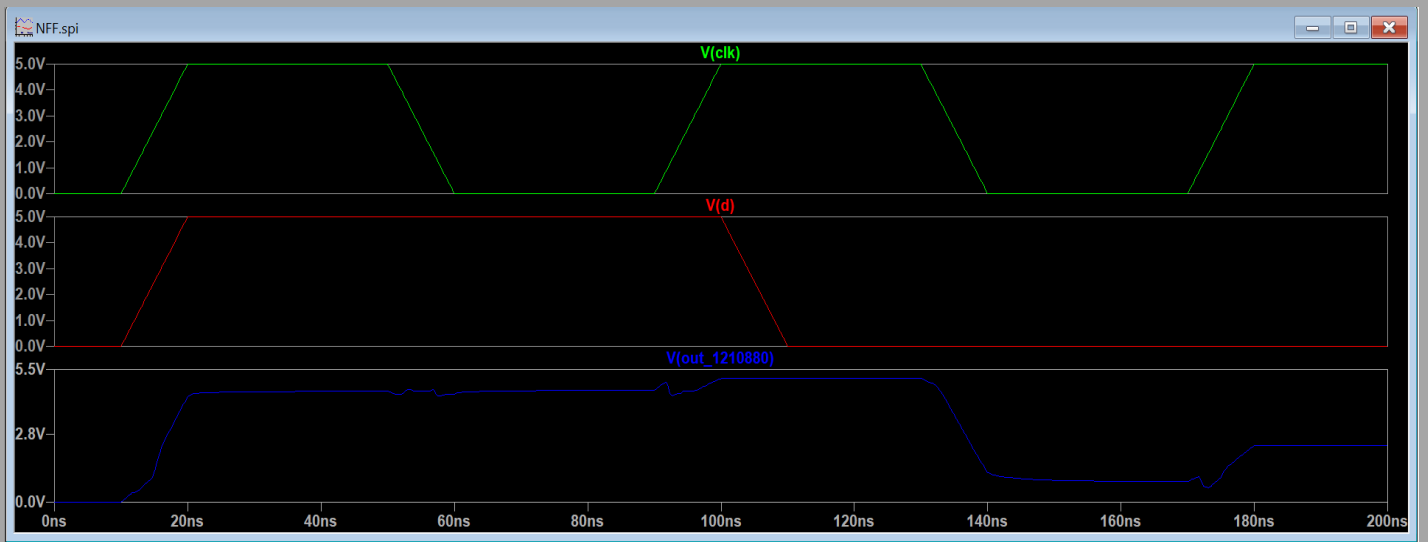


Figure 11: Simulation results for Rising edge flip-flop based on schematic

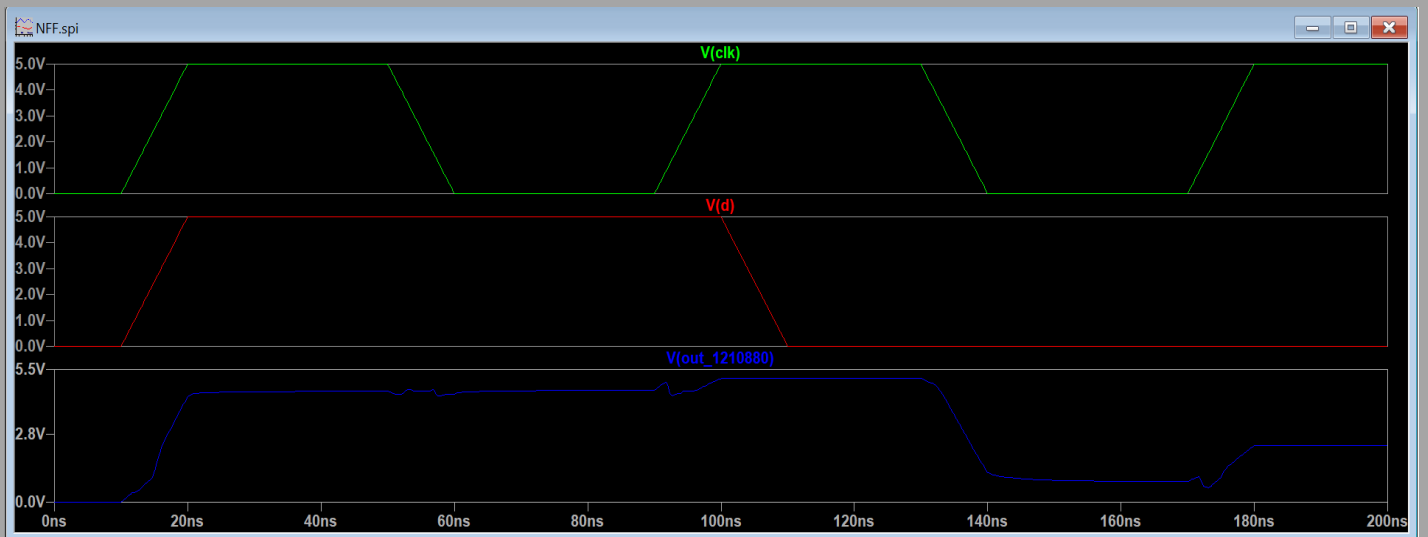


Figure 12: Simulation results for Rising edge flip-flop based on layout

Falling edge flip-flop

Schematic & Layout & Simulation

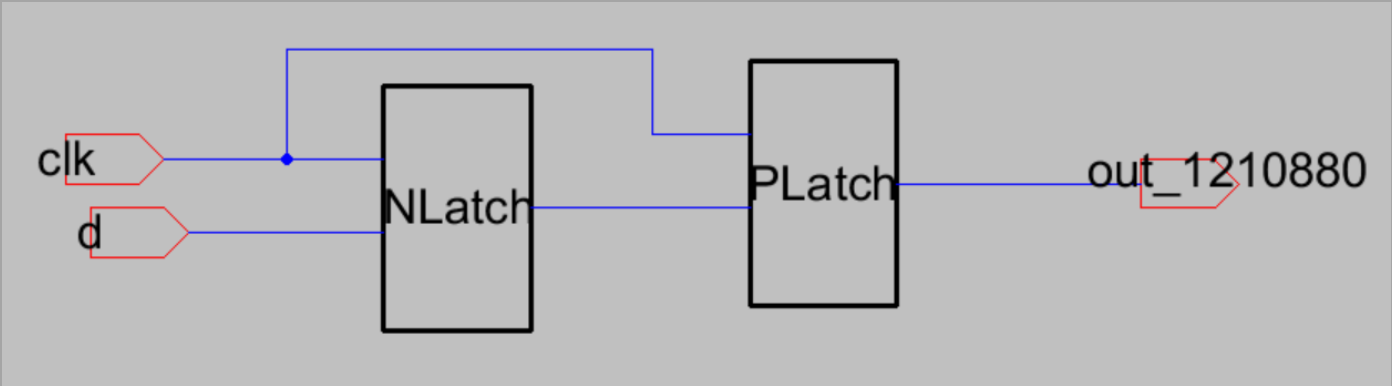


Figure 13: Falling edge flip-flop schematic

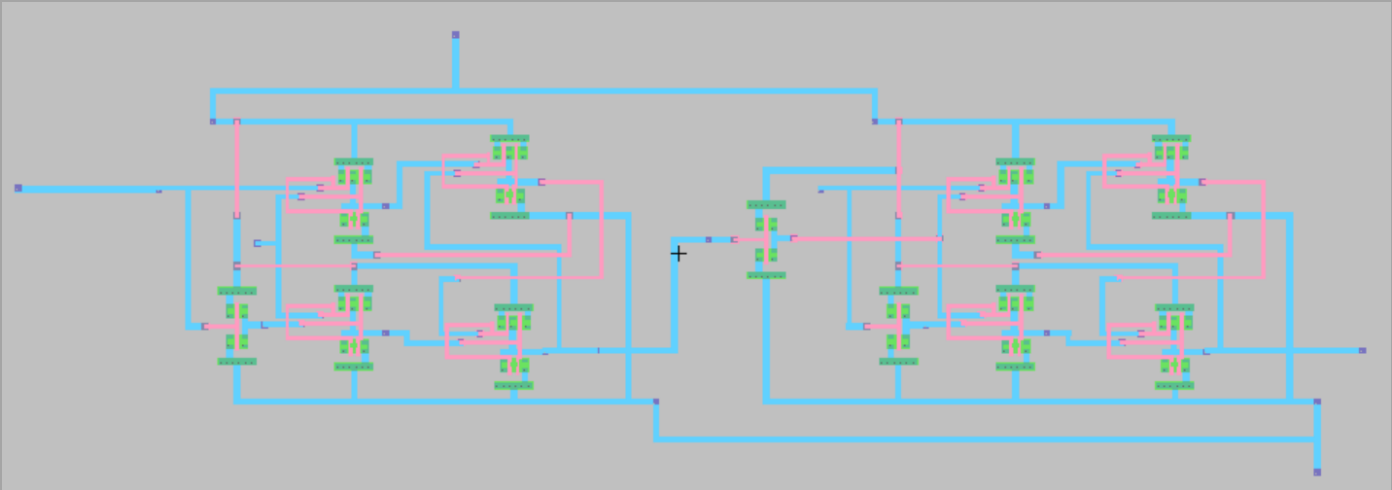


Figure 14: Falling edge flip-flop layout

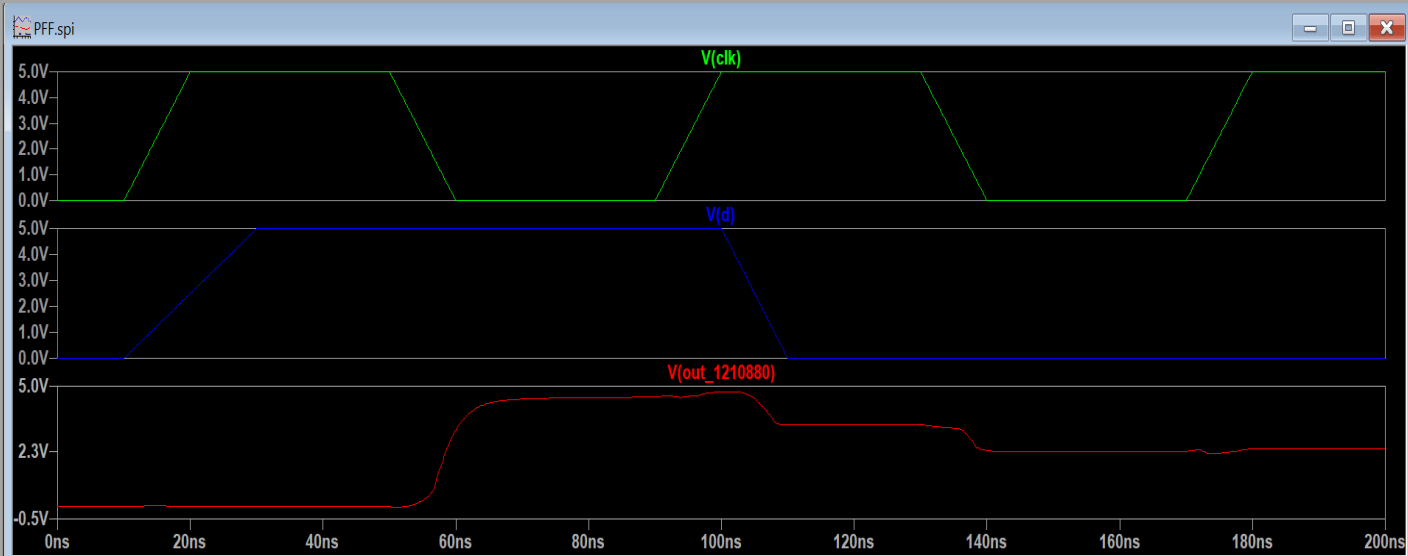


Figure 15: Simulation results for Falling edge flip-flop based on schematic



Figure 16: Simulation results for Falling edge flip-flop based on layout