Faculty of Engineering & Technology Electrical & Computer Engineering Department

DIGITAL INTEGRATED CIRCUITS-ENCS3330

Assignment 1

Schematic and Simulations for logic gate

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Section: Two

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Inverter GATE

Schematic

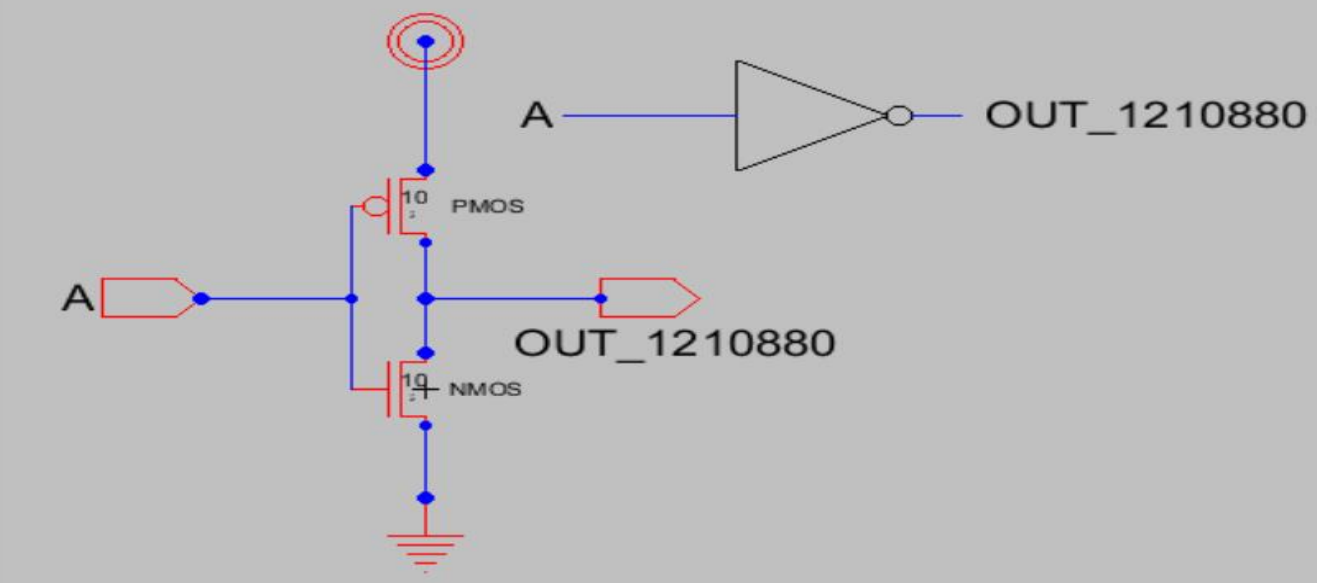

Figure 1: Inverter Schematic and symbole view

SPICE code

```
vdd vdd 0 DC 5
vin A 0 pwl 10n 0 20n 5 50n 5 60n 0
cload OUT_1210880 0 225fF
.measure tran tf_1210880 trig v(OUT_1210880) val=4.5 fall=1 td=8ns targ v(OUT_1210880) val=0.5 fall=1
.measure tran tr_1210880 trig v(OUT_1210880) val=0.5 rais=1 td=50ns targ v(OUT_1210880) val=4.5 rais=1
.tran 0 0.1us
.include C:\Users\USER\OneDrive\Documents\C5_models.txt
```

Figure 2: SPICE Code

Simulation & Results

Simulation based on schematic:

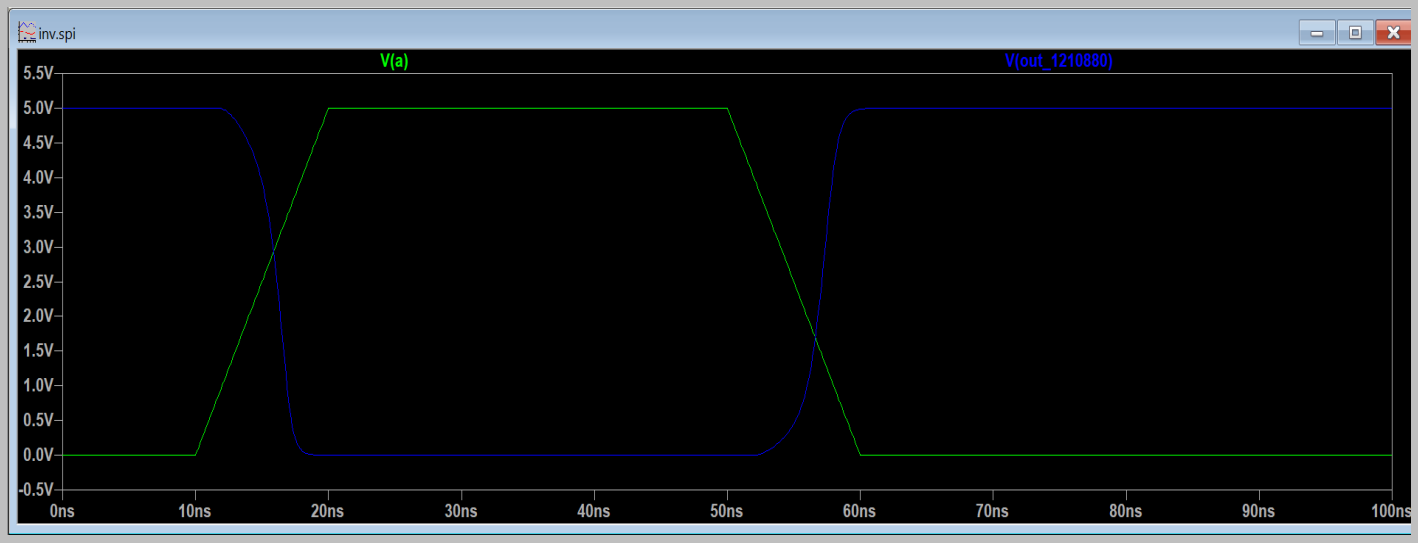

Figure 3: Inverter Simulation based on schematic

Rise and fall time:

- `tf_1210880=3.1964e-009 FROM 1.39976e-008 TO 1.7194e-008`
- `tr_1210880=-3.1964e-009 FROM 1.7194e-008 TO 1.39976e-008`

Simulation based on symbole:

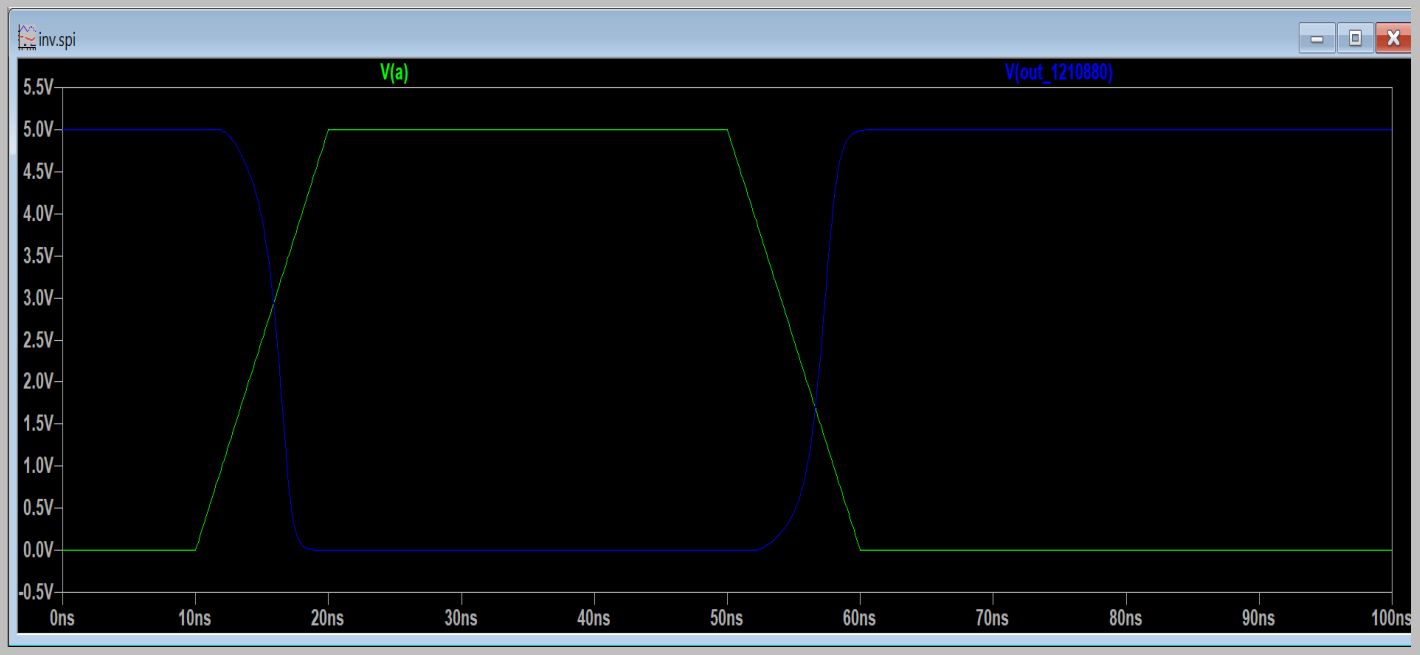

Figure 4: Inverter Simulation based on symbole

NAND GATE – 2 inputs

Schematic

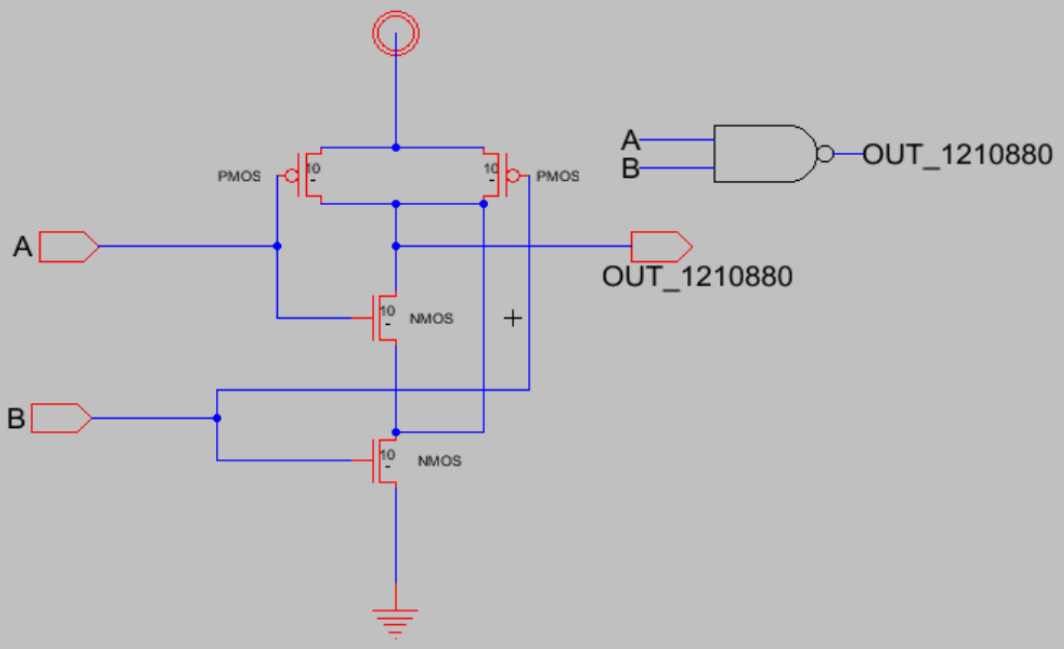

Figure 5: NAND Schematic and symbole view

SPICE code

```
vdd vdd 0 DC 5
vin1 A 0 pwl 10n 0 20n 5 50n 5 60n 0 90n 0 100n 5 130n 5 140n 0 170n 0 180n 5
vin2 B 0 pwl 10n 0 20n  5 100n 5 110n 0
cload OUT_1210880 0 225fF
.measure tran tf_1210880 trig v(OUT_1210880) val=4.5 fall=1 td=4ns targ v(OUT_1210880) val=0.5 fall=1
.measure tran tr_1210880 trig v(OUT_1210880) val=0.5 rais=1 td=4ns targ v(OUT_1210880) val=4.5 rais=1
.tran 200n
.include C:\Users\USER\OneDrive\Documents\C5_models.txt
```

Figure 6: SPICE Code

Simulation & Results

Simulation based on schematic:

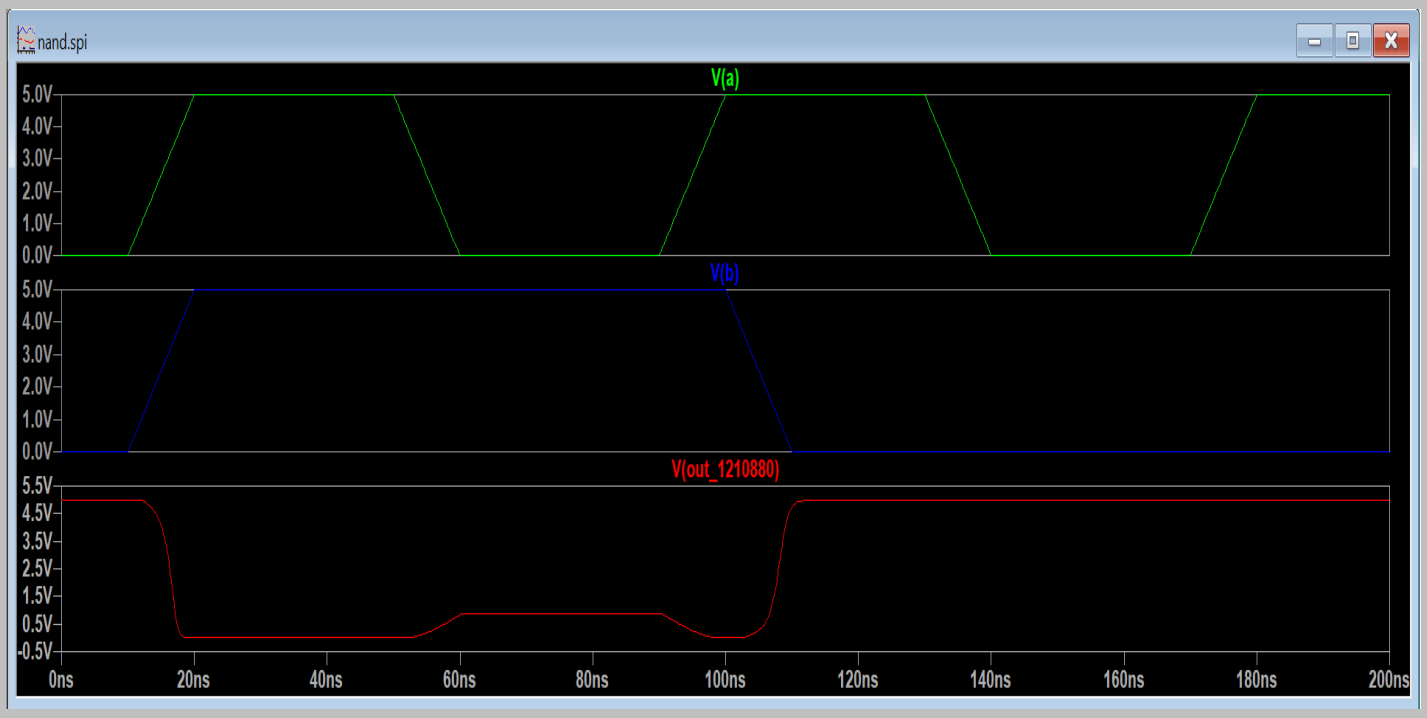

Figure 7: NAND Simulation based on schematic

Rise and fall time:

```
tf_1210880=3.1961e-009 FROM 1.4188e-008 TO 1.73841e-008
tr_1210880=-3.1961e-009 FROM 1.73841e-008 TO 1.4188e-008
```

Simulation based on symbole:

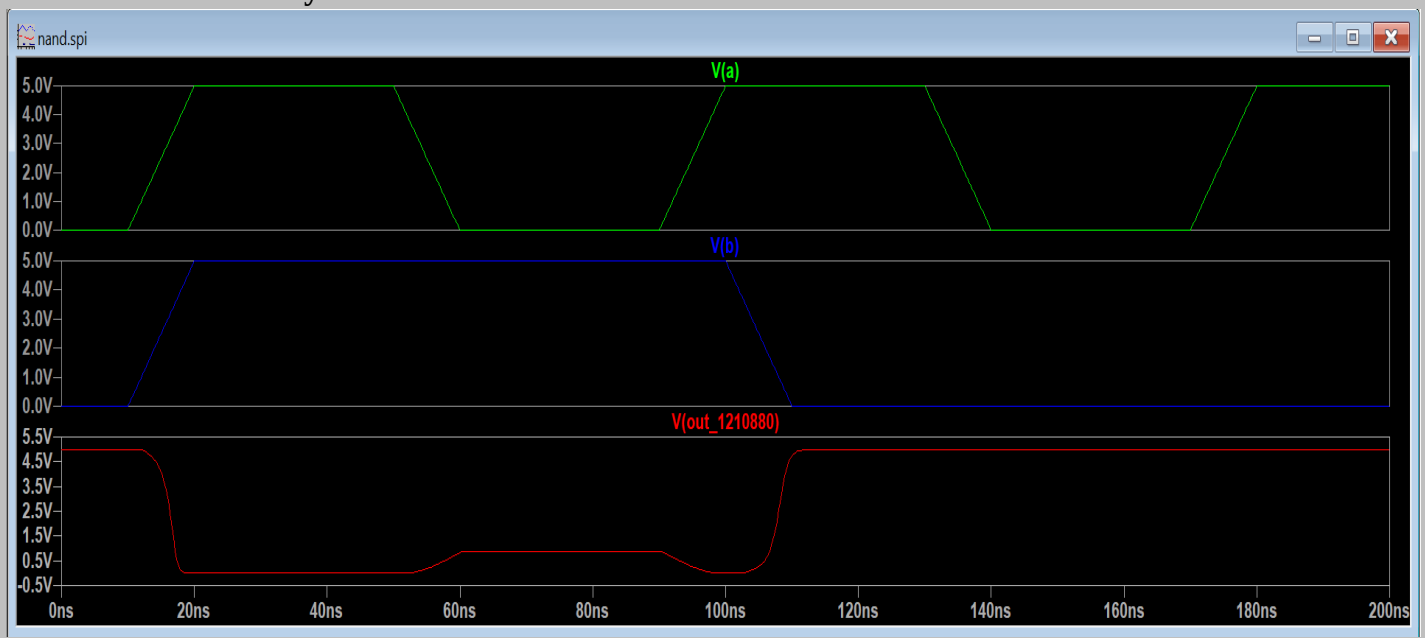

Figure 8:NAND Simulation based on symbole

NOR GATE – 2 inputs

Schematic

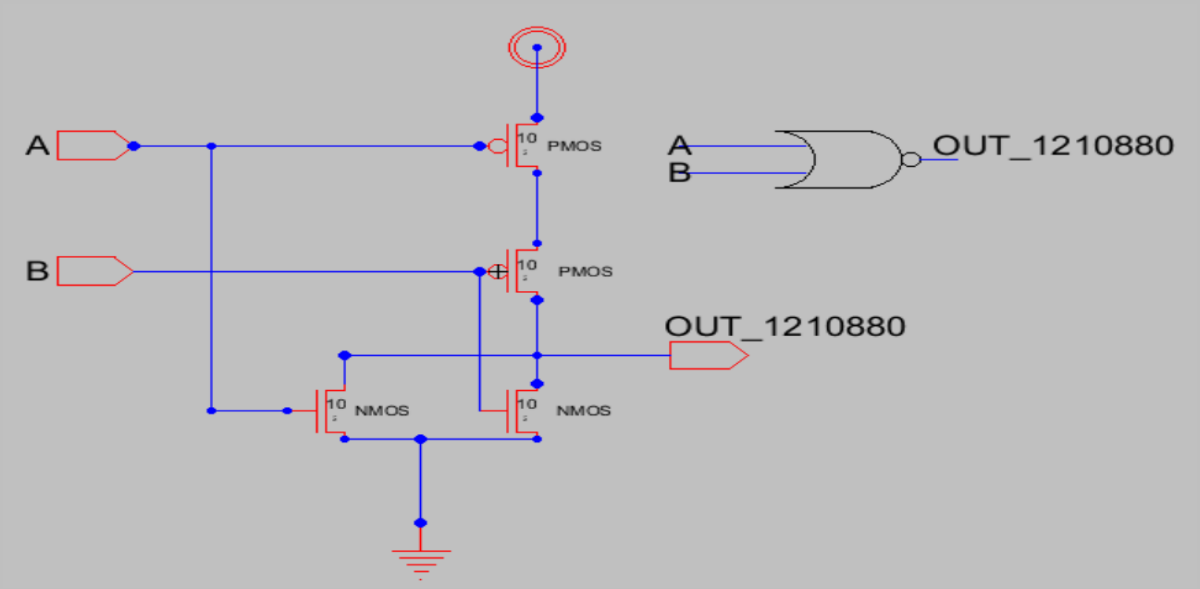

Figure 9: NOR Schematic and symbole view

SPICE code

```
vdd vdd 0 DC 5
vin1 A 0 pwl 10n 5 30n 5 40n 0 60n 0 70n 5 90n 5 100n 0 120n 0 130n 5 150n 5 160n 0 180n 0
vin2 B 0 pwl 10n 5 60n 5 70n 0 120n 0 130n 5 180n 5 190n 0 240n 0
cload OUT_1210880 0 225fF
.measure tran tf_1210880 trig v(OUT_1210880) val=4.5 fall=1 td=8ns targ v(OUT_1210880) val=0.5 fall=1
.measure tran tr_1210880  trig v(OUT_1210880) val=0.5 rais=1 td=50ns targ v(OUT_1210880) val=4.5 rais=1
.tran 200n
.include C:\Users\USER\OneDrive\Documents\C5_models.txt
```

Figure 10: SPICE code

Simulation & Results

Simulation based on schematic:

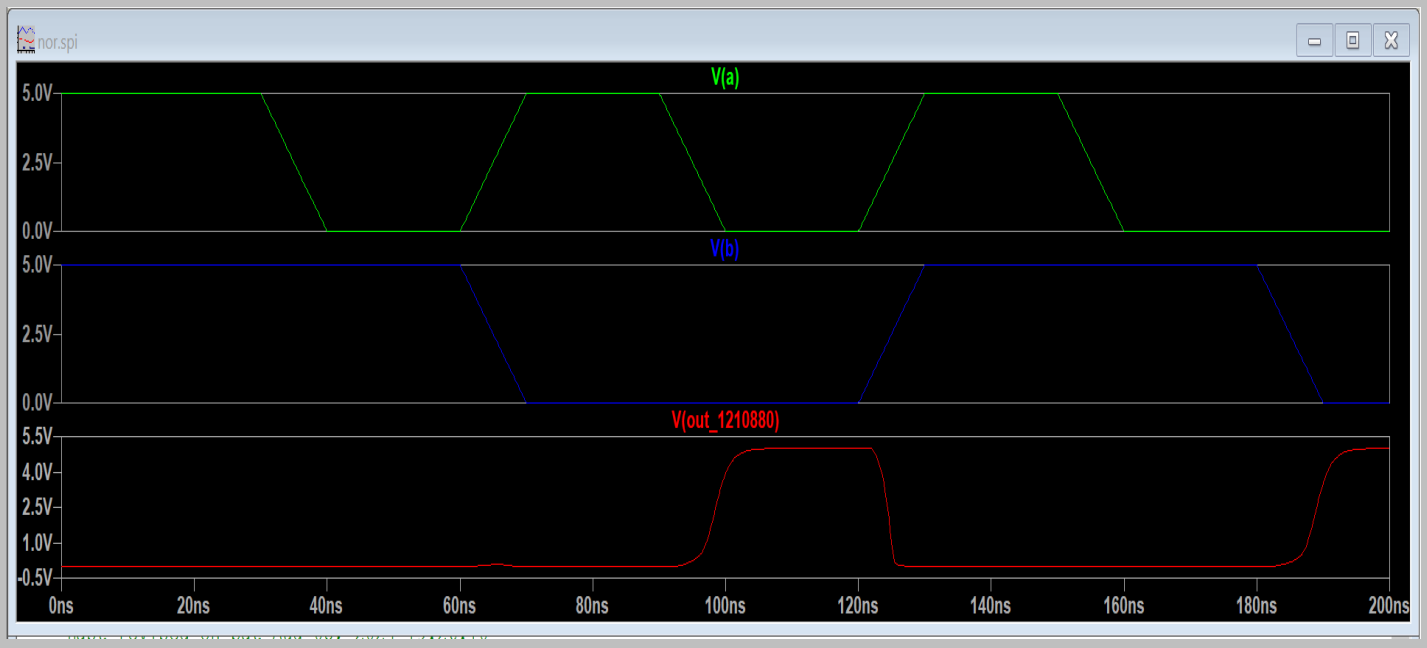

Figure 11: NOR Simulation based on schematic

Rise and fall time:

- `tf_1210880=2.2935e-009 FROM 1.22946e-007 TO 1.2524e-007`
- `tr_1210880=4.96677e-009 FROM 9.61779e-008 TO 1.01145e-007`

Simulation based on symbole:

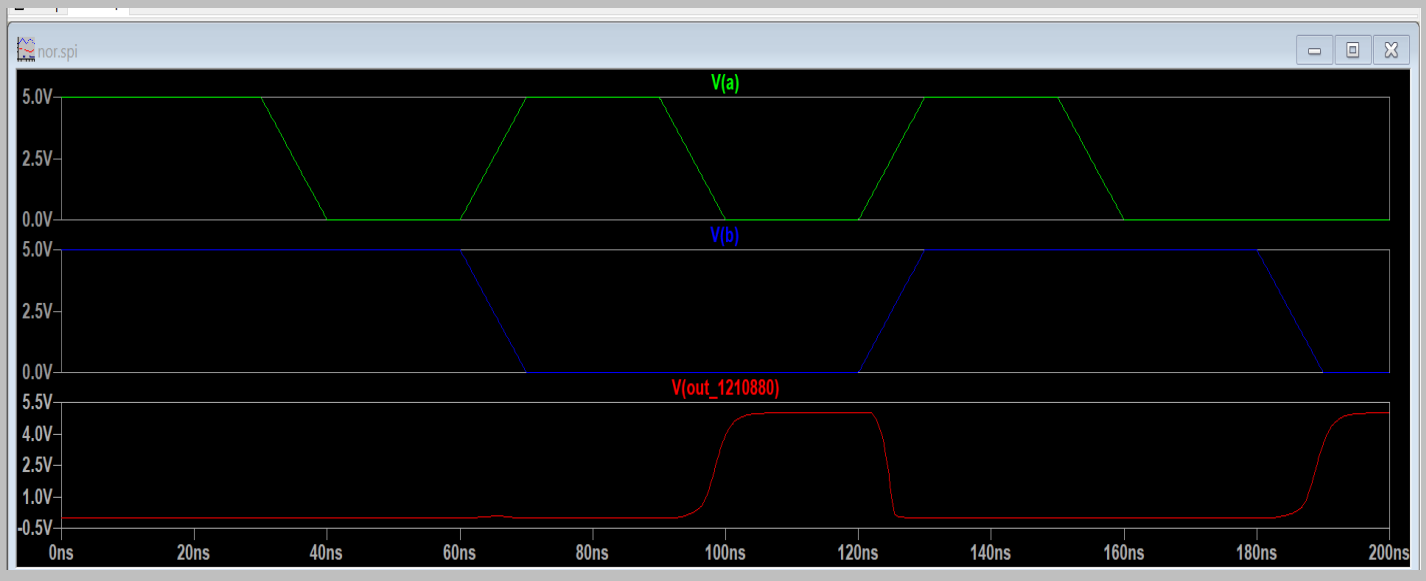

Figure 12: NOR Simulation based on symbole