Low Power Comparator Logic circuit

Maha eyad -1211905,Baraa Nasar– 1210880, Fatima zahran - 1212141

Electrical & Computer Engineering Department, Birzeit University
Ramallah, Palestine
1211905@student.birzeit.edu

Abstract—
The most important factors in VLSI (very large scale Integration) design are area, Power consumption and delay. epically for developing adders, and fast circuits. In this paper will investigates different circuits that output would be faster than expected. these Circuits are praised for it Their simplicity, high regularity, low power c consumption, 16-bit magnitude Comparator is important in DSP (digital signal processing) systems, microprocessors, because of its specifies fast and effective comparison is crucial, the main objective of this paper is to show solution for VLSI design using full adders.
Keywords: Power delay product (PDP), low power (LP), high performance (HP), full adder (FA24T), N-10T, and bridge are all examples of magnitude comparisons.

I. Introduction

it is a combinational circuit that compares two numbers to discover if the first number is less than or larger than or equal to the other number. logically it takes two inputs to give three outputs if the inputs were x, y the outputs should be x>y, x<y, x=y. [1]

As Moore's law, to the number of the transistors integrated in a chip double once in every 18 months. the transistors are very special invention it has some sensitivity like no Power Consumption, high reliability, Small size, so we are going to use it in our project.

This paper will focus more on 16-bit Comparator by connecting. 1- bit Comparators for to do the function, also an 8- bit comparator is implemented using 4-bits comparator.

Figure 1:N – bit Comparator

II. Related Work 'Exiting work'

In our design and implementation of the 16-bit comparator logic circuit, we've started with small comparators until we reach the 16-bit comparator, such as the 4-bit and 8-bit versions. The design was inspired by the work showed in the paper "VLSI Design of Low Power 4 Bit Magnitude Comparator Using GDI Technique" by Sujata S. Chiwande et al. The fundamental concept in this approach is to minimize power consumption by reducing the number of transistors, particularly through efficient designs of basic logic gates like XNOR, NAND, and NOR.

III. GDI Technique

it's a combinatorial circuit to reduce the power consumption, to propagate the delay also to low the complexity of the logic design, comparing to the CMOS it's better because it reduces the transistors [2]

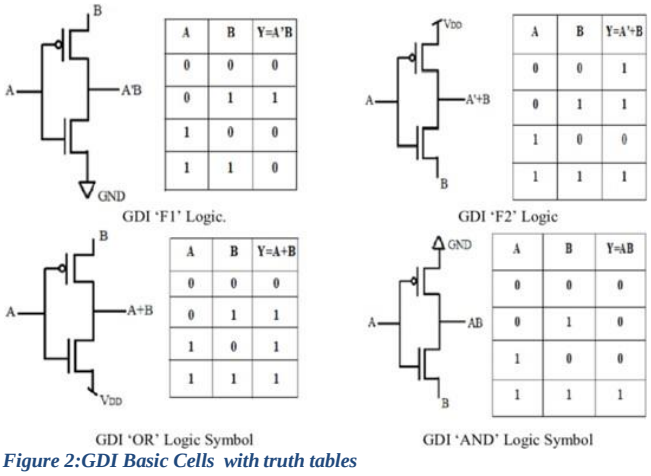


Figure 2:GDI Basic Cells with truth tables

IV. 1-BIT COMPARATOR

A comparator used to compare two inputs each input consists of one bit to give three outputs (less than, greater than, equal to). [3]

A_0	B_0	L	E	G
0	0	0	1	0
0	1	1	0	0
1	0	0	0	1
1	1	0	1	0

Figure 3:1-bit comparator truth table

The logical expressions for each output can be expressed as follows:

A>B: AB'
A<B: A'B
A=B: A'B' + AB

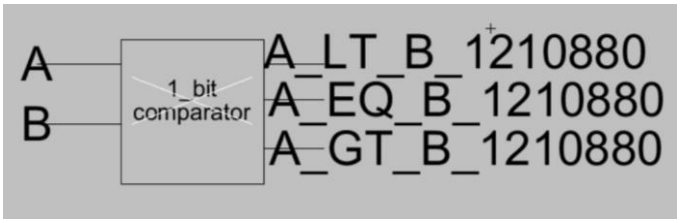


Figure 4:1-bit comparator block diagram

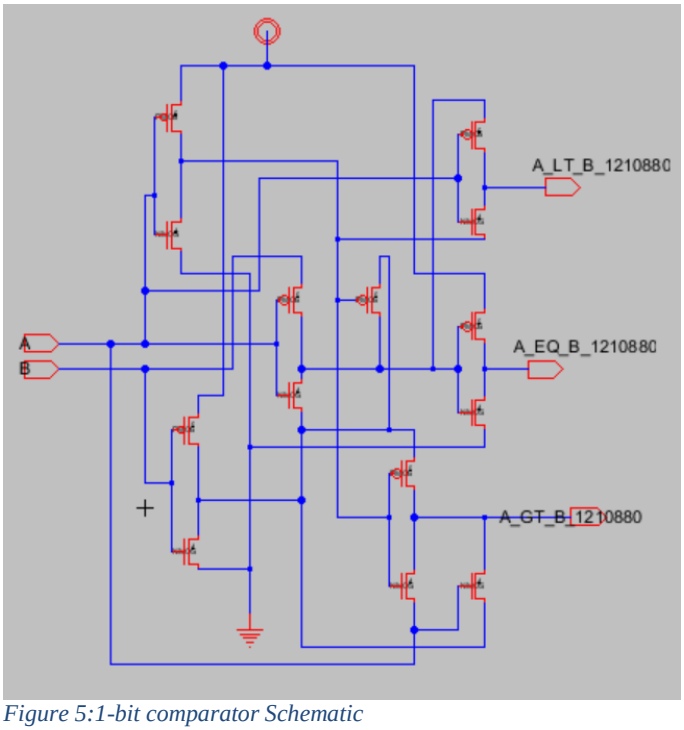


Figure 5:1-bit comparator Schematic

V. 2-BIT COMPARTOR

A 2-bit comparator compares two inputs, each of them consists of two bits it gives equal or greater than or less than the other. [4]

Inputs				Outputs		
A_1	A_0	B_1	B_0	A>B	A=B	A<B
0	0	0	0	0	1	0
0	0	0	1	0	0	1
0	0	1	0	0	0	1
0	0	1	1	0	0	1
0	1	0	0	1	0	0
0	1	0	1	0	1	0
0	1	1	0	0	0	1
0	1	1	1	0	0	1
1	0	0	0	1	0	0
1	0	0	1	1	0	0
1	0	1	0	0	1	0
1	0	1	1	0	0	1
1	1	0	0	1	0	0
1	1	0	1	1	0	0
1	1	1	0	1	0	0
1	1	1	1	0	1	0

Figure 6:2-bit comparator truth table

From the above truth table logical expressions for each output can be expressed as follows:

A > B : $A_1B_1' + A_0B_1'B_0' + A_1A_0B_0'$

A = B : $A_1'A_0'B_1'B_0' + A_1'A_0B_1'B_0 + A_1A_0B_1B_0 + A_1A_0'B_1B_0'$

: $A_1'B_1' (A_0'B_0' + A_0B_0) + A_1B_1 (A_0B_0 + A_0'B_0')$

: $(A_0B_0 + A_0'B_0') (A_1B_1 + A_1'B_1')$

: (A_0 Ex-Nor B_0) (A_1 Ex-Nor B_1)

A < B : $A_1'B_1 + A_0'B_1B_0 + A_1'A0'B0$

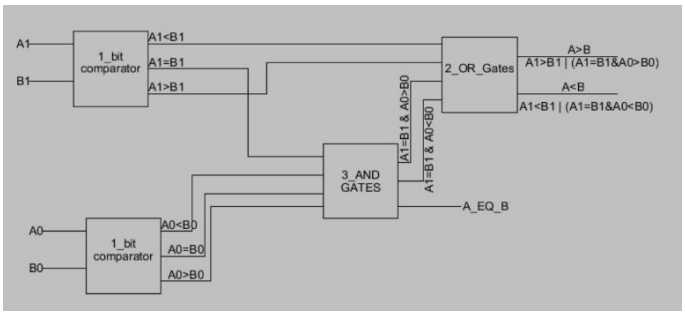
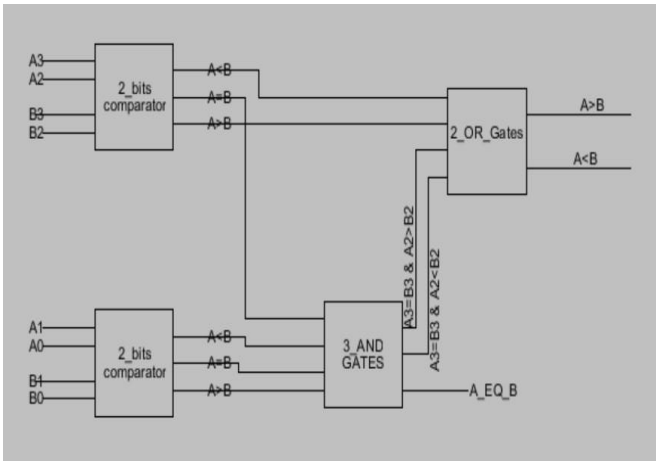


Figure 7:2-bit comparator block diagram

VI. 4-bit comparator

AN 8-BIT comparator compares two inputs using 16 inputs Comparator each of them consists of 8 bits it gives as output Equal or greater than or less than.

Figure 8:4-bit comparator block diagram



VII. 8-BIT COMPARATOR

AN 8-BIT comparator compares two inputs using 16 inputs Comparator each of them consists of 8 bits it gives As output Equal or greater than or less than

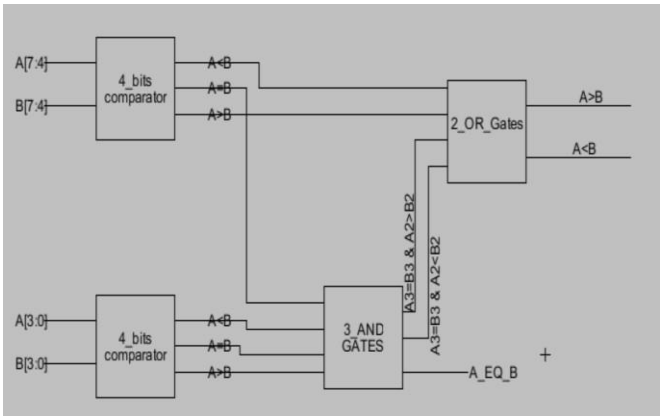


Figure 9: 8-bit comparator block diagram

VIII. OR gate

It is inverted and takes 2 inputs or more to give one input, it's enough is one of the inputs is true to be the output true.

Figure 10:or gate truth table

Input A	Input B	Output
false	false	false
false	true	true
true	false	true
true	true	true

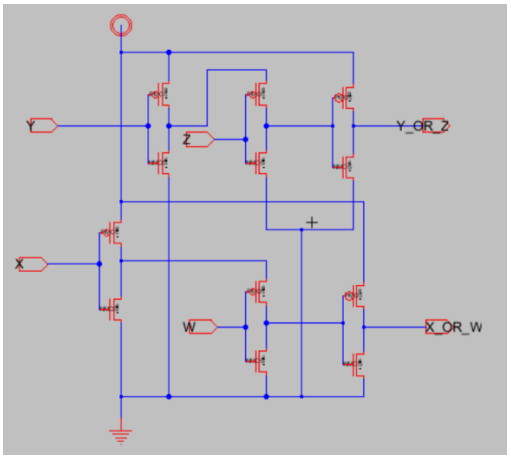


Figure 11:or gate schematic

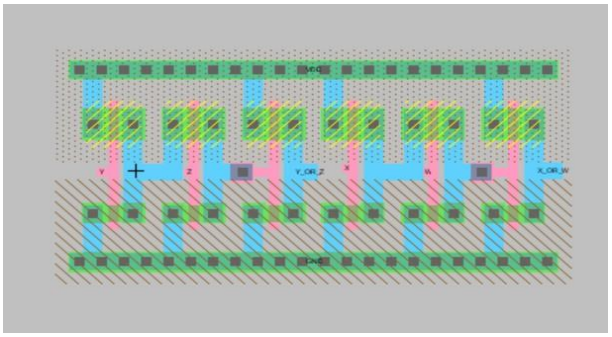


Figure 12:or gate layout

IX. AND GATE

Basic logic gate implement conjunction mathematics logic.

P	Q	$P \wedge Q$
T	T	T
T	F	F
F	T	F
F	F	F

Figure 13:and gate truth table

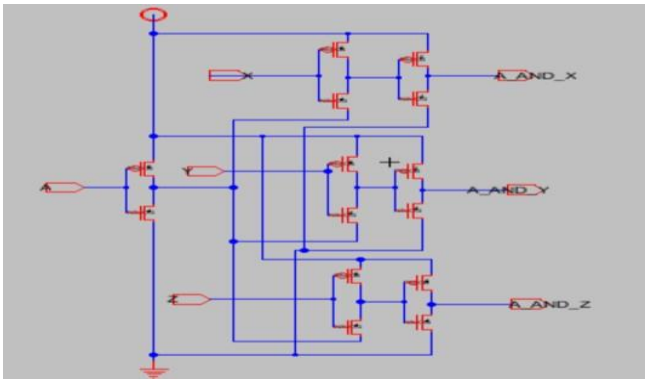


Figure 14:and gate schematic

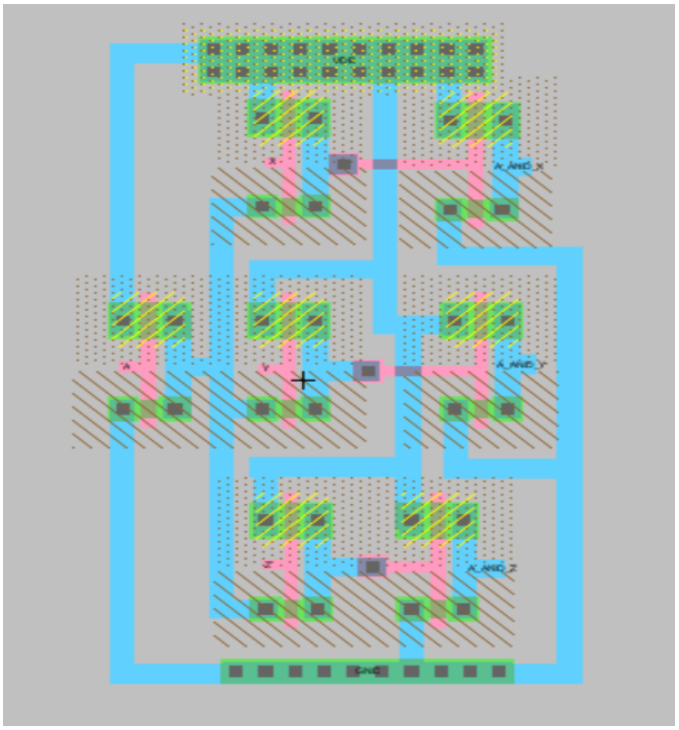


Figure 15:and gate layout

X. PRPOSED DESIGN

in this project we employed 300nm technology, because of the that the width should be 4mm for NMOS, the PMOS width should be 8microm, the length is 2microm for NMOSAND PMOS

to reach the aim from the logic operations in comparing two inputs we build the schematic diagram of the 1-2-4-8-16 bits comparators, the GDI technique here was used to simplify the project so it doesn't use a huge number of transistors, as result for that the power consumption will be less, also it will propagation the delay, the outputs (less than, larger than, equal to) are shown clearly in the design.

the layout here as an idea for the physical implementation on a silicon chip of 1-2-4-8-16 bits comparator, the GDI technique clearly reflected in the compact and efficient transistor arrangement, the design minimizes the area used, which is critical for scaling the comparator to higher bit widths. The reduced area not only conserves silicon space but also decreases parasitic capacitances, thereby improving the overall performance of the comparator.

1. 1- bit comparator

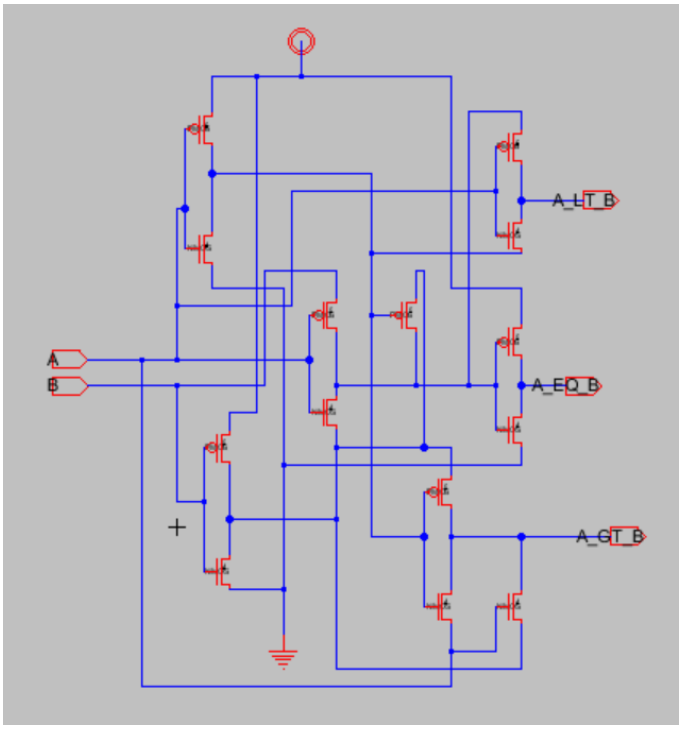


Figure 16:1-bit comparator schematic

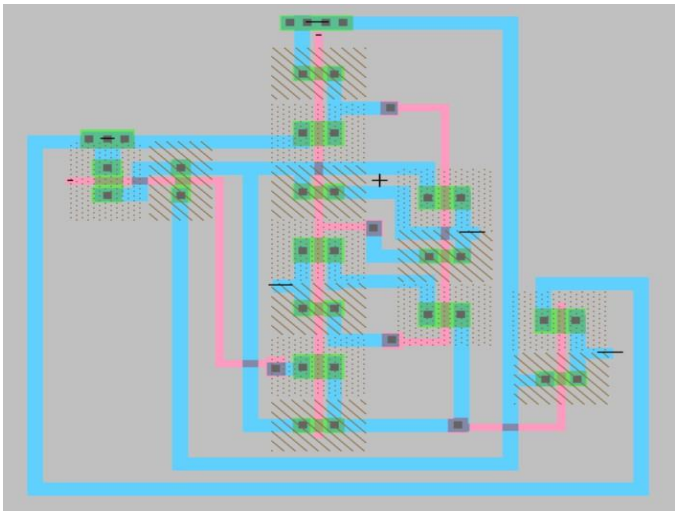


Figure 17:one bit comparator layout

2. 2-bit comparator

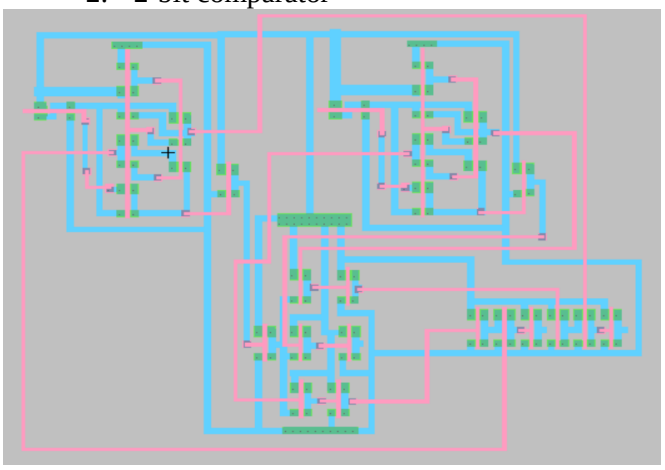


Figure 18:2-bit comparator layout

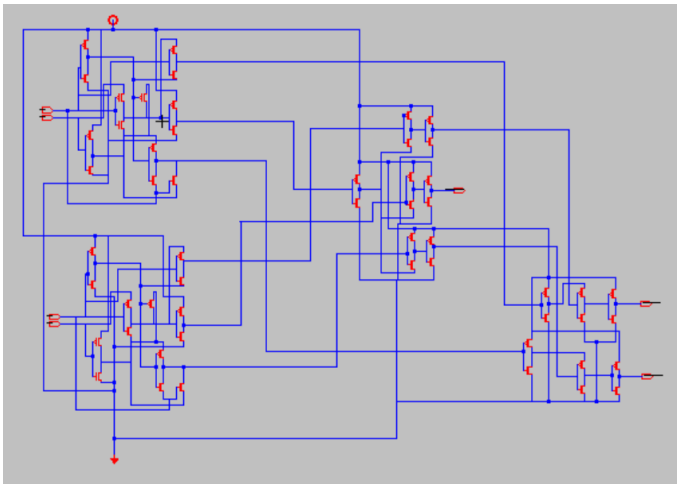


Figure 19:2-bit comparator schematic

3. 4-bit comparator

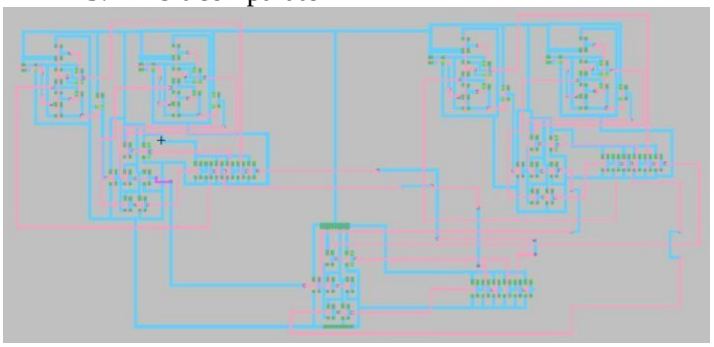


Figure 204-bit comparator layout

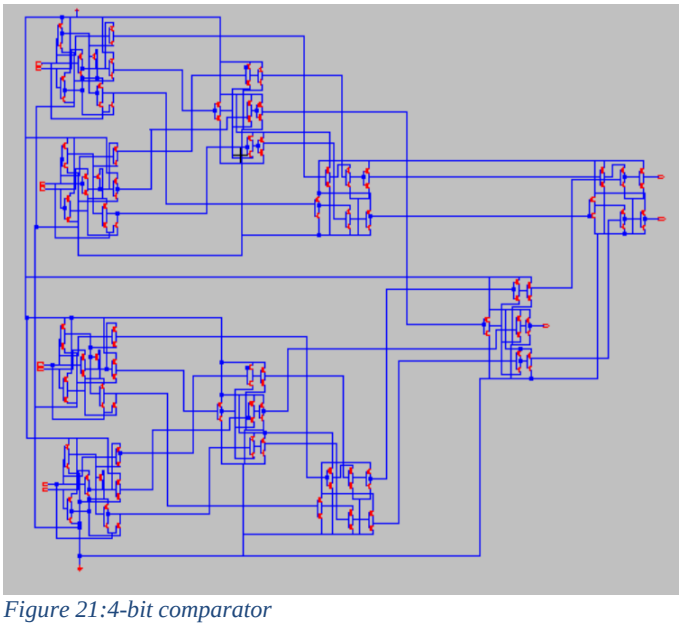


Figure 21:4-bit comparator

4. 8-bit comparator

Figure 22:8-bit comparator layout

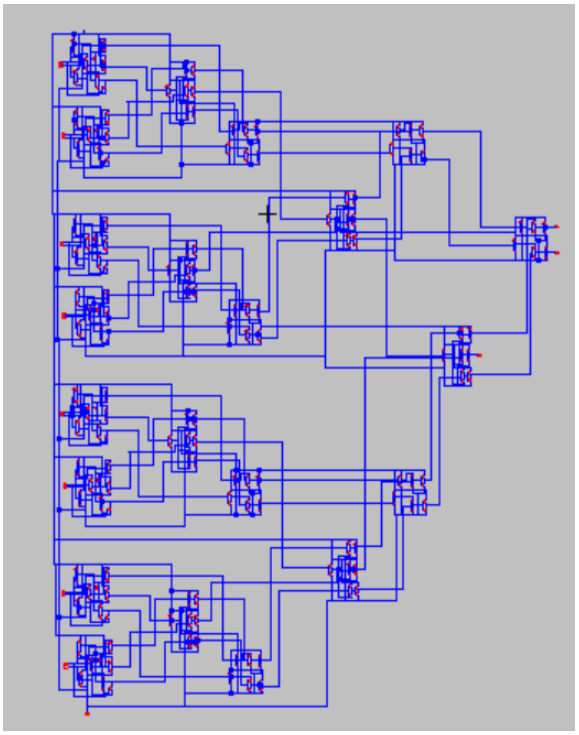


Figure 23:8-bit comparator schematic

C. 4-BIT COMPARATOR

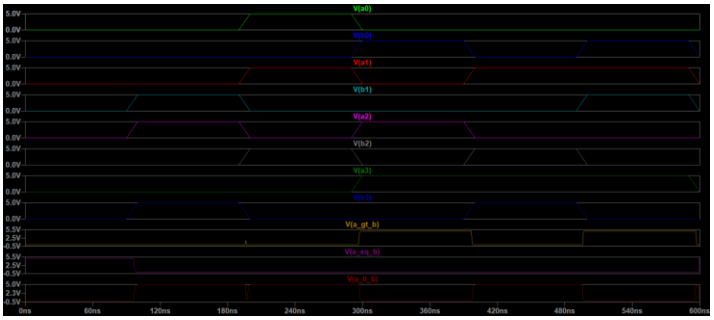


Figure 24:4-bit comparator

5. 16-bit comparator

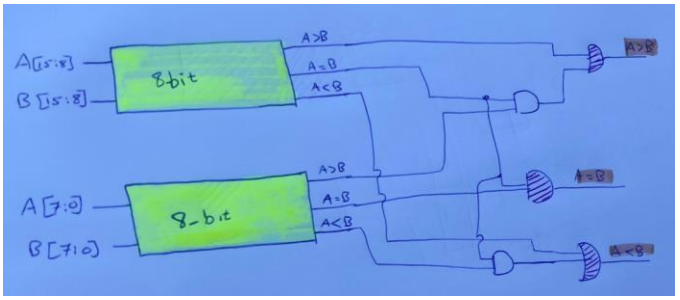


Figure 25:16-bit comparator schematic

We tried many times to build it on the program but we failed at the end, we don't want to waste our time so we draw it on paper, it was not easy for us to build it.

I. TESTING AND SIMULATION

A. 1-BIT COMPARATOR

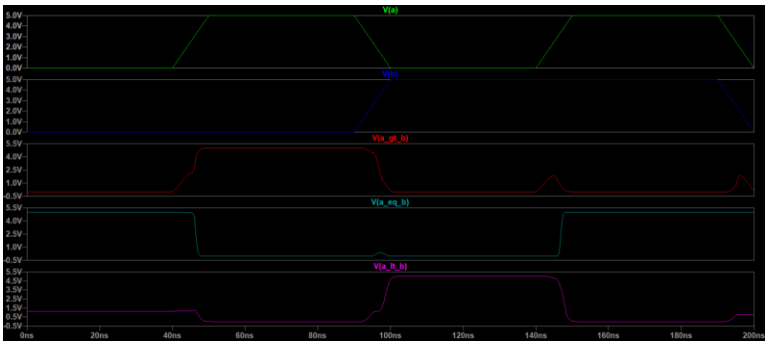


Figure 26:1-bit comparator simulation

B. 2-BIT COMPARATOR

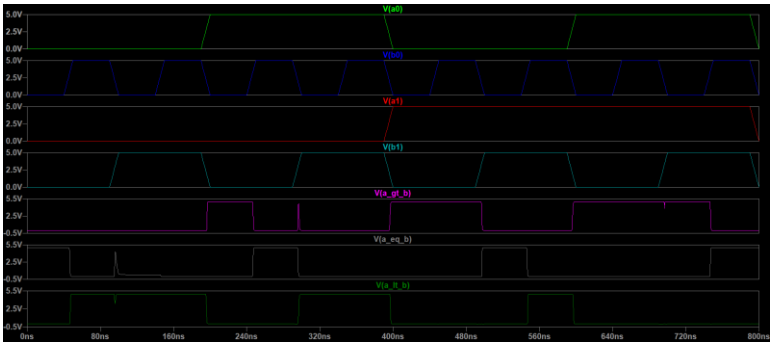


Figure 27:2-BIT comparator simulation

D. 8-Bit Comparator

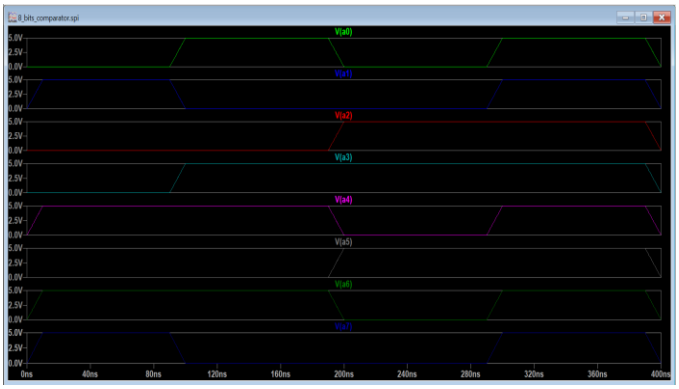


Figure 28:8-bit comparator simulation for input A

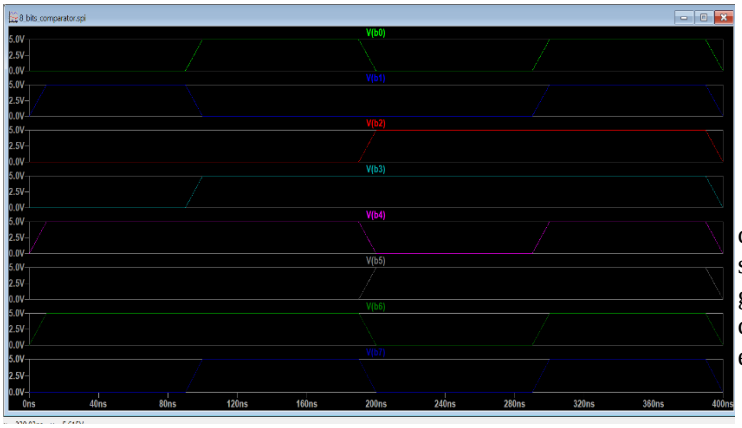


Figure 29:8-bit comparator simulation for input B

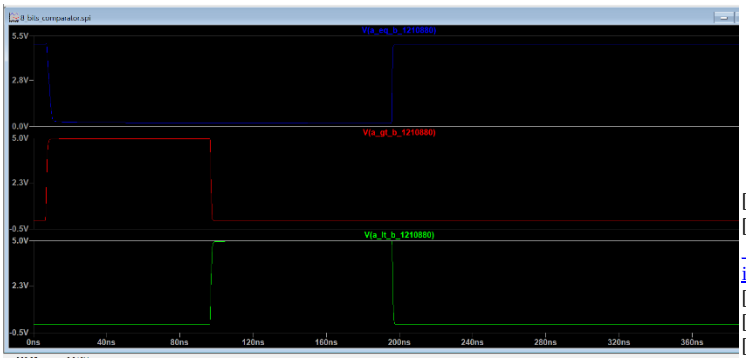


Figure 30:8-bit comparator simulation

.

Discussion

the results that we got for the 8bits comparator using the GDI technique was

1. the power consumption =77.01 microwatts it's lower than the CMOS which was 114.3 microwatts

2. the delay was 1.272ns it's also lower than CMOS delay which is 29.75ns

so we notice that the GDI technique is better than the CMOS so it's just faster, lower power consumption, more efficient.

I. Conclusions And Future work

In this project We have implemented many optimizations on the previous design, depending on different strategies like GDI technique, reducing the number of transistors, using logical optimization and so on, and We have succeeded in build until 8 –bit comparator, were designed and simulated, showing consistent improvements over traditional CMOS designs. These results demonstrate the potential of the GDI technique for enabling low-power, high-speed digital circuit applications.

For future work can focus on further enhancing the comparator design by utilizing smaller technology nodes. As semiconductor technology advances, scaling down to smaller geometries can provide even greater reductions in power consumption and delay while maintaining or improving area efficiency.

Acknowledgment

We want to thank Dr Khader Mohammad for the supervision in this project, and for the chance of trying new kind of projects. We are so thankful for the Eng.Raha zabadi she helped us a lot .

References

[1] https://www.analog.com/en/resources/glossary/comparator.html
[2]https://www.researchgate.net/publication/3952599_Gate-diffusion_input_GDI_-_A_technique_for_low_power_design_of_digital_circuits_Analysis_and_characterization
[3] https://ieeexplore.ieee.org/document/9641525
[4] https://www.ques10.com/p/65065/using-ic-7485-design-an-8-bit-comparator-1/
[5] https://www.ijera.com/papers/Vol4_issue8/Version%202/T4802120124.pdf