Faculty of Engineering & Technology
Electrical & Computer Engineering Department

DIGITAL INTEGRATED CIRCUITS- ENCS3330

Assignment 2

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Section: 2

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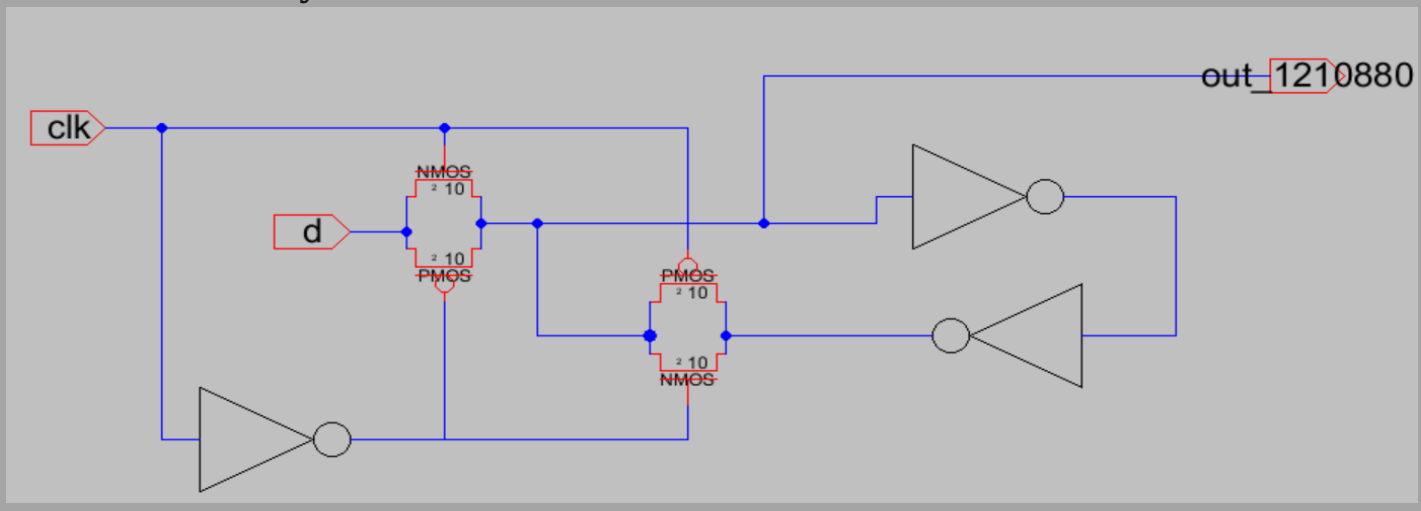

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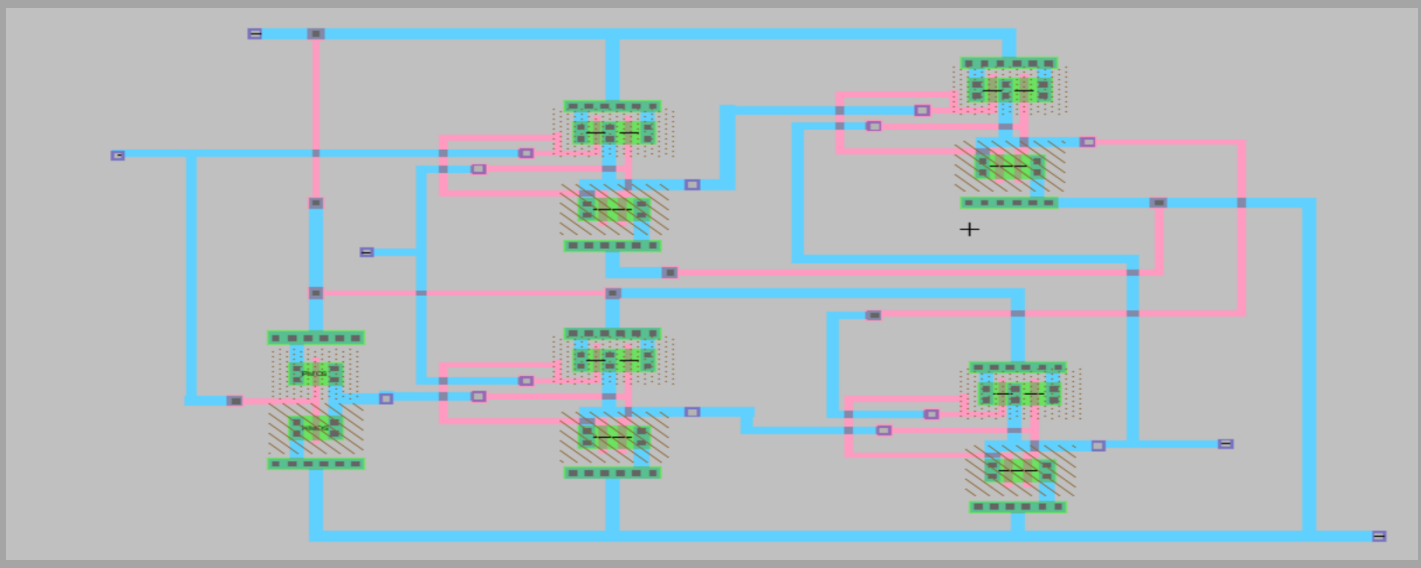

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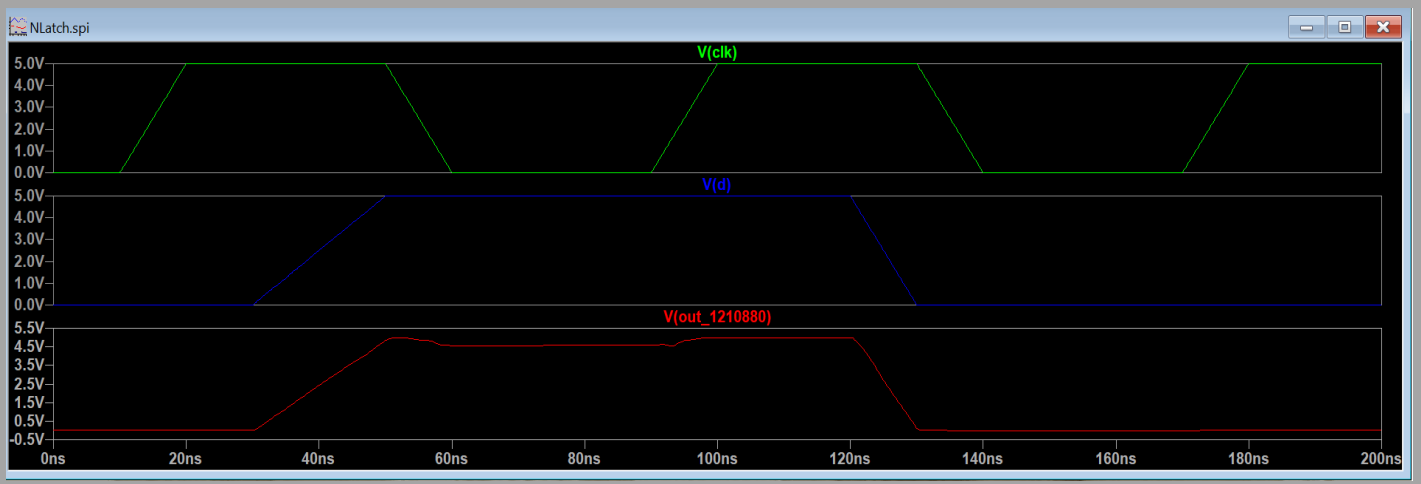

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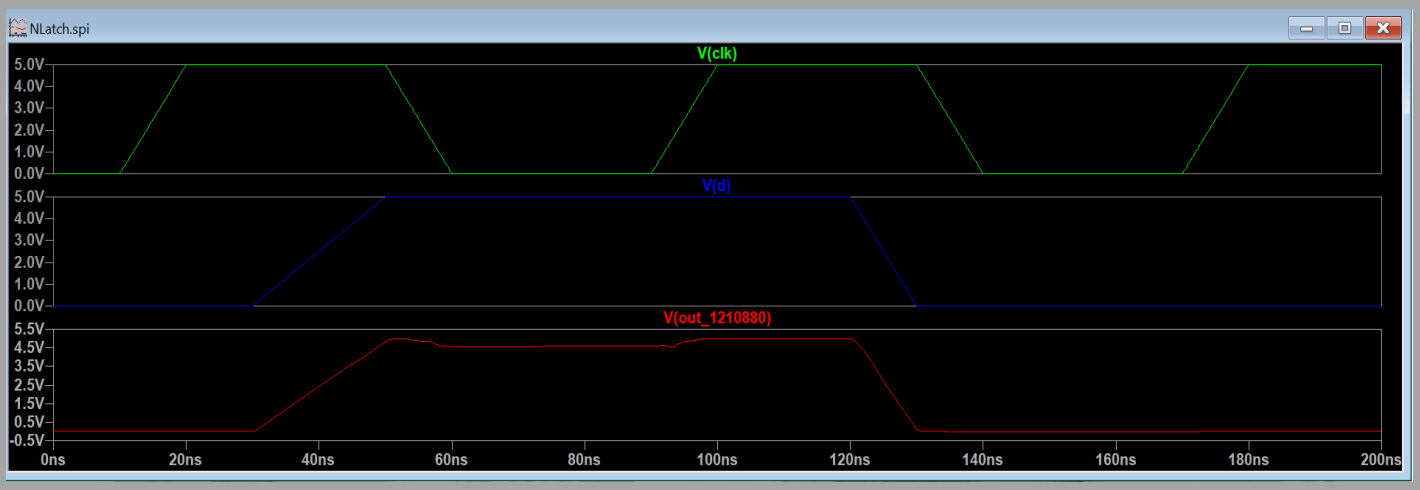

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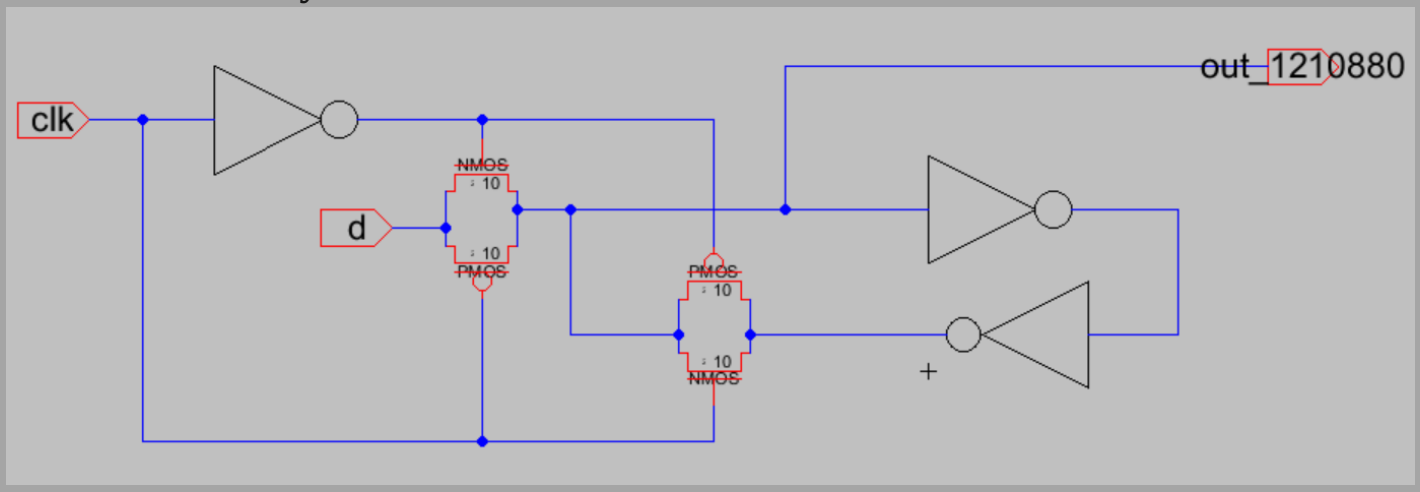
P-LATCH

Schematic & Layout & Simulation



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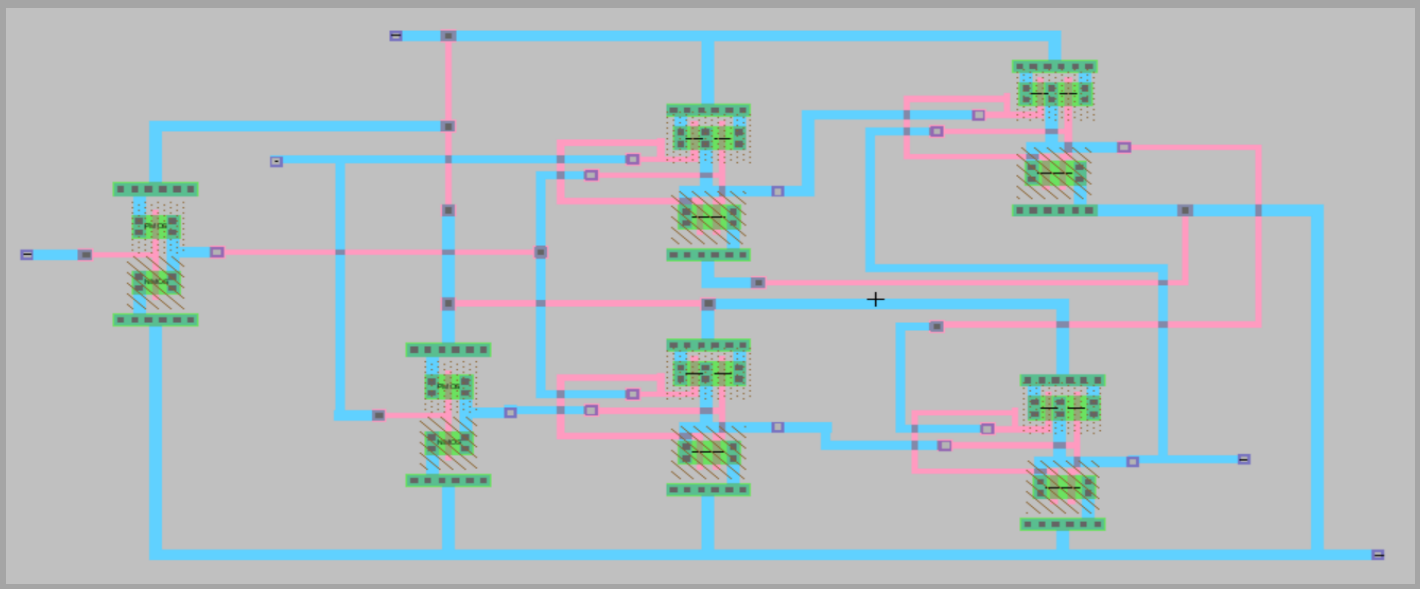

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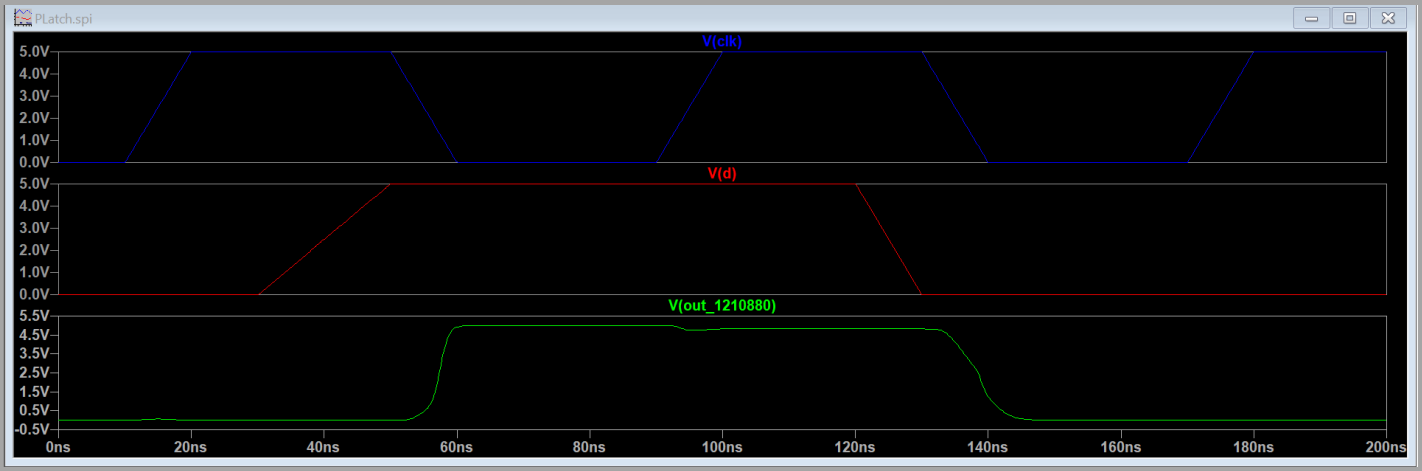

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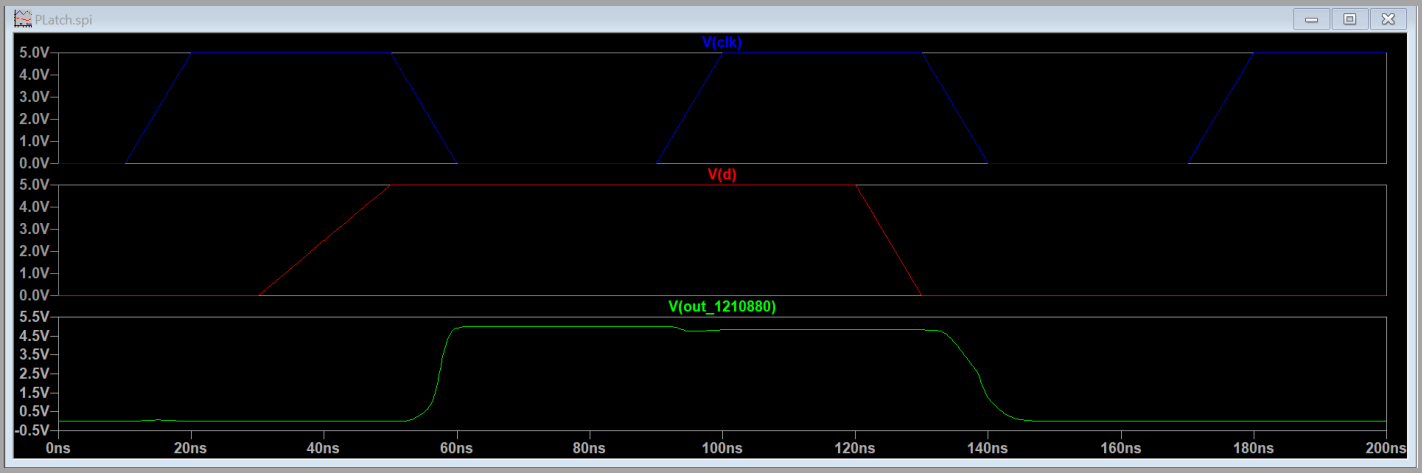

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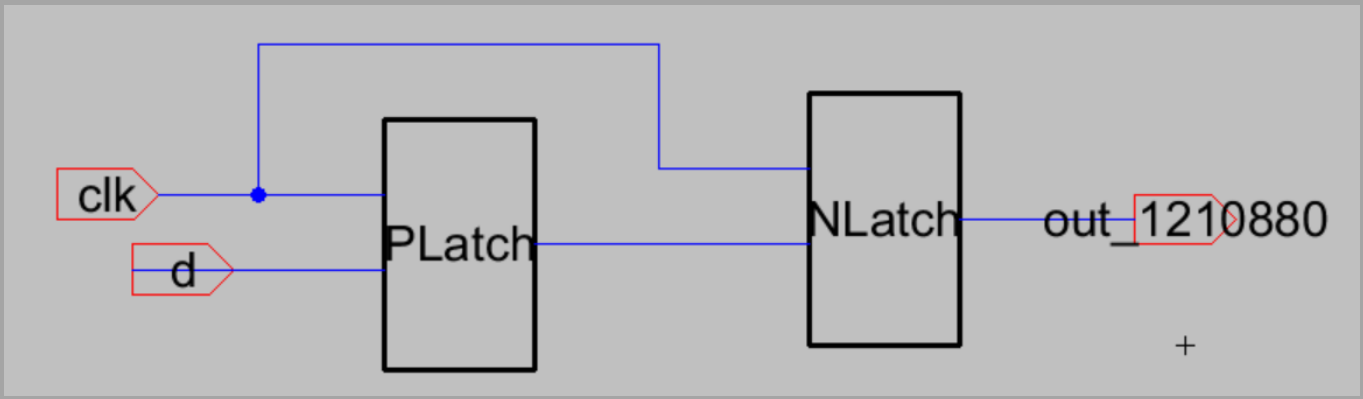
Rising edge flip-flop

Schematic & Layout & Simulation



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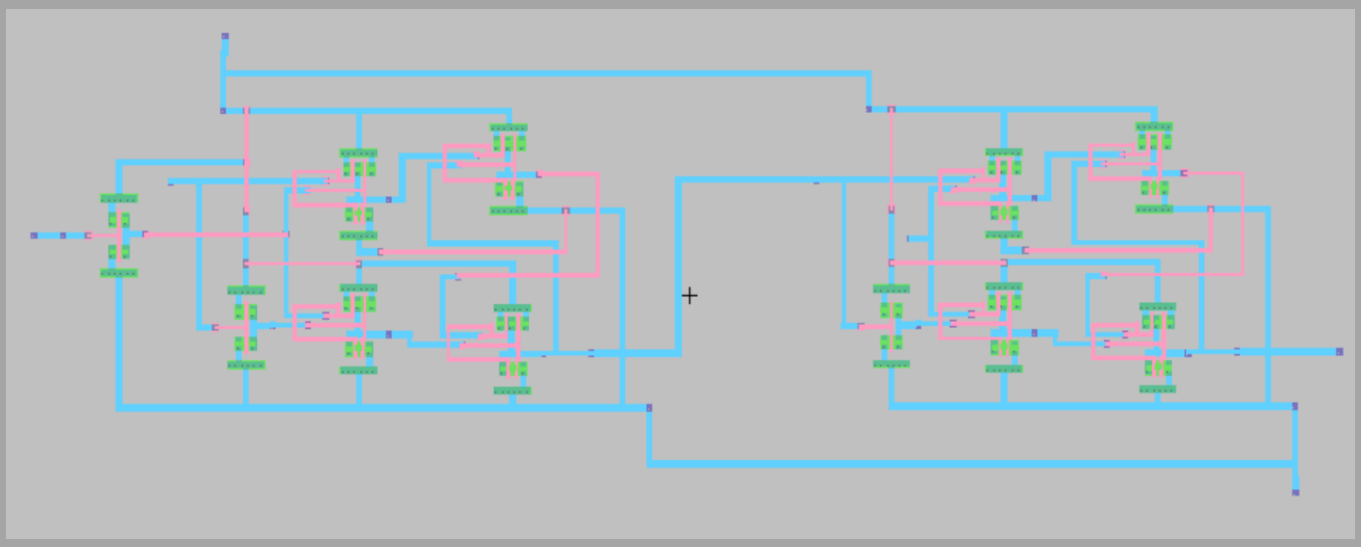

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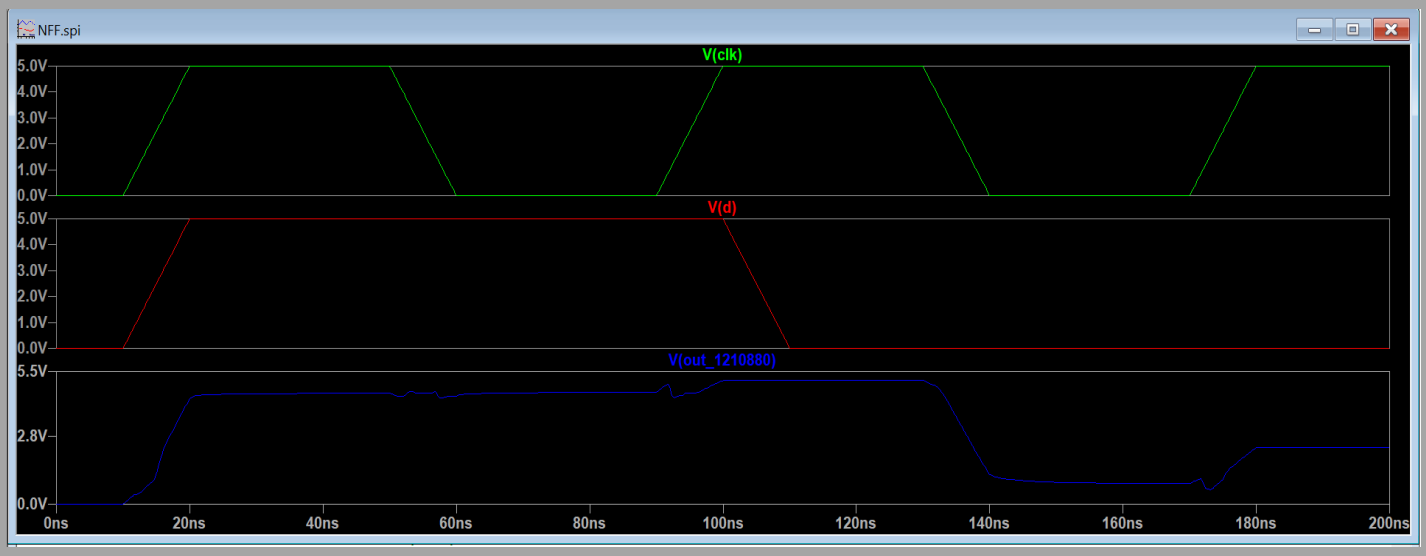

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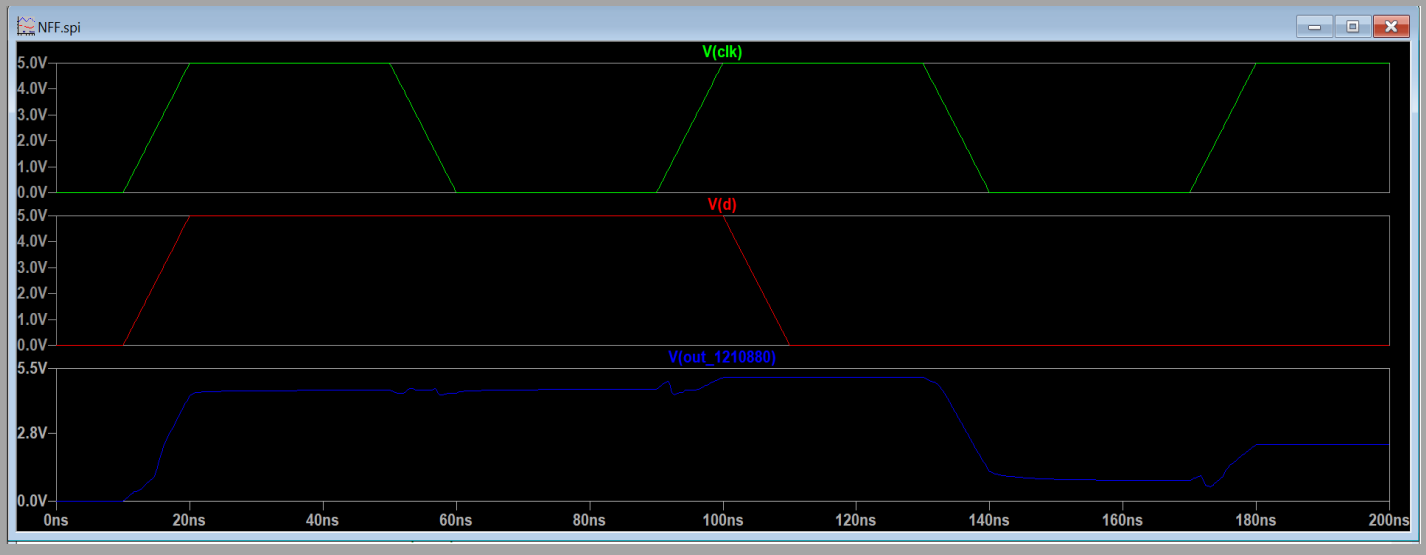

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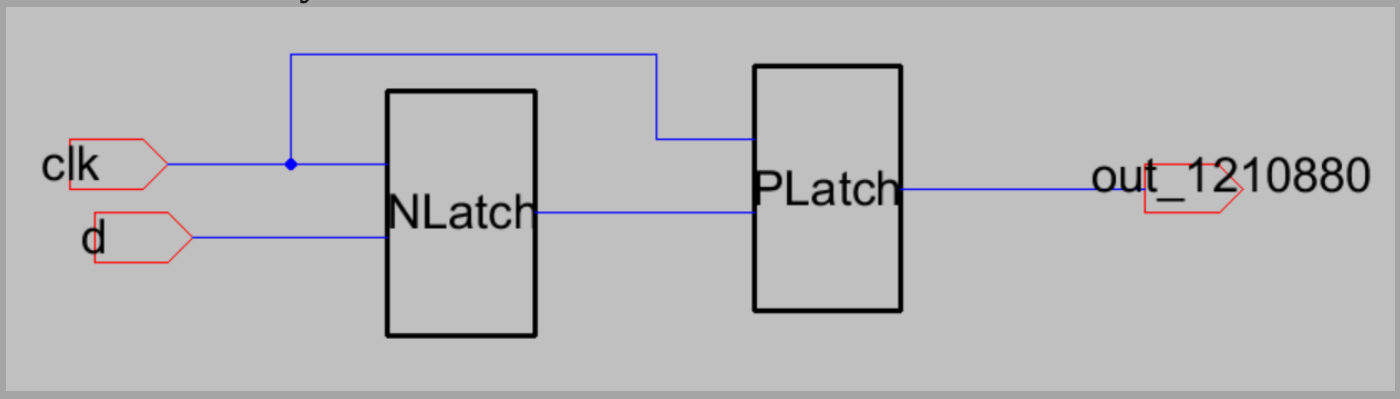
Falling edge flip-flop

Schematic & Layout & Simulation



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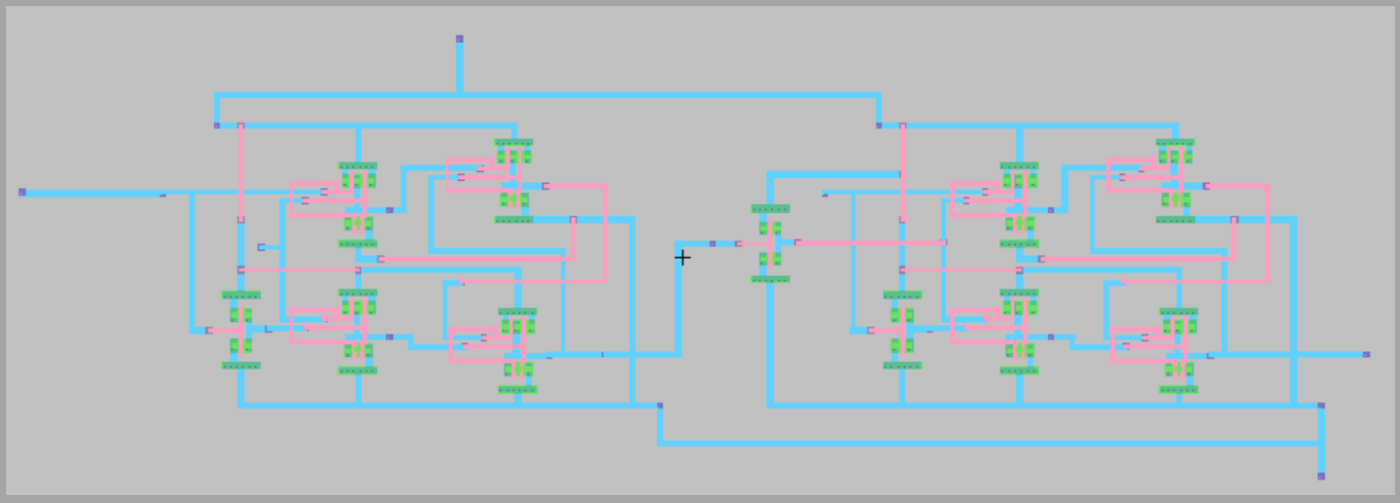

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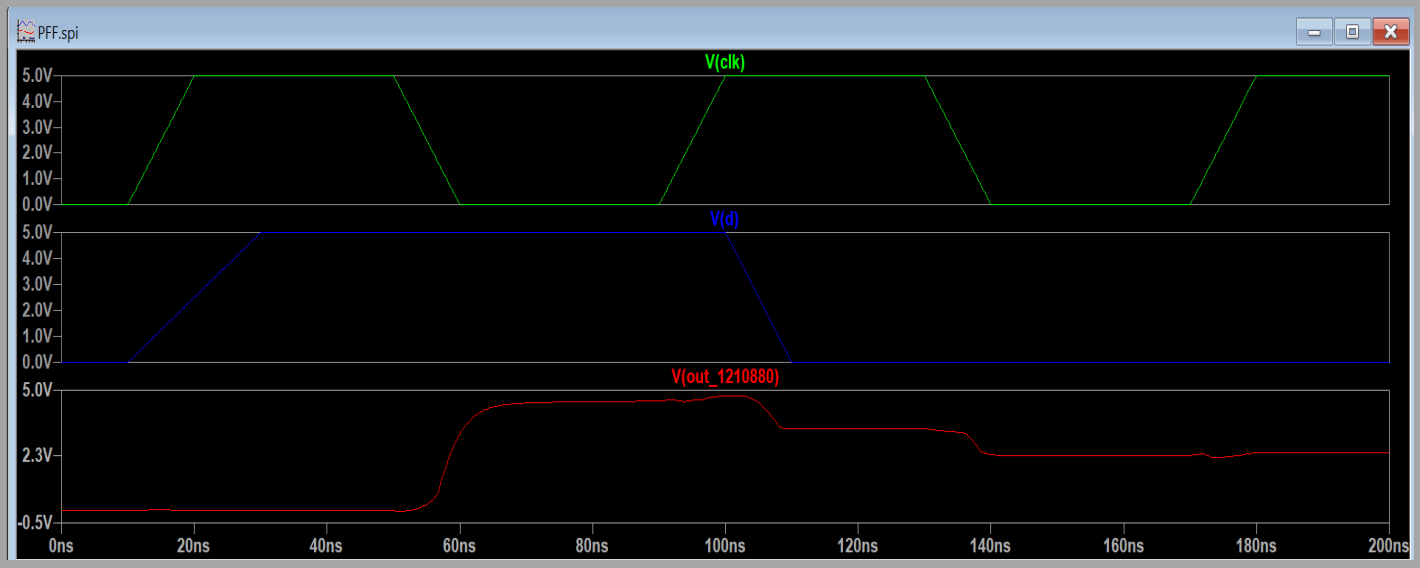

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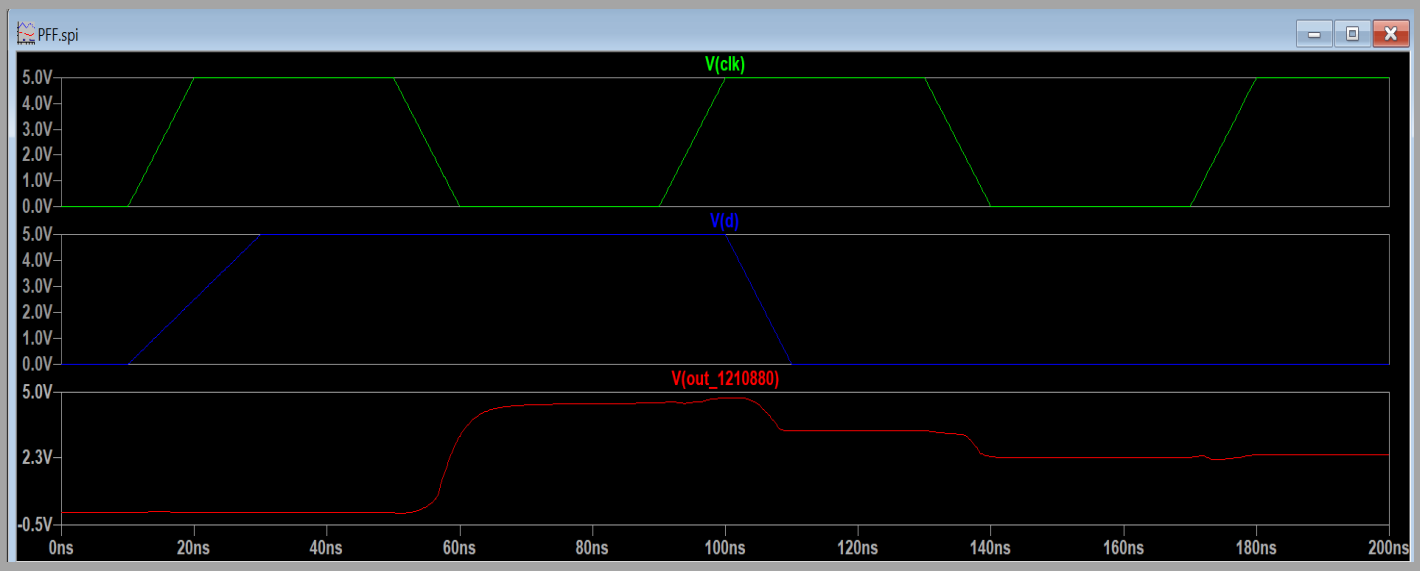

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