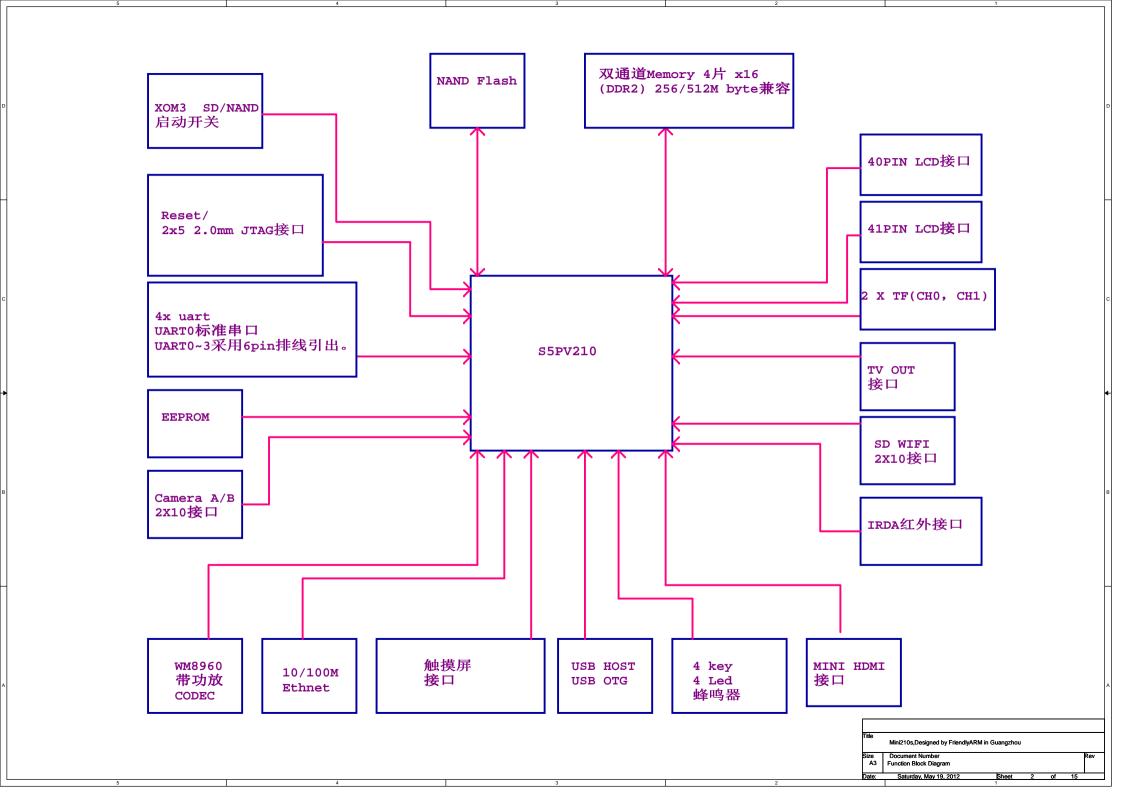
Revision History

Revision	Date	Comments	
1.0	2011-9-1	发布版本	
1.0	2011-11-25	修改为单通道内存 CON3 CON4由6PIN的改为4pin的	
	1	!	

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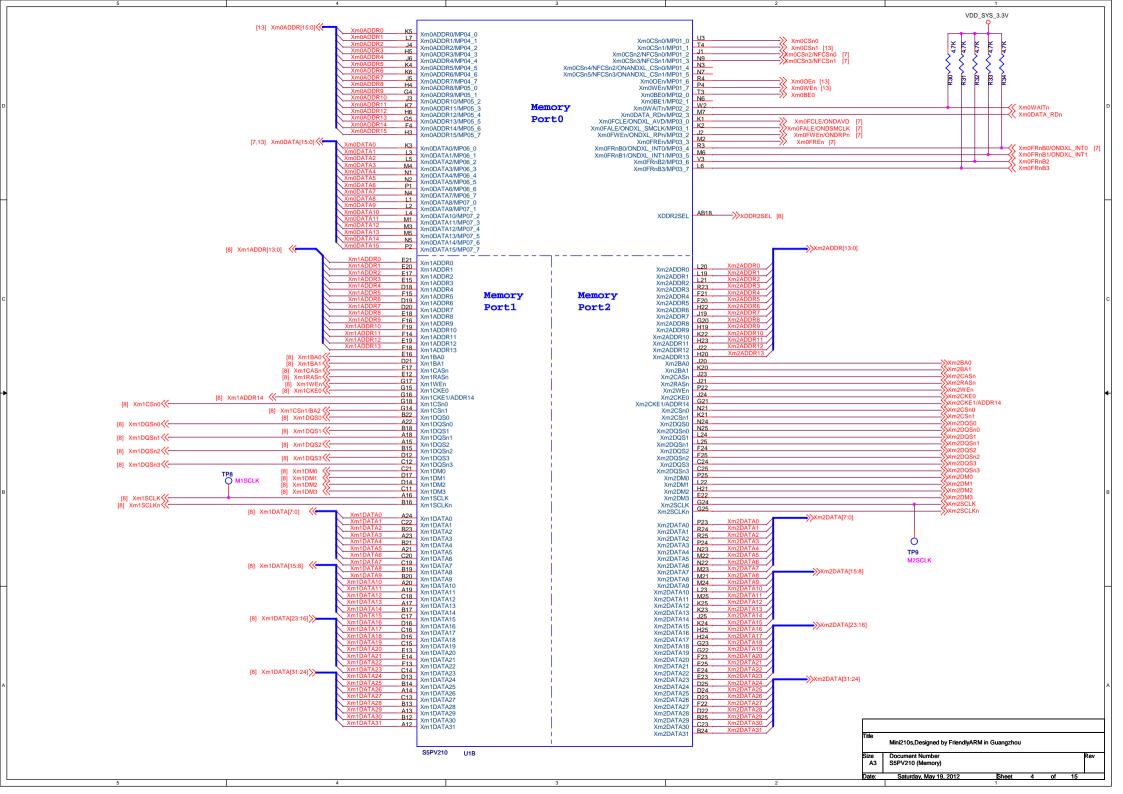
BootingMode Option U1A XuRXD0/GPA0_0 **XjTRST**n VDD_SYS_3.3V S2 [JTAG] R5 U4 XITMS (9) XuTXD0 XuTXD0/GPA0_1 XjTMS S300 XuCTSn0/GPA0_2 XuCTSn(XITCK A7 UART/IrDA XjTDI 1 2 3 4 5 W3 R1 XjTDO 100k DGND [9] XuRXD1 XURXD1/GPA0_4 XJDBGSEL [9] XuTXD1 [9] XuCTSn1 F10 XuTXD1/GPA0_5 B8 YOMO F10 [9] XuRTSn1 XuRTSn1/GPA0_7 YOM1 XM1 , XM2, XM3 SD 启动相关 [SYSTEM 1121 [9] XuRXD2 [9] XuTXD2 XuRXD2/UART_AUDIO_RXD/GPA1_0 XuTXD2/UART_AUDIO_TXD/GPA1_1 OPTION] XOM3 V25 XOM4 R17 V24 XOM5 VDD SYS 3.3V VDD 5V VDD SYS 3.3V AC13 XuRXD3/CTSn2/UART_AUDIO_CTSn/GPA1_2 XuTXD3/RTSn2/UART_AUDIO_RTSn/GPA1_3 [9] XuRXD3 [9] XuTXD3 200R **VXXTI** YYTI [CLOCK] U25 XXTO Эххто. XXTO [9] [15] XspiCLK0 XspiCLK0/GPB0 XusbXTI R211R208 F9 SYSTEM AF20 [15] XsniCS0 XsniCSn0/GPR1 XushXTO XusbXTO 191 AE24 XOM[5:0] XspiMISO0/GPB2 XCLKOUT ->>xci kout DGND DGND 10K 10K J11 XhdmiXTI [9] [15] XspiMOSI0 XspiMOSI0/GPB3 YhdmiYT HS-SPI XhdmiXTO [9] YeniCl K1/GPR/ [15] YeniCLK1 B11 XnWRESET [15] XspiCS1 XspiCSn1/GPB5 ->>XnWRESET [RESET] ⟨XnRESET [9] 15] XspiMISO1 XsniMISO1/GPB6 XnRESET U51 VDD SYS 3.3V A11 [15] XspiMOSI1 XspiMOSI1/GPB7 XnRSTOUT ->>XnRSTOUT [10.13.15] R18 _ _ OR/NC AE19 [15] XuhDP [15] XuhDN XuhDP XPWRRGTON XPWRRGTON [14,15] VCC XuhDM R20 AC17 USB HOST2.0 O TP4 R19 44 2K 1% XuhREXT XrtcXTI XuhPWREN XrtcXTO [9] GND XubOVERCUR 74LVC1G04 10K/NC ->>XRTCCLKO XRTCCLKO DGND AD21 [15] Base XuoDP XuoDP R21 OR [15] Base_XuoDM AE21 DGND XuoDM XefFSOURCE DGND AF18 USB OTG 2.0 R22 44.2K.1% XUOREXT AD18 XpwmTOUT0 [15] XpwmTOUT1 [10] XpwmTOUT2 [15] [15] XuolD XpwmTOUT0/GPD0 0 XuoID ΔC18 [15] XuoVBUS XuoVBUS XpwmTOUT1/GPD0_1 AC19 XpwmTOUT2/GPD0_2 [15] XuoDRVVBUS XuoDRVVBUS XpwmTOUT3/PWM_MIE/GPD20_3 XpwmTOUT3 [15] [11] Audio Xi2sSCLK0 (Xi2sSCLK0/PCM_SCLK2 AC4 Audio_Xi2sCDCLK0 Audio_Xi2sLRCK0 OM1 OM2 Xi2sCDCLK0/PCM_EXTCLK2 AF3 PWM Timer Xi2sI RCK0/PCM_ESYNC2 OM3 OM4 Xi2sSDI0/PCM_SIN2 AD3 [11] Audio Xi2sSDO0 0 Xi2sSDO0_0/PCM_SOUT2 ×AC3 ×AA3 I2S/PCM/AC97 XEINT0/GPH0_0 Xi2sSDO0 W25 Xi2sSDO0 2 XEINT1/GPH0 XEINT1 [15 W23 XEINT2/GPH0 2 XEINT2 AD1 V25 Xi2sCLK1/PCM_SCLK1/AC97_BITCLK Xi2sSCLK1/PCM_SCLK1/AC97BITCLK/GPC0_0 YEINT3/GPH0 3 启动方式 AB3 AA22 Xi2sCDCLK1/PCM_EXTCLK1/AC97_RESETn Xi2sCDCLK1/PCM_EXTCLK1/AC97RESETn/GPC0_1 XEINT4/GPH0_4 XEINT4 W24 Xi2sLRCK1/PCM_FSYNC1/AC97_SYNC Xi2sLRCK1/PCM_FSYNC1/AC97SYNC/GPC0_2 Xi2sSDI1/PCM_SIN1/AC97SDI/GPC0_3 XEINT5/GPH0 XEINT5 [10,15] XEINT6 [10,15] AA5 XEINT6/GPH0_6 W21 AB4 AA25 EINT Xi2sSDO1/PCM SOUT1/AC97 SDO Xi2sSDO1/PCM SOUT1/AC97SDO/GPC0 4 XEINT7/GPH0 V20 XEINT8/GPH1 KEYPAD V22 Y24 XpcmSCLK0/SPDIF_OUT0/Xi2sSCLK2 XpcmSCLK0/SPDIF_OUT0/Xi2sSCLK2/GPC1_0 XpcmEXTCLK0/SPDIF_EXTCLK/Xi2sCDCLK2/GPC1_1 XEINT9/GPH1 XEINT9 [15] AA1 XEINT10 [10] XpcmEXTCLK0/SPDIF EXTCLK/Xi2sCDCLK2 XFINT10/GPH1 W22 AA24 Sevele XpcmFSYNC0/LCD_FRM/Xi2sLRCK2 XpcmFSYNC0/LCD_FRM/Xi2sLRCK2/GPC1_2 USBOTG_OVERCUR [15] HDMI_CEC [15] AR2 XEINT12/HDML CEC/GPH1 XncmSIN0/Xi2sSDI2 XncmSIN0/Xi2sSDI2/GPC1 3 XpcmSOUT0/Xi2sSDO2 XpcmSOUT0/Xi2sSDO2/GPC1_4 XEINT13/HDMI_HPD/GPH1 HDMI_HPD [15] rvole (default) AB25 XEINT14/GPH1_6 [10] YEINT14/GPH1 (Nand 16bit ECC) W20 XEINT15/GPH1_7 XEINT16/KP COL0 XmmcCLK0/GPG0 0 XEINT15/GPH1 E6 F7 1120 XmmcCMD0 Xmmc0CDn Xmmc0DATA0 XEINT16/KP_COL0/GPH2_ XEINT17/KP_COL1/GPH2 XmmcCMD0/GPG0 Y23 Xmmc0CDn/GPG0_2 C5 HS-MMC V21 AB24 Xmmc0DATA0/GPG0_3 Xmmc0DATA1/GPG0_4 XEINT18/KP_COL2/GPH2 XFINT18/KP COL2 A5 XEINT19/KP COL3/GPH2 3 AA21 AA23 Xmmc0DATA2 Xmmc0DATA2/GPG0_5 XEINT20/KP_COL4/GPH2_ XEINT20/KP COL4 [9] Xmmc0DATA3 C6 XEINT21/KP_COL5 Xmmc0DATA3/GPG0_6 XFINT21/KP COL5/GPH2 XEINT22/KP_COL6/GPH2_ XFINT22/KP COL6 Y20 XEINT23/KP_COL7 XmmcCl K1 Xmmc1CLK/GPG1_0 XEINT23/KP COL7/GPH2 F8 XmmcCMD1 XmmcCDn1 XEINT24/KP_ROW0 XEINT25/KP_ROW1 C7 AB22 Ymmc1CDn/GPG1 2 YEINT25/KP POW/1/GPH3 AD25 Xmmc1DATA0/Xmmc0DATA4/GPG1_3 XEINT26/KP_ROW2/GPH3_2 XEINT26/KP_ROW2 XEINT27/KP_ROW3 Xmmc1DATA0 F7 Y22 AD24 Xmmc1DATA1 Xmmc1DATA2 Xmmc1DATA1/Xmmc0DATA5/GPG1_4 Xmmc1DATA2/Xmmc0DATA6/GPG1_5 XEINT27/KP_ROW3/GPH3 3 A6 XEINT28/KP ROW4/GPH3 4 XEINT28/KP_ROW4 AA20 Y19 F9 Xmmc1DATA3 Xmmc1DATA3/Xmmc0DATA7/GPG1_6 XEINT29/KP ROW5/GPH3 XFINT29/KP ROW5 XEINT30/KP ROW6/GPH3 (Xmmc2CLK/SPLCLK2/GPG2_0 XEINT31/KP_ROW7/GPH3_ XEINT31/KP ROW7 W6 Xmmc2CMD/SPI_CSn2/GPG2_1 Xmmc2CDn/SPI_MISO2/GPG2_2 [15] XmmcCMD2 [15] XmmcCDn2 Xi2cSDA0/GPD1_0 CODEC/EEPROM/CAMERA A/SD WIFI C9 AE23 Y4 [15] Xmmc2DATA0 [15] Xmmc2DATA1 Xmmc2DATA0/SPI_MOSI2/GPG2_3 Xi2cSCL0 [9,11,15] Xi2cSDA1 [15] Xi2cSCL0/GPD1 1 Xmmc2DATA1 Xmmc2DATA1/GPG2_4 Xi2cSDA1/GPD1 CAMERA B/HDM1 AD22 Y3 I2C Ymmc2DATA2 Ymmc2DATA2/GPG2 5 Yi2cSCL1/GPD1 Yi2cSCL1 W4 AC16 [15] Xmmc2DATA3 Xmmc2DATA3/GPG2 6 Xi2cSDA2/IEM_SCLK/GPD1 TOUCH PANAL Xi2cSCL2/IEM SPWI/GPD1 Xi2cSCL2 [10,15] XmmcCLK3 D10 OVDD_SYS_3.3V XmmcCMD3 Xmmc3CMD/GPG3 1 E11 XmmcCDn3 Xmmc3CDn R21 Xmmc3DATA0 Xmmc3DATA0/Xmmc2DATA4/GPG3 3 NC/EPLL(evt1) C10 EPLL Filter Xmmc3DATA1/Xmmc2DATA5/GPG3 4 Xmmc3DATA1 D11 Xmmc3DATA2/Xmmc2DATA6/GPG3_5 A10 Xmmc3DATA3 Xmmc3DATA3/Xmmc2DATA7/GPG3_6 S5PV210 Mini210s, Designed by Friendly ARM in Guangzhou

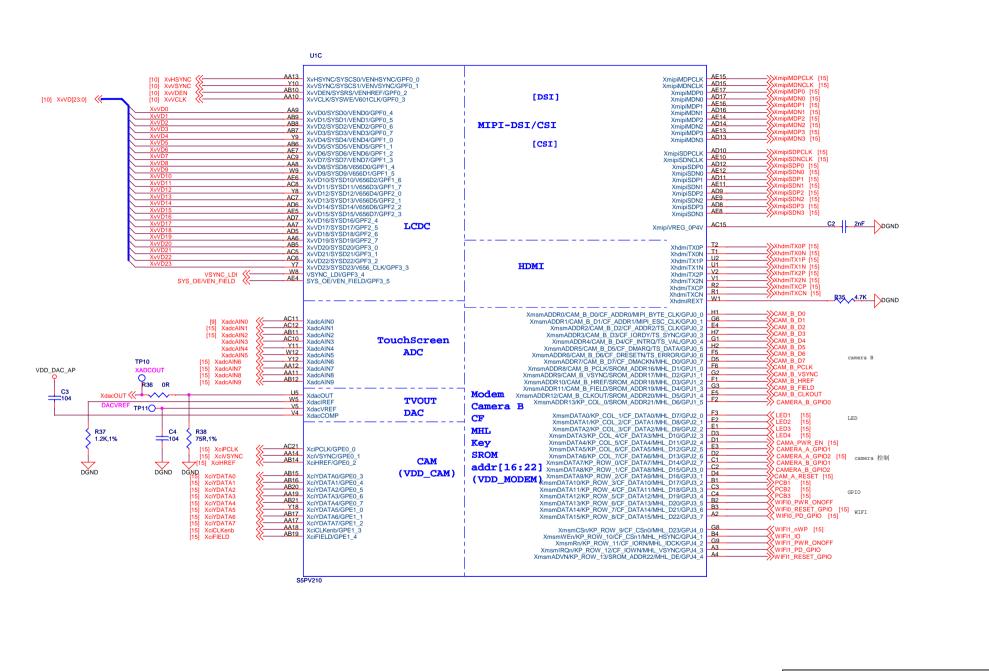
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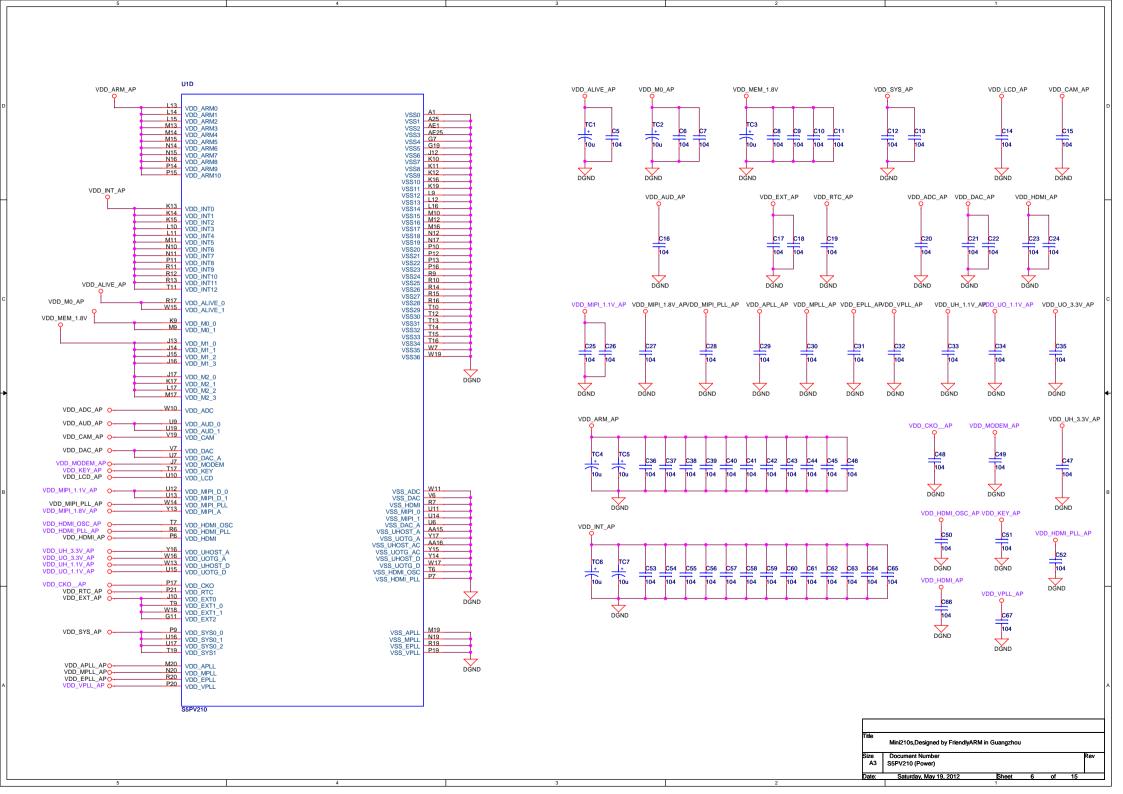


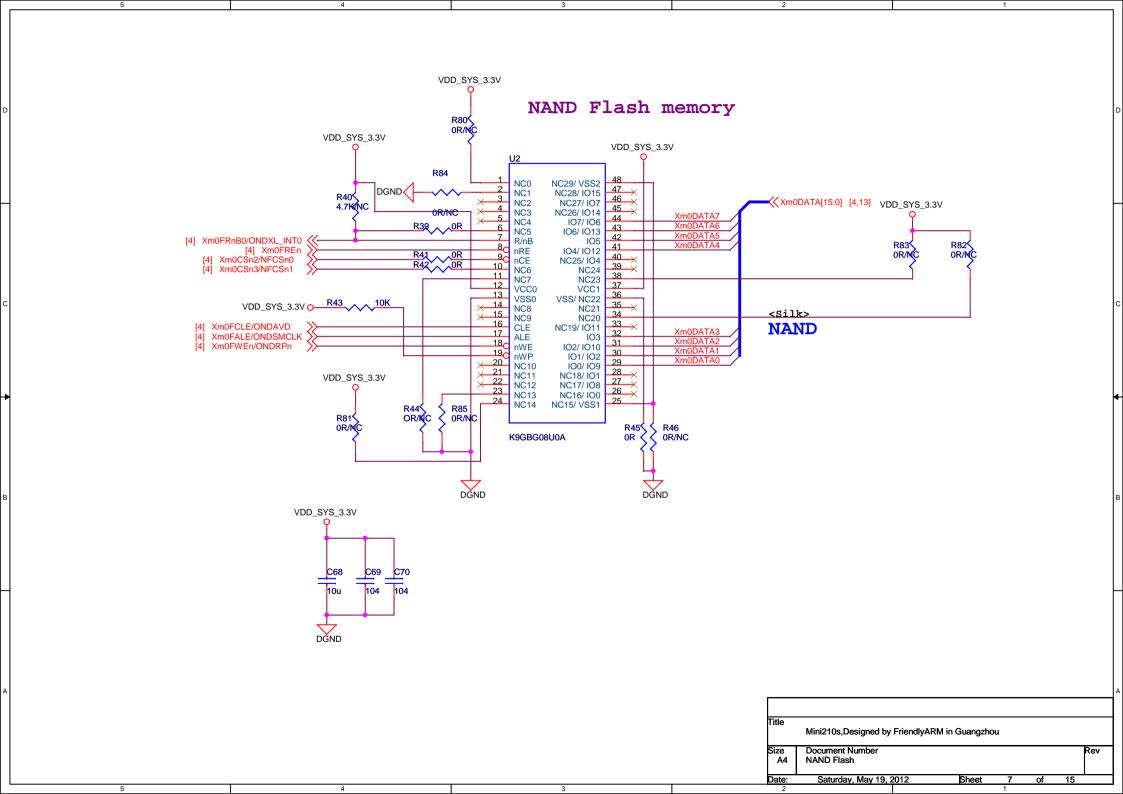


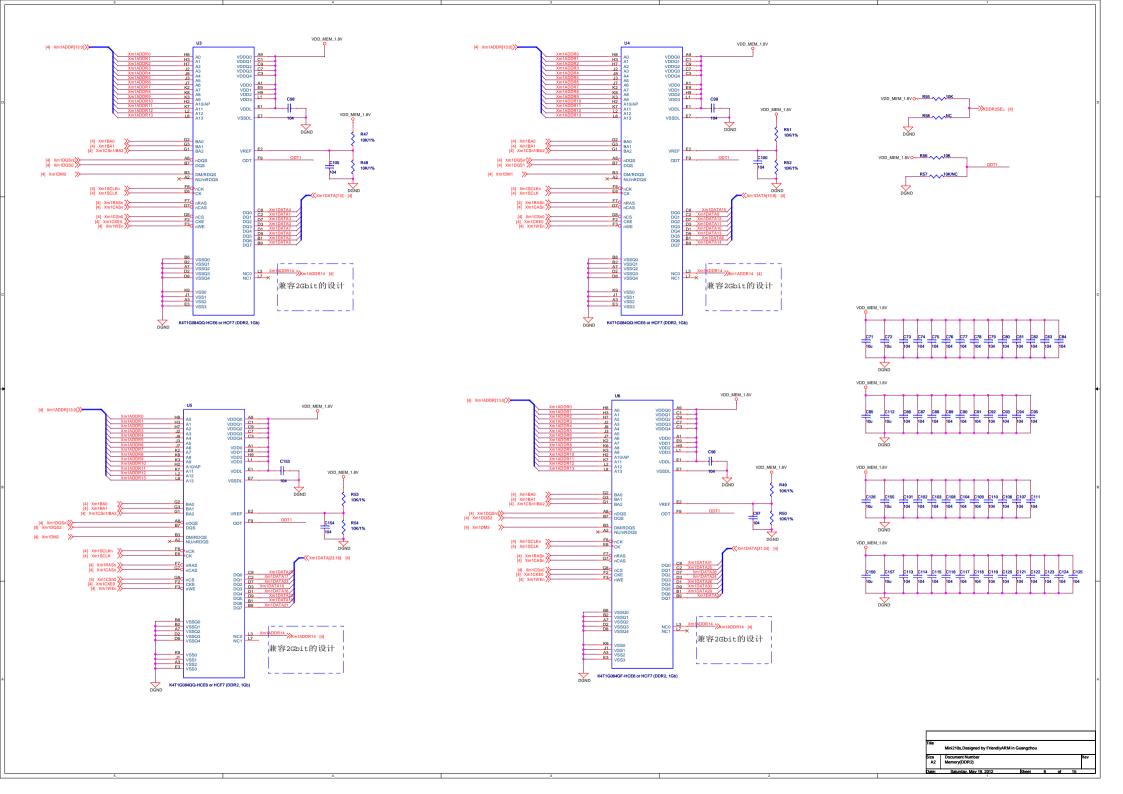
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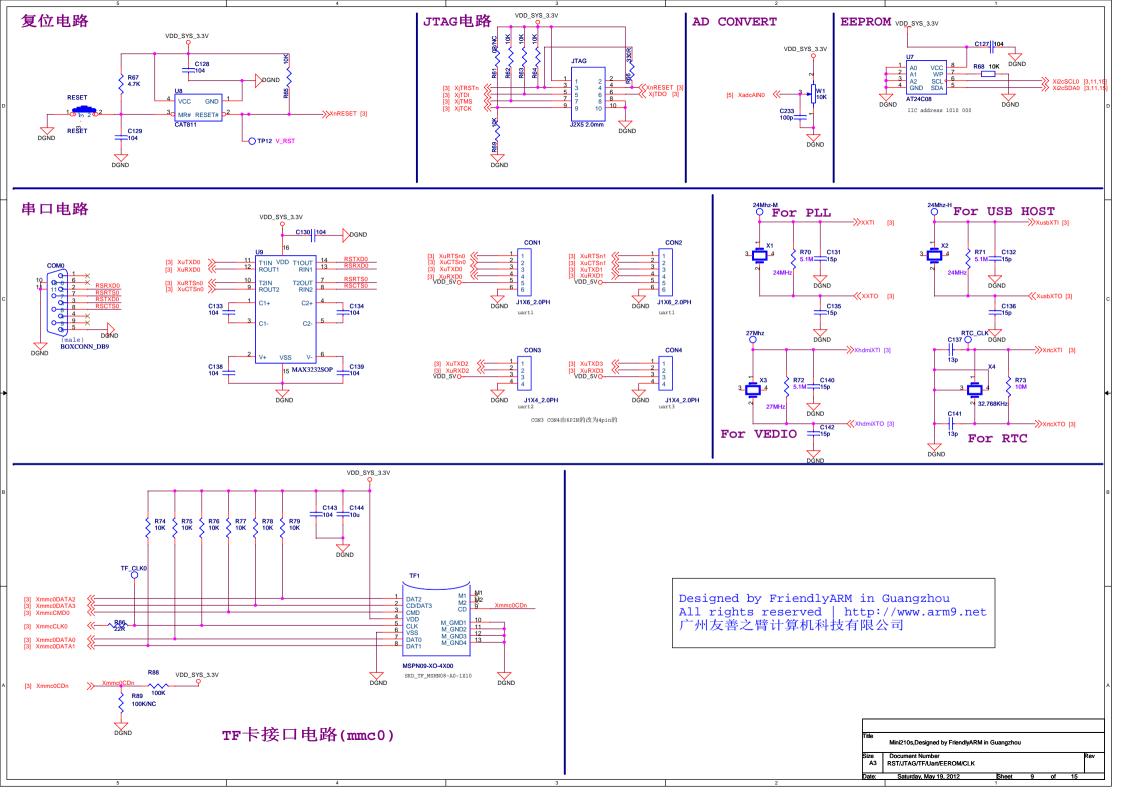
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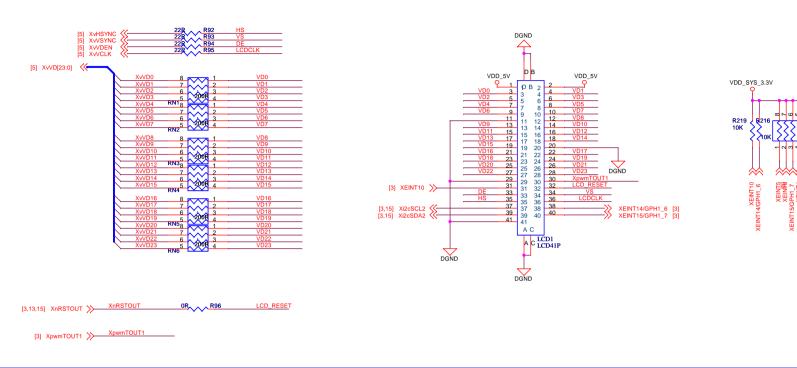




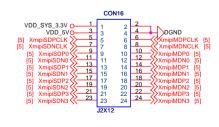




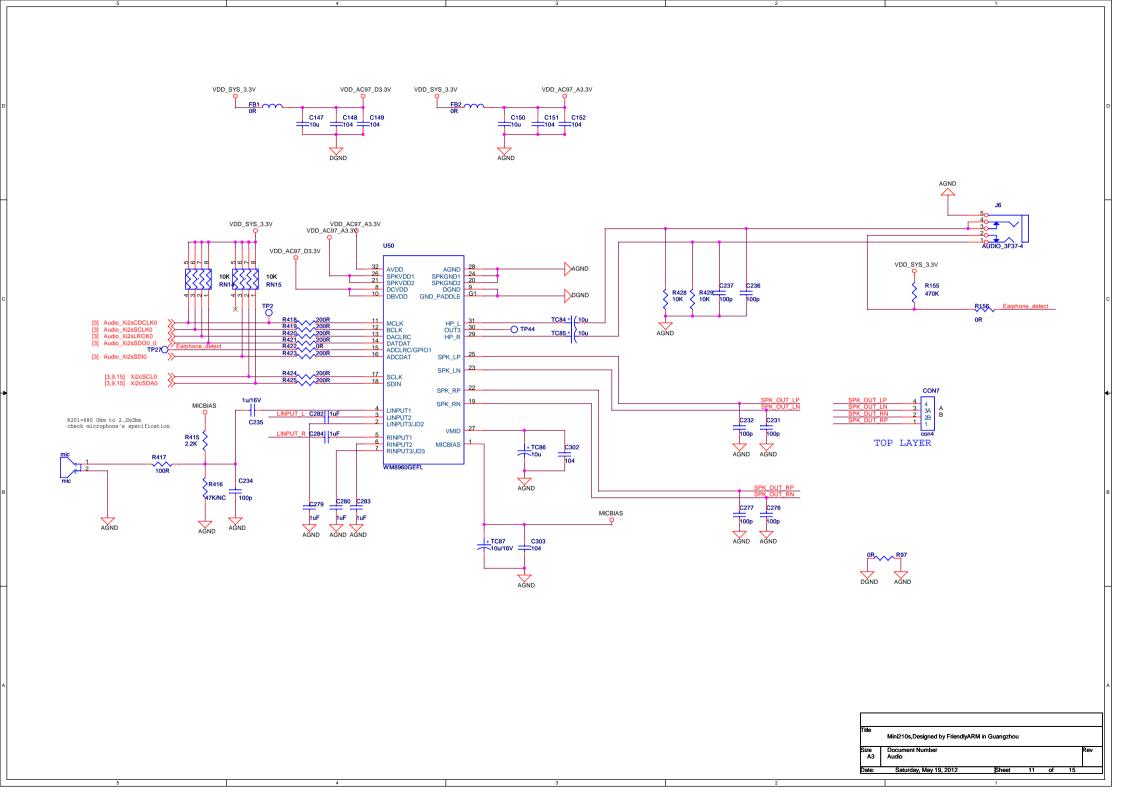
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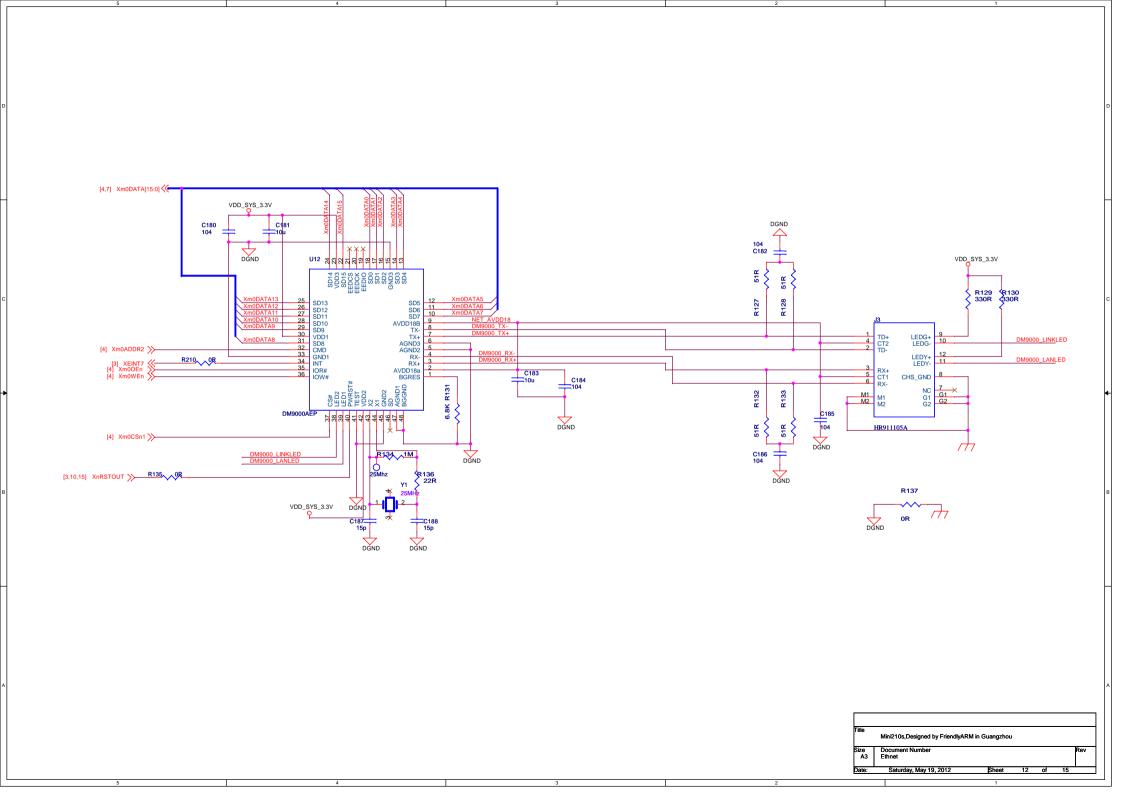


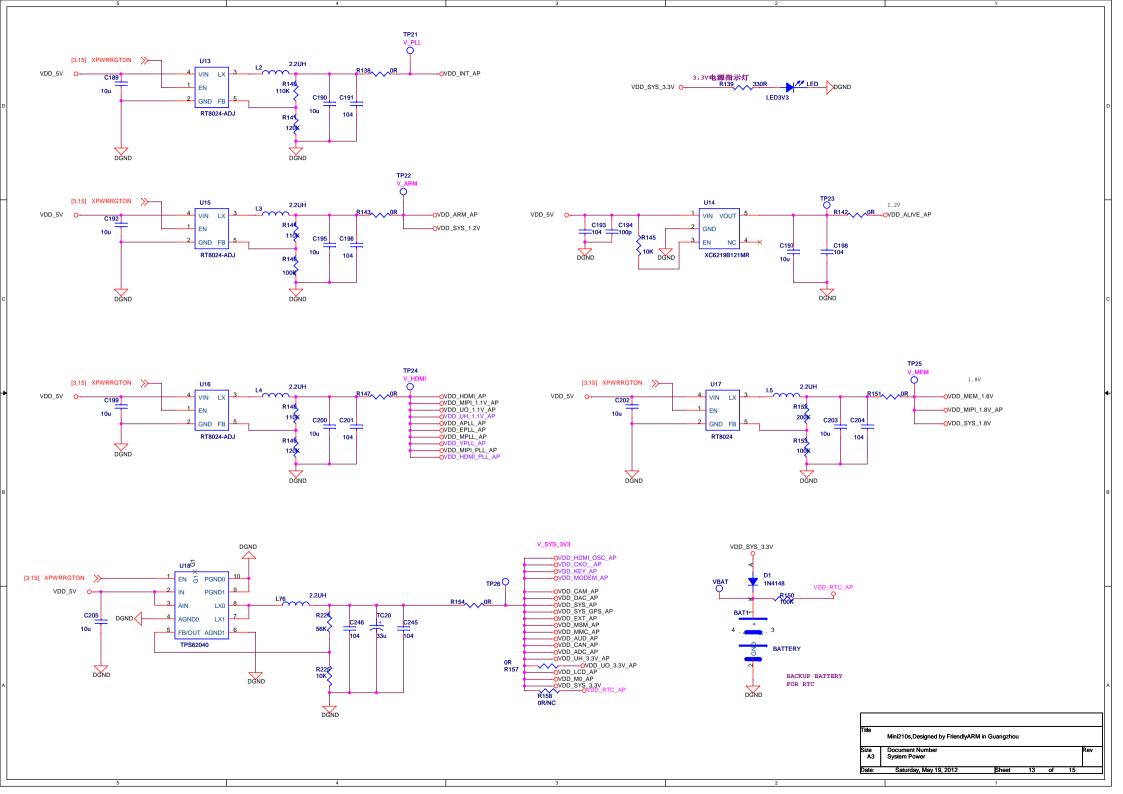
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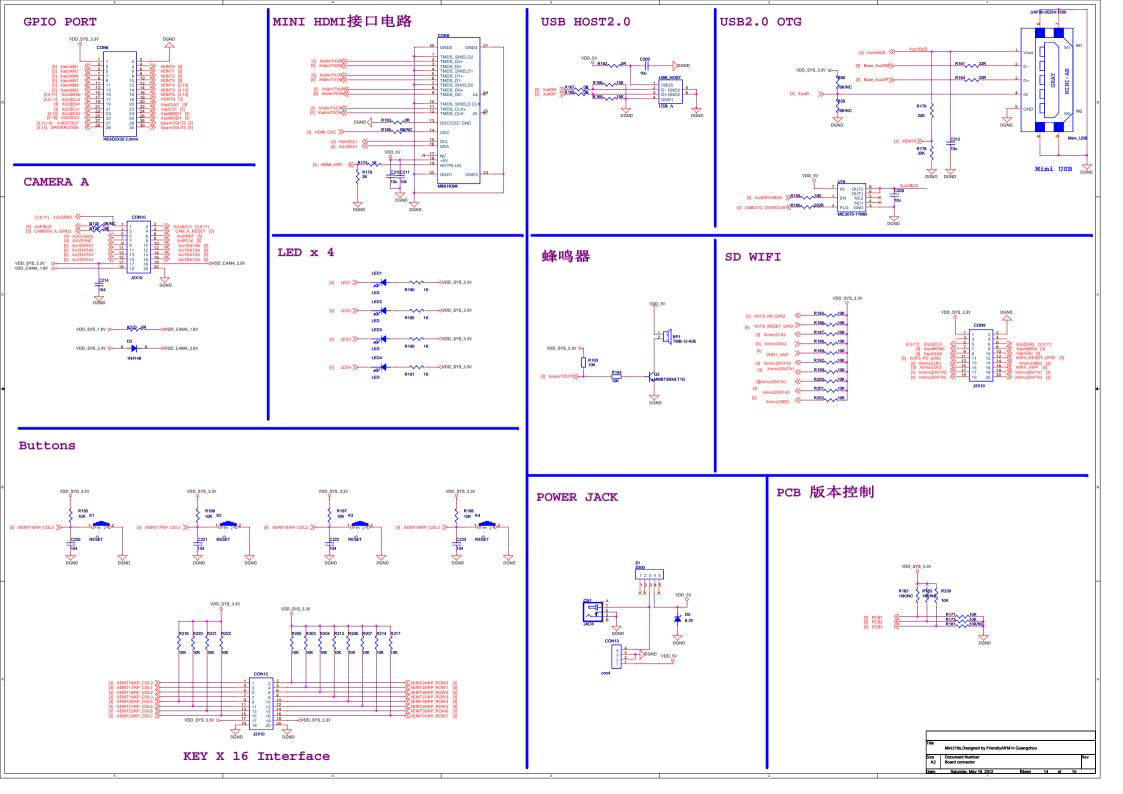


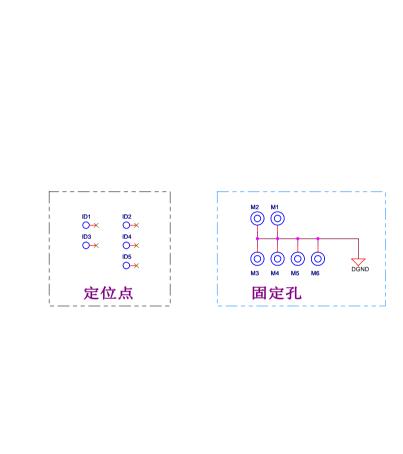
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