

## 1. Description

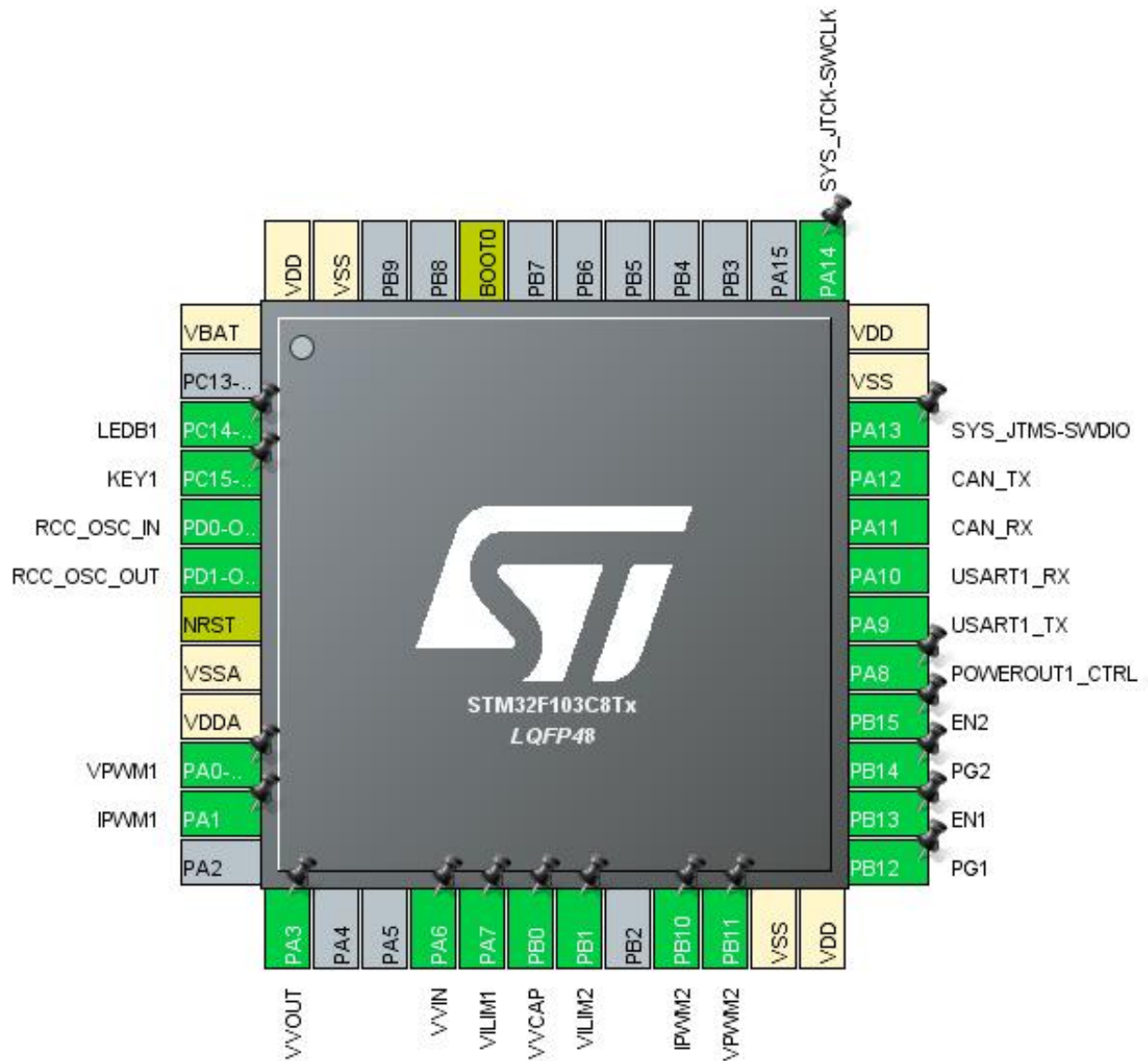
### 1.1. Project

Project Name	Codes
Board Name	custom
Generated with:	STM32CubeMX 5.3.0
Date	03/22/2020

### 1.2. MCU

MCU Series	STM32F1
MCU Line	STM32F103
MCU name	STM32F103C8Tx
MCU Package	LQFP48
MCU Pin number	48

## 2. Pinout Configuration

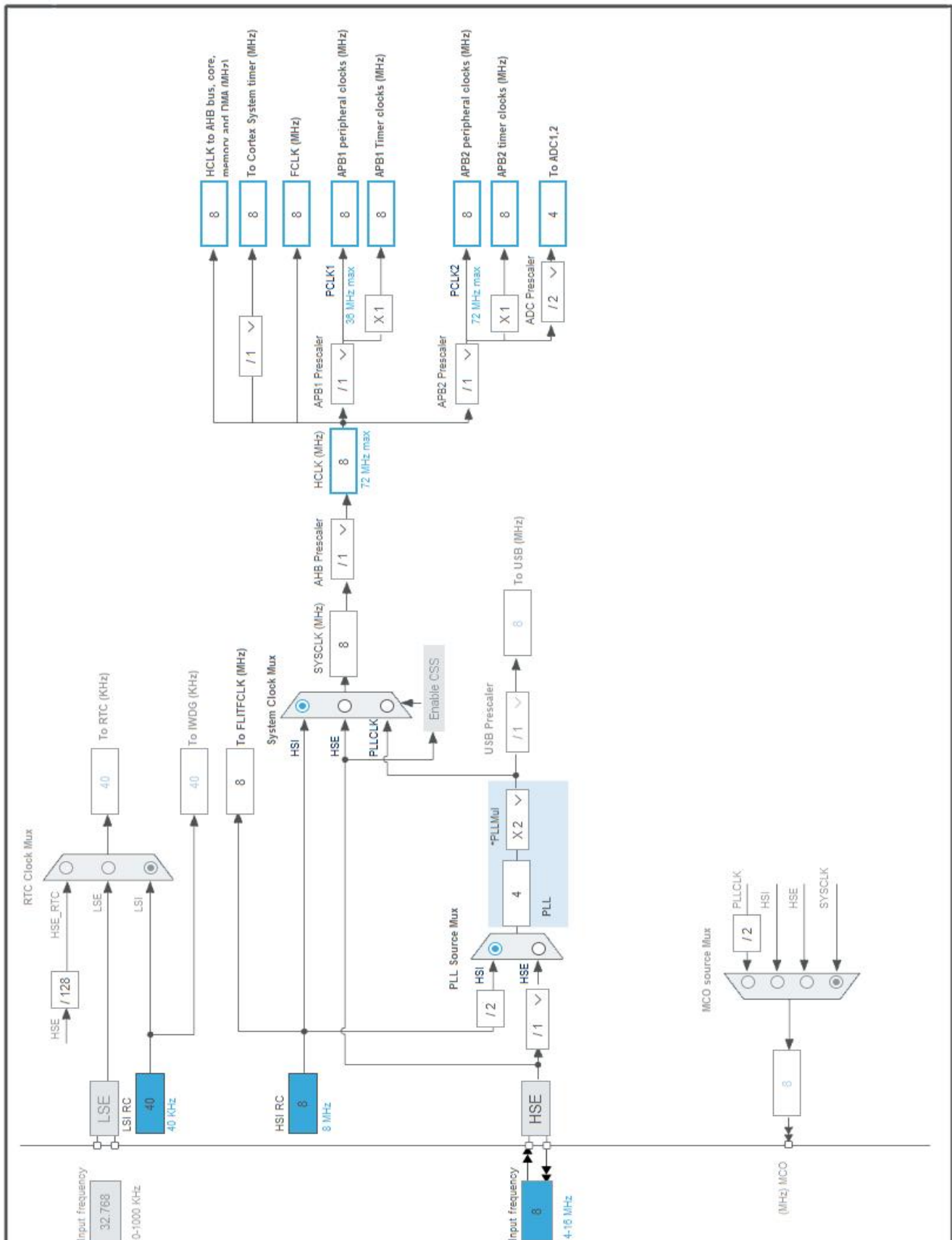


### 3. Pins Configuration

Pin Number LQFP48	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	VBAT	Power		
3	PC14-OSC32_IN *	I/O	GPIO_Output	LEDB1
4	PC15-OSC32_OUT *	I/O	GPIO_Input	KEY1
5	PD0-OSC_IN	I/O	RCC_OSC_IN	
6	PD1-OSC_OUT	I/O	RCC_OSC_OUT	
7	NRST	Reset		
8	VSSA	Power		
9	VDDA	Power		
10	PA0-WKUP	I/O	TIM2_CH1	VPWM1
11	PA1	I/O	TIM2_CH2	IPWM1
13	PA3	I/O	ADC1_IN3, ADC2_IN3	VVOUT
16	PA6	I/O	ADC1_IN6, ADC2_IN6	VVIN
17	PA7	I/O	ADC1_IN7, ADC2_IN7	VILIM1
18	PB0	I/O	ADC1_IN8, ADC2_IN8	VVCAP
19	PB1	I/O	ADC1_IN9, ADC2_IN9	VILIM2
21	PB10	I/O	TIM2_CH3	IPWM2
22	PB11	I/O	TIM2_CH4	VPWM2
23	VSS	Power		
24	VDD	Power		
25	PB12 *	I/O	GPIO_Input	PG1
26	PB13 *	I/O	GPIO_Output	EN1
27	PB14 *	I/O	GPIO_Input	PG2
28	PB15 *	I/O	GPIO_Output	EN2
29	PA8 *	I/O	GPIO_Output	POWEROUT1_CTRL
30	PA9	I/O	USART1_TX	
31	PA10	I/O	USART1_RX	
32	PA11	I/O	CAN_RX	
33	PA12	I/O	CAN_TX	
34	PA13	I/O	SYS_JTMS-SWDIO	
35	VSS	Power		
36	VDD	Power		
37	PA14	I/O	SYS_JTCK-SWCLK	
44	BOOT0	Boot		
47	VSS	Power		
48	VDD	Power		

\* The pin is affected with an I/O function

## 4. Clock Tree Configuration



## 5. Software Project

### 5.1. Project Settings

Name	Value
Project Name	Codes
Project Folder	D:\Artinx\SuperCapacitor\SuperCapacitor2\Codes\SC_Cube
Toolchain / IDE	MDK-ARM V5
Firmware Package Name and Version	STM32Cube FW_F1 V1.8.0

### 5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy all used libraries into the project folder
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No

## 6. Power Consumption Calculator report

### 6.1. Microcontroller Selection

Series	STM32F1
Line	STM32F103
MCU	STM32F103C8Tx
Datasheet	13587_Rev17

### 6.2. Parameter Selection

Temperature	25
Vdd	3.3

## 7. IPs and Middleware Configuration

### 7.1. ADC1

mode: IN3

mode: IN6

mode: IN7

mode: IN8

mode: IN9

mode: Temperature Sensor Channel

#### 7.1.1. Parameter Settings:

##### ADCs\_Common\_Settings:

Mode	Independent mode
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##### ADC\_Settings:

Data Alignment	Right alignment
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Scan Conversion Mode	Disabled
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Continuous Conversion Mode	Disabled
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Discontinuous Conversion Mode	Disabled
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##### ADC\_Regular\_ConversionMode:

Enable Regular Conversions	Enable
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Number Of Conversion	1
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External Trigger Conversion Source	Regular Conversion launched by software
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<u>Rank</u>	1
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Channel	Channel 3
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Sampling Time	1.5 Cycles
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##### ADC\_Injected\_ConversionMode:

Number Of Conversions	0
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##### WatchDog:

Enable Analog WatchDog Mode	false
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### 7.2. ADC2

mode: IN3

mode: IN6

mode: IN7

mode: IN8

mode: IN9



### 7.2.1. Parameter Settings:

#### ADCs\_Common\_Settings:

Mode Independent mode

#### ADC\_Settings:

Data Alignment Right alignment

Scan Conversion Mode Disabled

Continuous Conversion Mode Disabled

Discontinuous Conversion Mode Disabled

#### ADC\_Regular\_ConversionMode:

Enable Regular Conversions Enable

Number Of Conversion 1

External Trigger Conversion Source Regular Conversion launched by software

Rank 1

Channel **Channel 7 \***

Sampling Time 1.5 Cycles

#### ADC\_Injected\_ConversionMode:

Number Of Conversions 0

#### WatchDog:

Enable Analog WatchDog Mode false

## 7.3. CAN

### mode: Mode

### 7.3.1. Parameter Settings:

#### Bit Timings Parameters:

Prescaler (for Time Quantum) 16

Time Quantum **2000.0 \***

Time Quanta in Bit Segment 1 1 Time

Time Quanta in Bit Segment 2 1 Time

Time for one Bit **6000 \***

ReSynchronization Jump Width 1 Time

#### Basic Parameters:

Time Triggered Communication Mode Disable

Automatic Bus-Off Management Disable

Automatic Wake-Up Mode Disable

No-Automatic Retransmission Disable

Receive Fifo Locked Mode Disable

Transmit Fifo Priority                      Disable

**Advanced Parameters:**

Operating Mode                              Normal

## 7.4. RCC

### High Speed Clock (HSE): Crystal/Ceramic Resonator

#### 7.4.1. Parameter Settings:

**System Parameters:**

VDD voltage (V)                              3.3  
Prefetch Buffer                                Enabled  
Flash Latency(WS)                            0 WS (1 CPU cycle)

**RCC Parameters:**

HSI Calibration Value                        16  
HSE Startup Timeout Value (ms)            100  
LSE Startup Timeout Value (ms)            5000

## 7.5. SYS

### Debug: Serial Wire

Timebase Source: SysTick

## 7.6. TIM2

Channel1: PWM Generation CH1

Channel2: PWM Generation CH2

Channel3: PWM Generation CH3

Channel4: PWM Generation CH4

#### 7.6.1. Parameter Settings:

**Counter Settings:**

Prescaler (PSC - 16 bits value)            0  
Counter Mode                                  Up  
Counter Period (AutoReload Register - 16 bits value )    **1800 \***  
Internal Clock Division (CKD)              No Division  
auto-reload preload                          Disable

**Trigger Output (TRGO) Parameters:**

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

#### PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (16 bits value)	<b>900 *</b>
Fast Mode	Disable
CH Polarity	High

#### PWM Generation Channel 2:

Mode	PWM mode 1
Pulse (16 bits value)	<b>1800 *</b>
Fast Mode	Disable
CH Polarity	High

#### PWM Generation Channel 3:

Mode	PWM mode 1
Pulse (16 bits value)	<b>1800 *</b>
Fast Mode	Disable
CH Polarity	High

#### PWM Generation Channel 4:

Mode	PWM mode 1
Pulse (16 bits value)	<b>900 *</b>
Fast Mode	Disable
CH Polarity	High

## 7.7. USART1

### Mode: Asynchronous

#### 7.7.1. Parameter Settings:

##### Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

##### Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples

**\* User modified value**

## 8. System Configuration

### 8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PA3	ADC1_IN3	Analog mode	n/a	n/a	VVOUT
	PA6	ADC1_IN6	Analog mode	n/a	n/a	VVIN
	PA7	ADC1_IN7	Analog mode	n/a	n/a	VILIM1
	PB0	ADC1_IN8	Analog mode	n/a	n/a	VVCAP
	PB1	ADC1_IN9	Analog mode	n/a	n/a	VILIM2
ADC2	PA3	ADC2_IN3	Analog mode	n/a	n/a	VVOUT
	PA6	ADC2_IN6	Analog mode	n/a	n/a	VVIN
	PA7	ADC2_IN7	Analog mode	n/a	n/a	VILIM1
	PB0	ADC2_IN8	Analog mode	n/a	n/a	VVCAP
	PB1	ADC2_IN9	Analog mode	n/a	n/a	VILIM2
CAN	PA11	CAN_RX	Input mode	No pull-up and no pull-down	n/a	
	PA12	CAN_TX	Alternate Function Push Pull	n/a	High *	
RCC	PD0-OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	
	PD1-OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
SYS	PA13	SYS_JTMS-SWDIO	n/a	n/a	n/a	
	PA14	SYS_JTCK-SWCLK	n/a	n/a	n/a	
TIM2	PA0-WKUP	TIM2_CH1	Alternate Function Push Pull	n/a	Low	VPWM1
	PA1	TIM2_CH2	Alternate Function Push Pull	n/a	Low	IPWM1
	PB10	TIM2_CH3	Alternate Function Push Pull	n/a	Low	IPWM2
	PB11	TIM2_CH4	Alternate Function Push Pull	n/a	Low	VPWM2
USART1	PA9	USART1_TX	Alternate Function Push Pull	n/a	High *	
	PA10	USART1_RX	Input mode	No pull-up and no pull-down	n/a	
GPIO	PC14-OSC32_IN	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LEDB1
	PC15-OSC32_OUT	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	KEY1
	PB12	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	PG1
	PB13	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	EN1
	PB14	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	PG2
	PB15	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	EN2
	PA8	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	POWEROUT1_CTRL



## 8.2. DMA configuration

DMA request	Stream	Direction	Priority
ADC1	DMA1_Channel1	Peripheral To Memory	Low

### ADC1: DMA1\_Channel1 DMA request Settings:

Mode: Normal  
Peripheral Increment: Disable  
Memory Increment: **Enable \***  
Peripheral Data Width: Half Word  
Memory Data Width: Half Word

### 8.3. NVIC configuration

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Prefetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
DMA1 channel1 global interrupt	true	0	0
PVD interrupt through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
ADC1 and ADC2 global interrupts	unused		
USB high priority or CAN TX interrupts	unused		
USB low priority or CAN RX0 interrupts	unused		
CAN RX1 interrupt	unused		
CAN SCE interrupt	unused		
TIM2 global interrupt	unused		
USART1 global interrupt	unused		

\* User modified value



## ***9. Software Pack Report***