CS 303 Logic and Digital System Design Assigned : 01/05/2024
Laboratory Assignment #04 Pre-lab due : 06/05/2024 23:59

A Tally Counter

We would like to design a 2-digit decimal tally counter, which is expected to count the sequence 00-01-02-...-98-99-00-. You are provided with a project template in *Digital* in a file named *lab4pre.zip*. The top design is in *testbench.dig*. When opened, a module named *tally.dig* will be seen along two seven segment displays, and a clock input with 100 Hz frequency. Additionally, two buttons labeled COUNT and RESET are present, which will be used to advance and clear the counter, respectively.

You are expected to place your counter design in *tally.dig*. Inside this module, you are provided with two instances of decimal counters with LOAD0 inputs, which can be used to set the count to 0. Other than the count, you are provided with an EQ9 output, which, implied by the name, indicates that the count has reached 9.

Requirements:

- Full synchronous design: all FFs to be driven with the 100 Hz clock, and no clock gating.
- Full schematic design.

Submit your *tally.dig* which contains your design. Do not change any of the input/output terminals.

In-lab

During the laboratory session, you will export your circuit in *tally.dig* to a verilog file named *tally.v* and place this into a folder contained in *tally.zip*. The .zip file contains all necessary supporting files to test your tally counter on the Tang Nano 9 FPGA board, which will be done during the session. You will also be asked to make some modifications to our design and re-test.

You are advised to try producing *tally.v* before the laboratory session by selecting

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File -> Export -> Export to Verilog
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on *Digital*, and make sure that there are no errors generated.

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