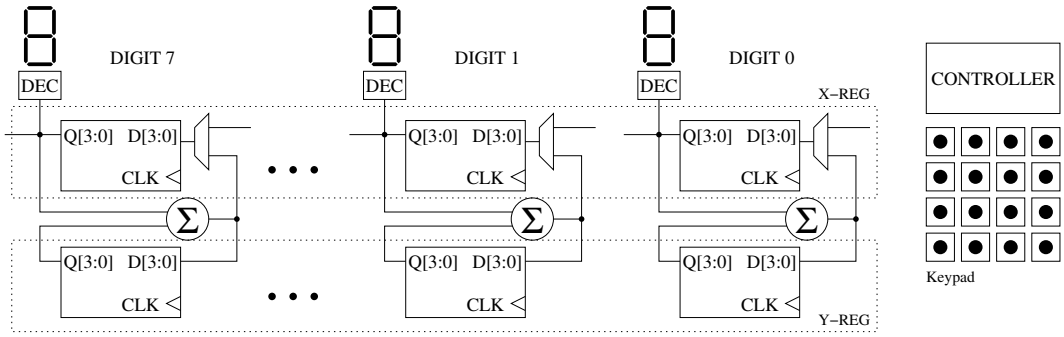
CS 303 Logic and Digital System Design Assigned : 13/05/2024
Term Project Part I Due : 29/05/2024

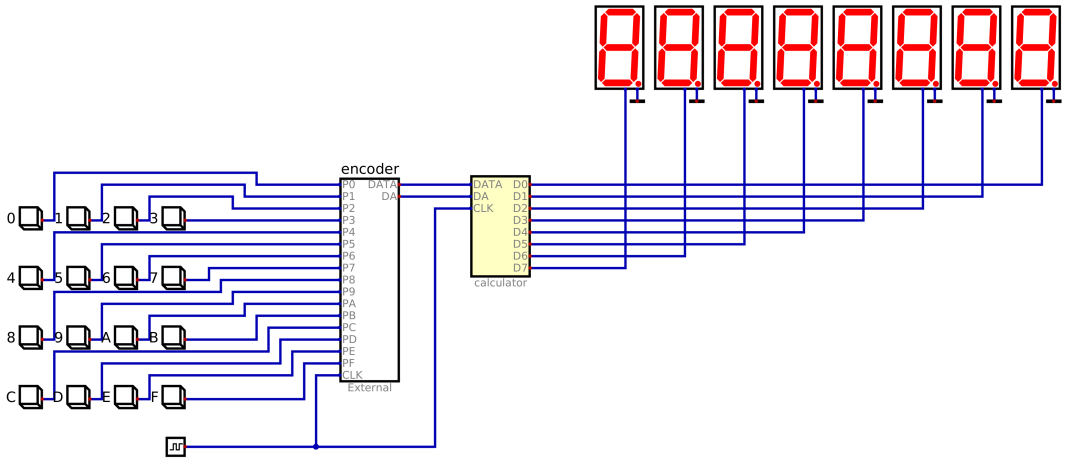
A pocket calculator comprises two registers, named X and Y, each of which are composed of 8 4-bit registers. The X-register is also responsible of maintaining the the display information, while the Y-register acts as an accumulator to perform the transfer operation $Y \leftarrow X + Y$.



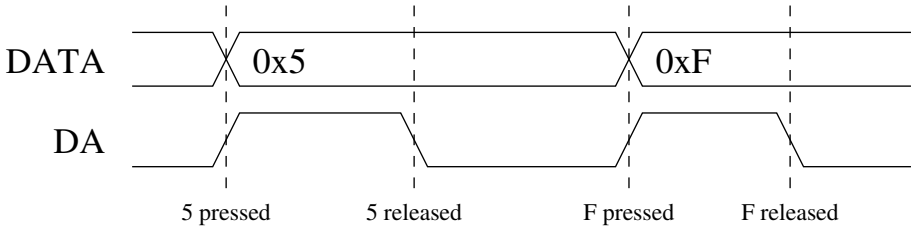
The controller feeds numeric data into the X-register serially. Each time the "+" key is pressed, $X + Y$ is transferred to both registers. The display will continue getting numeric data upon displaying the summation result. Both registers are cleaned when "C" is entered by the user.

PART I

In the first part of the CS303 Term Project, you are asked to perform the schematic design of a simple 8-digit decimal adder and demonstrate its functionality on *Digital*. You will be provided with a template project in *project_template.zip* (with the top level schematic in *project.dig*) that contains 8 seven-segment displays and a hex keypad with the accompanying decoder (in Verilog). Your design is expected to be in *calculator.dig*.



Whenever a key is pressed, the associated key number gets loaded into DATA, while DA remains asserted as long as the key is pressed, as seen in the timing diagram:



Digits “E” and “F” are expected to act as “C” (clear) and “+” inputs for the calculator, respectively. The following behavior is expected:

Key Sequence	Display
C	00000000
1	00000001
3,6	00000136
+	00000136
4,5	00000045
+	00000181
7	00000007
+	00000188
C	00000000
3,3	00000033
+	00000033
1,1	00000011
+	00000044
C	00000000

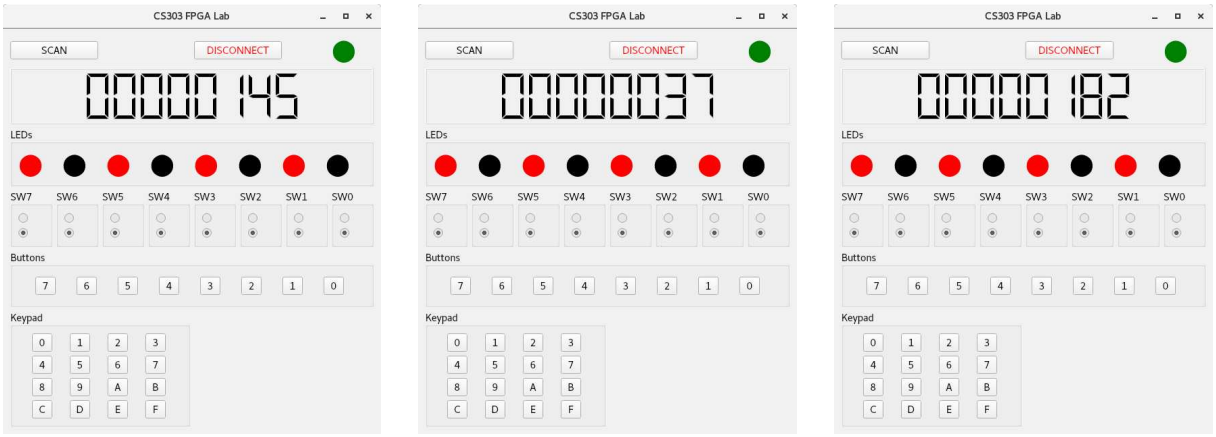
Important notes:

- Each of registers X and Y should contain 4×8=32 bits.
- Full synchronous design: all FFs to be driven with the clock signal, and no clock gating
- Fully schematic design. HDL code is not accepted.
- Work in groups.

At the assigned deadline, return all *.dig* files of your design.

PART II

Export *calculator.dig* into *calculator.v* and synthesize a circuit to run on your FPGA board, using the template project in *calculator.zip*. You will be asked to demonstrate your design at a time which will be announced in due course. A sample run to add 145 and 37 is shown:



Important Note: Avoid using the built-in adder and comparator blocks of *Digital* in your design. They cause some issues during the synthesis.

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