1306160048 Barış Yarar

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-- Company:

-- Engineer:

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-- Create Date: 14:32:27 10/30/2018

-- Design Name:

-- Module Name: module1 - Behavioral

-- Project Name:

-- Target Devices:

-- Tool versions:

-- Description:

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-- Dependencies:

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-- Revision:

-- Revision 0.01 - File Created

-- Additional Comments:

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library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

entity and\_kapisi is

port( and\_g1: in STD\_LOGIC;

and\_g2: in STD\_LOGIC;

and\_cikis: out STD\_LOGIC);

end and\_kapisi;

architecture Behavioral of and\_kapisi is

begin

process(and\_g1,and\_g2)

begin

and\_cikis <= and\_g1 and and\_g2;

end process;

end Behavioral;

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library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

entity or\_kapisi is

port( or\_g1: in STD\_LOGIC;

or\_g2: in STD\_LOGIC;

or\_cikis: out STD\_LOGIC);

end or\_kapisi;

architecture Behavioral of or\_kapisi is

begin

process(or\_g1,or\_g2)

begin

or\_cikis <= or\_g1 or or\_g2;

end process;

end Behavioral;

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library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

entity not\_kapisi is

port( not\_g: in STD\_LOGIC;

not\_cikis: out STD\_LOGIC);

end not\_kapisi;

architecture Behavioral of not\_kapisi is

begin

process(not\_g)

begin

not\_cikis <= not(not\_g);

end process;

end Behavioral;

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library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

entity nor\_kapisi is

port( nor\_g1: in STD\_LOGIC;

nor\_g2: in STD\_LOGIC;

nor\_cikis: out STD\_LOGIC);

end nor\_kapisi;

architecture Behavioral of nor\_kapisi is

begin

process(nor\_g1,nor\_g2)

begin

nor\_cikis <= not(nor\_g1 or nor\_g2);

end process;

end Behavioral;

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library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

entity nand\_kapisi is

port( nand\_g1: in STD\_LOGIC;

nand\_g2: in STD\_LOGIC;

nand\_cikis: out STD\_LOGIC);

end nand\_kapisi;

architecture Behavioral of nand\_kapisi is

begin

process(nand\_g1,nand\_g2)

begin

nand\_cikis <= not(nand\_g1 or nand\_g2);

end process;

end Behavioral;

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library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

entity YT is

port( X: in STD\_LOGIC;

Y: in STD\_LOGIC;

Z: in STD\_LOGIC;

F: out STD\_LOGIC);

end YT;

architecture Behavioral of YT is

component not\_kapisi is

port( not\_g: in STD\_LOGIC;

not\_cikis: out STD\_LOGIC);

end component;

component and\_kapisi is

port( and\_g1: in STD\_LOGIC;

and\_g2: in STD\_LOGIC;

and\_cikis: out STD\_LOGIC);

end component;

component nand\_kapisi is

port( nand\_g1: in STD\_LOGIC;

nand\_g2: in STD\_LOGIC;

nand\_cikis: out STD\_LOGIC);

end component;

component nor\_kapisi is

port( nor\_g1: in STD\_LOGIC;

nor\_g2: in STD\_LOGIC;

nor\_cikis: out STD\_LOGIC);

end component;

component or\_kapisi is

port( or\_g1: in STD\_LOGIC;

or\_g2: in STD\_LOGIC;

or\_cikis: out STD\_LOGIC);

end component;

signal ara1: STD\_LOGIC;

signal ara2: STD\_LOGIC;

signal ara3: STD\_LOGIC;

signal ara4: STD\_LOGIC;

signal ara5: STD\_LOGIC;

signal ara6: STD\_LOGIC;

signal ara7: STD\_LOGIC;

signal ara8: STD\_LOGIC;

begin

blok1: not\_kapisi port map(not\_g=>X,not\_cikis=>ara1);

blok2: or\_kapisi port map(or\_g1=>ara1, or\_g2=>Y, or\_cikis=>ara2);

block4: not\_kapisi port map(not\_g=>Z,not\_cikis=>ara3);

block5: and\_kapisi port map(and\_g1=>X, and\_g2=> ara3, and\_cikis=>ara4);

blok3: nor\_kapisi port map(nor\_g1=>Y, nor\_g2=>ara4, nor\_cikis => ara5);

block6: and\_kapisi port map(and\_g1=>ara2, and\_g2=> ara5, and\_cikis=>ara6); -------en son işleme ara 6 gidecek-----

block7: nand\_kapisi port map(nand\_g1 => Y, nand\_g2=> Z, nand\_cikis=>ara7);

block8: and\_kapisi port map(and\_g1=>ara7, and\_g2=> X, and\_cikis=>ara8); ----en son işleme girecek ara8----

block9: or\_kapisi port map(or\_g1=>ara8, or\_g2=>ara6, or\_cikis=>F);

end Behavioral;



