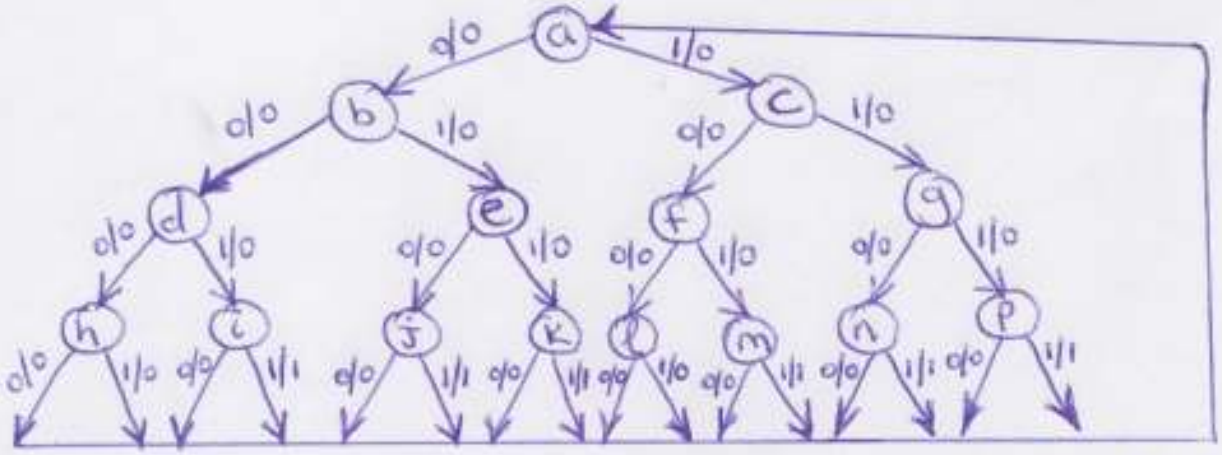
Example: A single-input single-output clocked sequential circuit is to be designed. The circuit will determine whether a string of four consecutive input bits constitute a valid BCD code or not. The output $\underline{Z=1}$ if the four consecutive bits $\underline{\text{DO NOT}}$ constitute a valid BCD representation, and $Z=0$ otherwise. Least significant bit of the BCD code is applied to the checker input first.

X → [BCD checker] → Z (after the 4th input)



PS	NS x=0	NS x=1	Output x=0	Output x=1
a	b	c	0	0
b	d	e	0	0
c	f	g	0	0
d	h	i	0	0
e	j	k	0	0
f	l	m	0	0
g	n	p	0	0
h	a	a	0	0
i	a	a	0	1
j	a	a	0	1
k	a	a	0	1
l	a	a	0	0
m	a	a	0	1
n	a	a	0	1
p	a	a	0	1

— State table —

$P_1 = (a,b,c,d,e,f,g,h,l)\ (i,j,k,m,n,p)$

$P_2 = (a,b,c,h,l)(d,f)\ (e,g)(i,j,k,m,n,p)$

$P_3 = (a,h,l)(b,c)(d,f)\ (e,g)(i,j,k,m,n,p)$

$P_4 = (a)(h,l)(b,c)(d,f)(e,g)(i,j,k,m,n,p)$

PS	NS x=0	NS x=1	Output x=0	Output x=1
a	b	b	0	0
b	d	e	0	0
d	h	i	0	0
e	i	i	0	0
h	a	a	0	0
i	a	a	0	1

— Reduced state table —

⇒ h, i must be adjacent
d, e may be adjacent

	00	01	11	10
0	h	d	b	a
1	i	e	–	–

h ≡ 000 i ≡ 100
d ≡ 001 e ≡ 101
a ≡ 010
b ≡ 011

PS	NS		Output	
	X=0	X=1	X=0	X=1
ABC	ABC	ABC	z	z
h → 000	010	010	0	0
d → 001	000	100	0	0
a → 010	011	011	0	0
b → 011	001	101	0	0
i → 100	010	010	0	1
e → 101	100	100	0	0

6 states ⇒ 3 FFs

3 FFs ⇒ 8 states

$2^3 = 8$

∴ 2 unused states: 110 and 111

Design the circuit using one JK FF for A, one RS FF for B and one T FF for C.

PS	Input	NS	Output	Flip-flop Inputs				
ABC	X	ABC	z	JA	KA	SB	RB	TC
000	0	010	0	0	X	1	0	0
000	1	010	0	0	X	1	0	0
001	0	000	0	0	X	0	X	1
001	1	100	0	1	X	0	X	1
010	0	011	0	0	X	X	0	1
010	1	011	0	0	X	X	0	1
011	0	001	0	0	X	0	1	0
011	1	101	0	1	X	0	1	0
100	0	010	0	X	1	1	0	0
100	1	010	1	X	1	1	0	0
101	0	100	0	X	0	0	X	1
101	1	100	0	X	0	0	X	1
110	0	xxx	x	x	x	x	x	x
110	1	xxx	x	x	x	x	x	x
111	0	xxx	x	x	x	x	x	x
111	1	xxx	x	x	x	x	x	x

— Excitation Table —

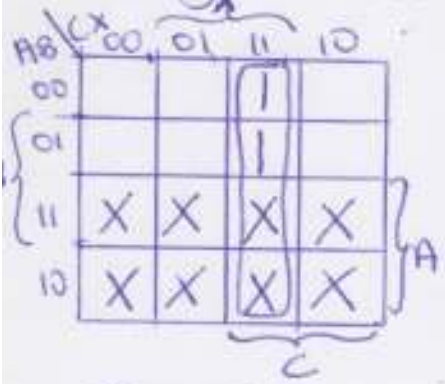
Remember:

PS	NS	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

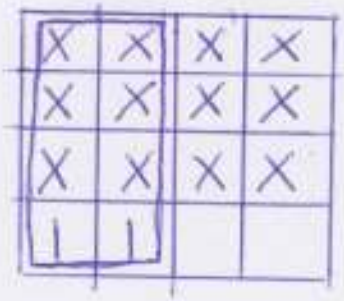
PS	NS	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

PS	NS	T
0	0	0
0	1	1
1	0	1
1	1	0

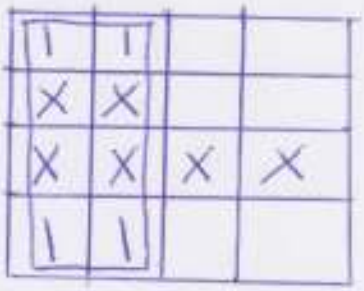
Using the K-map simplification;



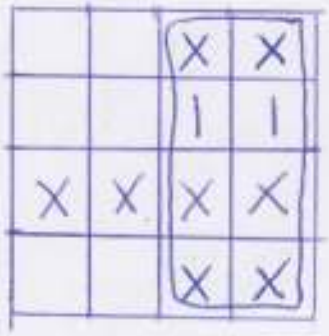
$J_A = CX$



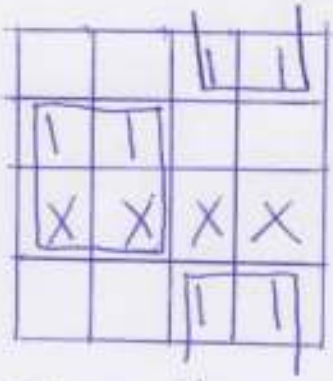
$K_A = C'$



$S_B = C'$



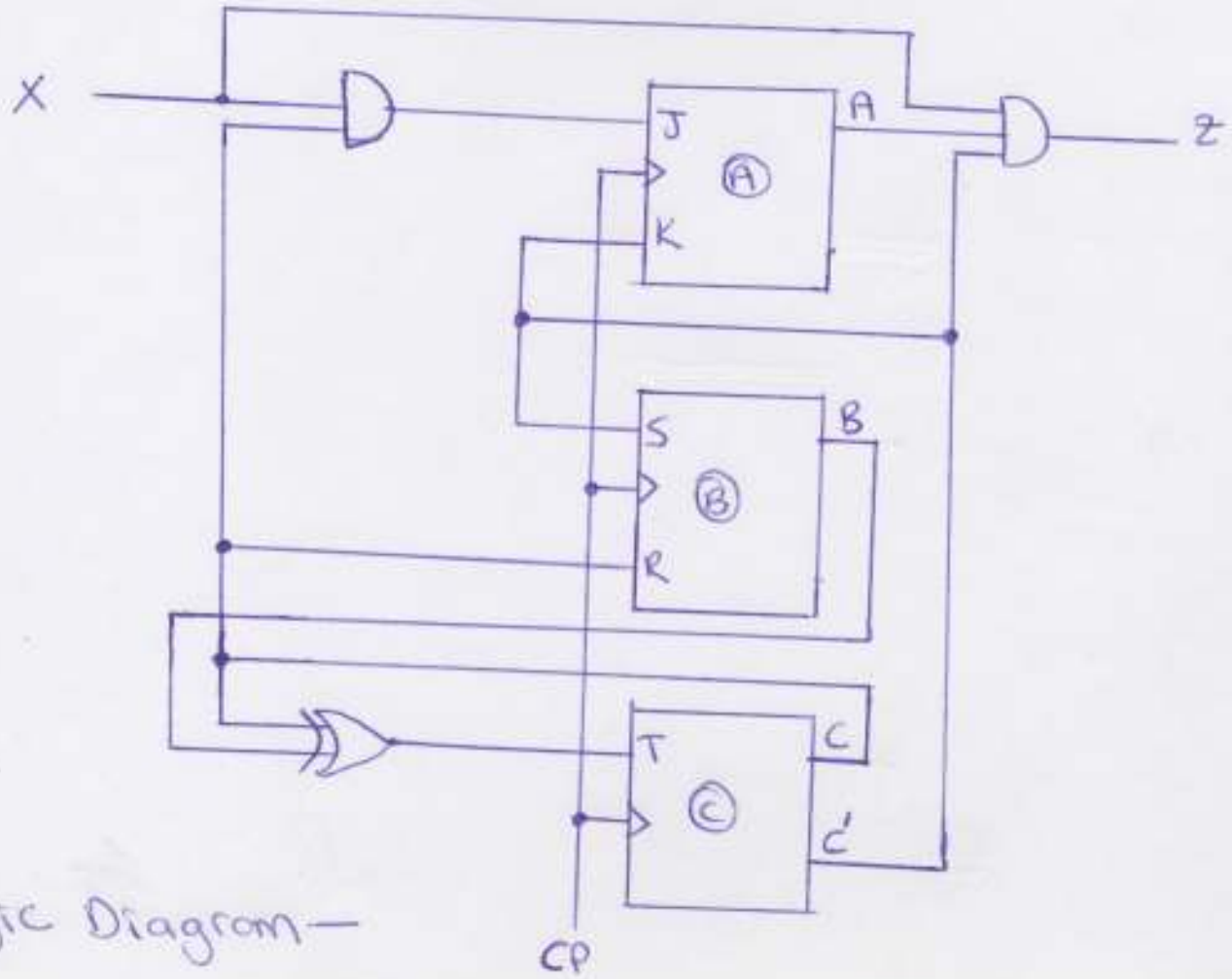
$R_B = C$



$T_C = B'C + BC'$

$= B \oplus C$

$Z = AC'X$



— Logic Diagram —

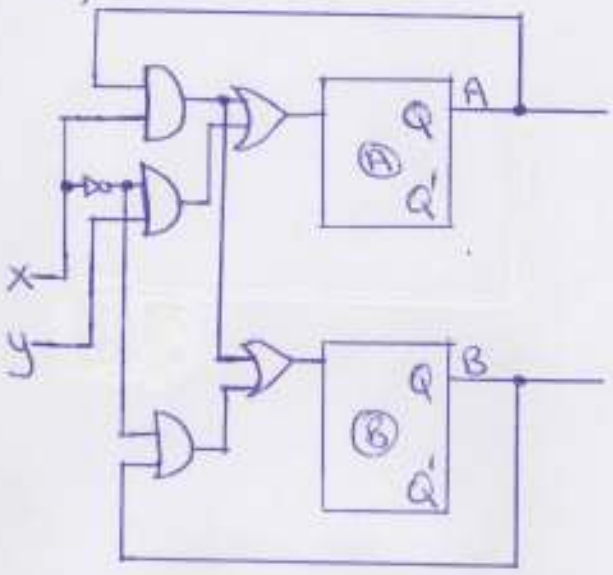
Example: A sequential circuit with two D flip-flops, A and B; two inputs, x and y; and one output, z, is specified by the following next-state and output equations:

$$A(t+1) = x'y + xA \quad , \quad B(t+1) = x'B + xA \qquad z = B$$

a) Draw the logic diagram of the circuit
b) Derive the state table
c) Derive the state diagram

Solution:

a)



b)

A(t+1):

xy \ AB	00	01	11	10
00				
01	1	1	1	1
11			1	1
10			1	1

(y: 01, 11, 10; x; B)

B(t+1):

xy \ AB				
		1	1	
		1	1	
			1	1
			1	1

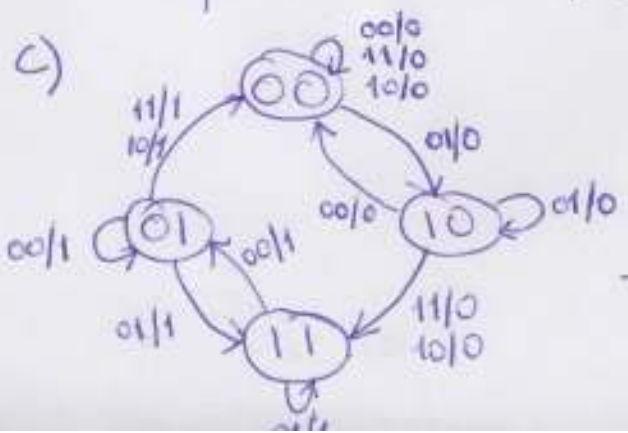
z:

xy \ AB				
	1	1		
	1	1		
	1	1		
	1	1		

PS	NS				Output			
	xy=00	01	11	10	00	01	11	10
AB	AB	AB	AB	AB	z	z	z	z
00	00	10	00	00	0	0	0	0
01	01	11	00	00	1	1	1	1
11	01	11	11	11	1	1	1	1
10	00	10	11	11	0	0	0	0

— State table —

c)



— State diagram —

Example: A sequential circuit has three D flip-flops, A, B, and C, and one input, X. It is described by the following flip-flop input functions:

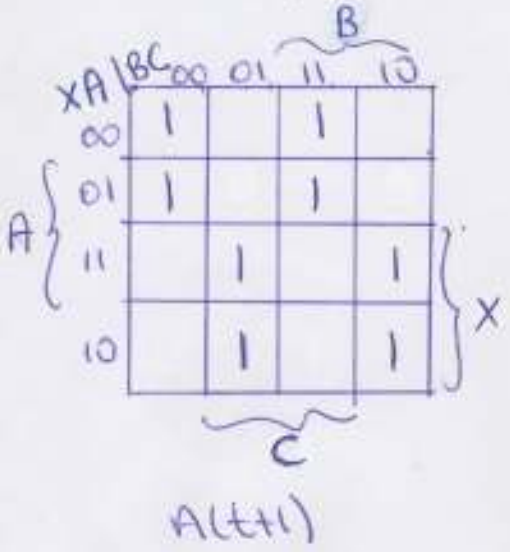
$$D_A = (BC' + B'C)X + (BC + B'C')X'$$
$$D_B = A$$
$$D_C = B$$

a) Derive the state table

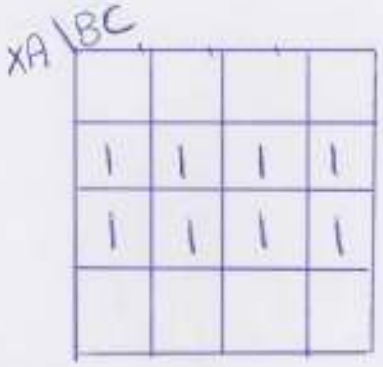
b) Draw two state diagrams: one for x=0 and the other for x=1

a) Next state equations:

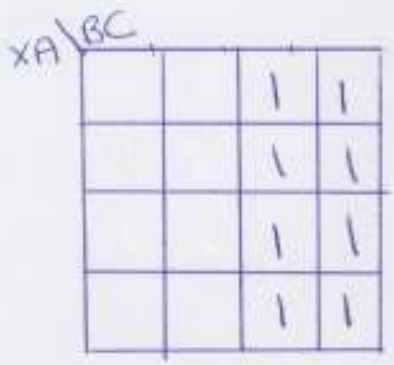
$$A(t+1) = D = XBC' + XB'C + X'BC + X'B'C', \quad B(t+1) = A, \quad C(t+1) = B$$



A(t+1)



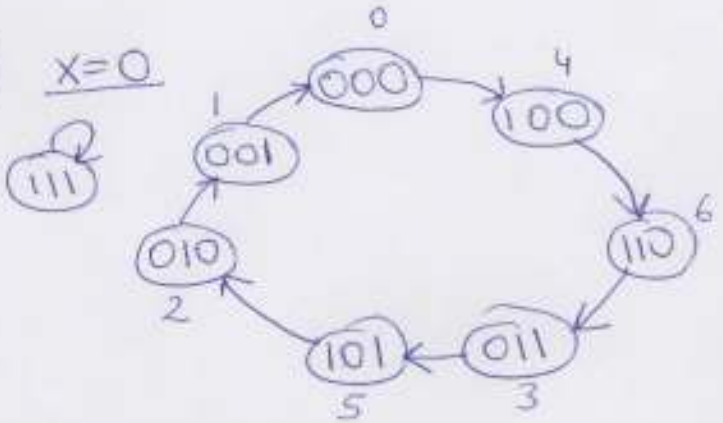
B(t+1)



C(t+1)

PS	NS	
	x=0	x=1
ABC	ABC	ABC
000	100	000
001	000	100
010	001	101
011	101	001
100	110	010
101	010	110
110	011	111
111	111	011

b) x=0



x=1