PARITY GENERATION AND CHECKING

A parity bit is an extra bit included in a binary message to make the *number of 1's* either *odd* or *even*. It is used for detecting errors during transmission of binary information. The parity bit is generated by the transmitter and checked by the receiver for errors.

Ex: Consider a 3-bit message to be transmitted with an even parity bit. Design a 3-bit even parity generator and a 4-bit even parity checker.

Sender site: for even parity, bit *P* must be generated to make the total number of 1's even (including P).

Receiver site: the received four bits must have an even number of 1's. If the received four bits have an odd number of 1's an error occurs. In case of error, the output of the parity checker is 1.

ANALYSIS PROCEDURE OF COMBINATIONAL LOGIC CIRCUITS

The analysis procedure for a combinational logic circuit starts with a given logic diagram and ends with a set of Boolean functions, a truth table, or, an explanation of the circuit operation. The analysis procedure comprises the following steps:

1. Label the logic gate outputs with different symbols.
2. Determine the Boolean functions for each gate output.
3. Use algebraic manipulation or truth table to obtain the output Boolean functions in terms of input variables.

Ex: Analyse the combinational circuit shown below. Find the Boolean functions for the two outputs as a function of the three inputs and explain the circuit operation.