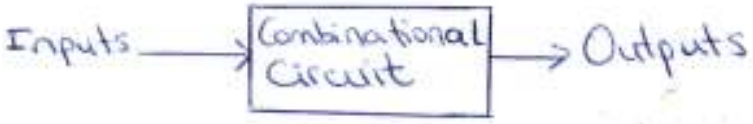
Logic Circuits

- Combinational Circuits
- Sequential Circuits

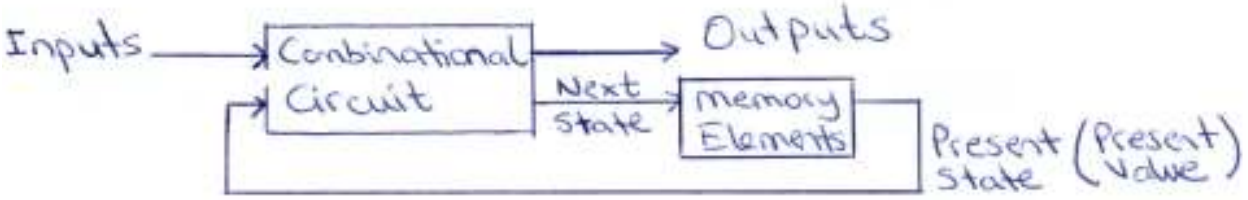


* Outputs depend only on the present inputs.

  Outputs = f(external inputs)

Sequential Circuits

- Consists of a <u>combinational circuit</u> and <u>memory elements</u> which are connected to form a feedback path



- The memory elements are devices capable of storing binary information (0 or 1) within them. The binary information stored in the memory elements at any given time defines the state of the sequential circuit.

* Outputs depend not only its present inputs, but also on the past inputs.

  Outputs = f(external inputs, present state (of the memory elements))

  Next State (of the memory elements) = f(external inputs, present state (of the memory elements))

- A sequential circuit is specified by a time sequence of inputs, outputs and internal states.

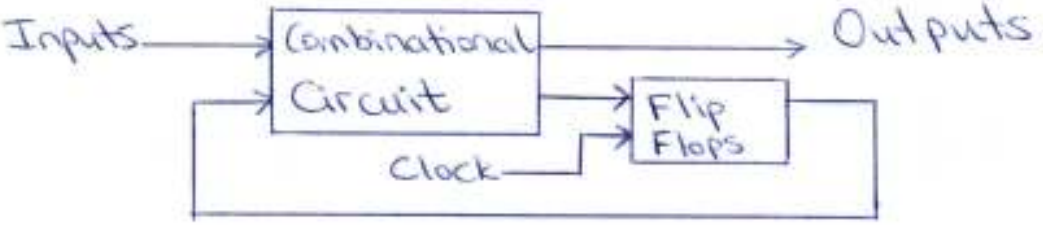
There are two main types of sequential circuits:

1- Synchronous Sequential Circuits
State of the circuit changes at discrete instants of time depending on a synchronizing <u>clock pulse</u> (⎍).

2- Asynchronous Sequential Circuits
State of the circuit can change at any instant of time.

— Synchronous (Clocked) Sequential Circuits —

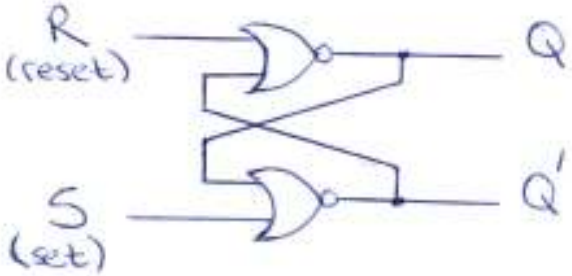
Block diagram of a synchronous sequential circuit is shown below:



* Flip-Flops

The memory elements used in clocked sequential circuits are called flip-flops.

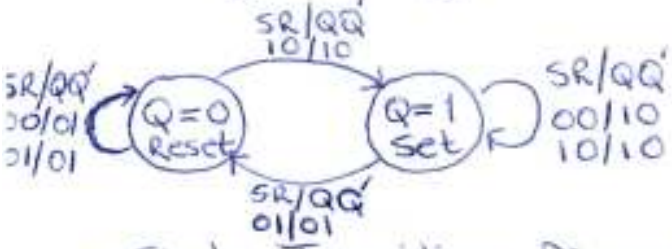
Basic Flip-Flop Circuit with NOR Gates:



— Logic Diagram —

S R	Q Q'	
1 0	1 0	Set
0 0	1 0	(after S=1, R=0)
0 1	0 1	Reset
0 0	0 1	(after S=0, R=1)
1 1	0 0	(Indeterminate)

— Truth Table —

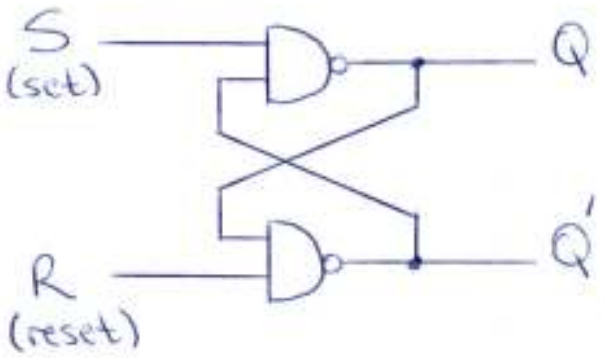


— State Transition Diagram —

* When Q=1 and Q'=0 ⇒ SET state

When Q=0 and Q'=1 ⇒ RESET or CLEAR state

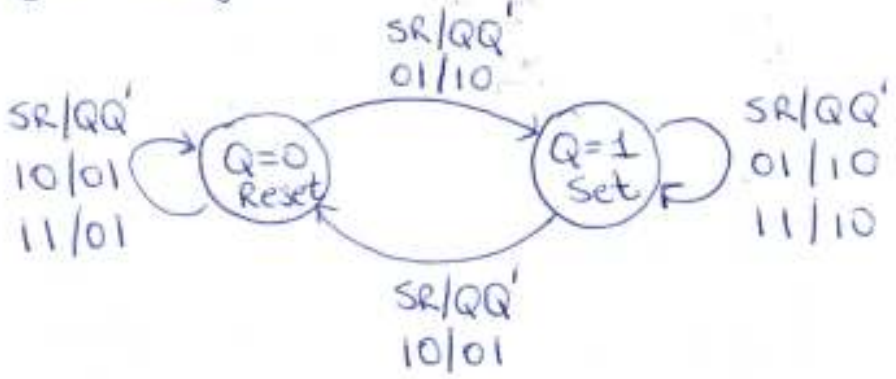
Basic Flip-Flop Circuit with NAND Gates:



- Logic Diagram -

S R	Q Q'	
1 0	0 1	Reset
1 1	0 1	(after S=1, R=0)
0 1	1 0	Set
1 1	1 0	(after S=0, R=1)
0 0	1 1	(Indeterminate)

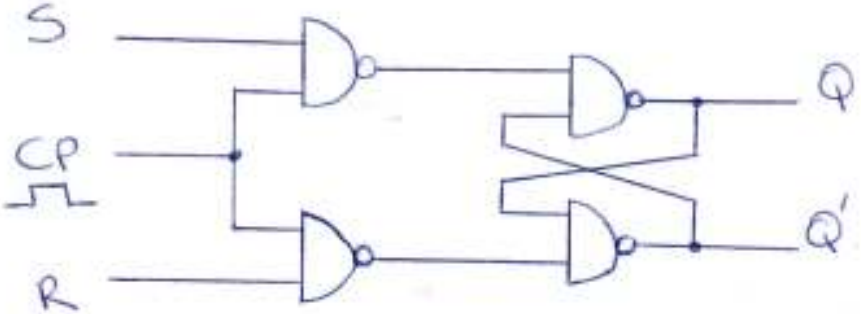
- Truth Table -



- State Transition Diagram -

- The operation of the basic flip-flop can be modified by providing an additional control input that determines when the state of the circuit can be changed.

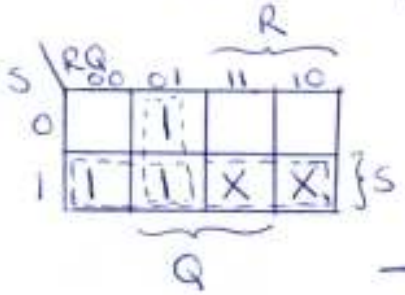
SR Flip-Flop (with a clock pulse):



- Logic Diagram -

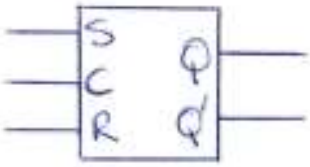
S	R	Q(t)	Q(t+1)	
0	0	0	0	No Change
0	0	1	1	
0	1	0	0	Reset
0	1	1	0	
1	0	0	1	Set
1	0	1	1	
1	1	0	X	Indeterminate (Undefined)
1	1	1	X	

- Characteristic Table -



$Q(t+1) = S + R'Q$
$(SR = 0)$
↳ otherwise indeterminate

- Characteristic Equation -



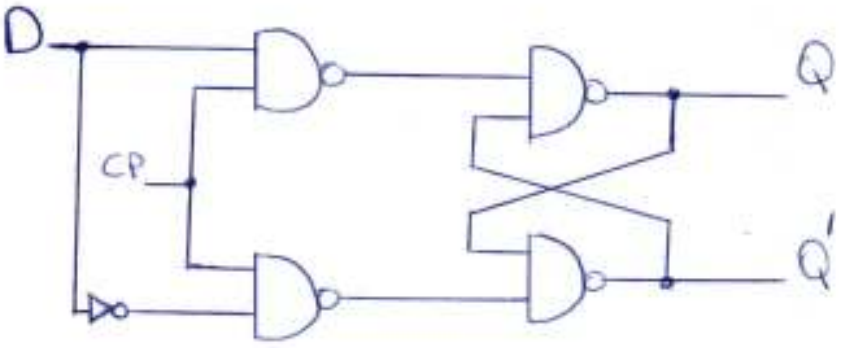
- Graphic Symbol -

S	R	Q(t+1)	
0	0	Q(t)	No change
0	1	0	Reset
1	0	1	Set
1	1	?	Unpredictable

- Characteristic Table of the SR Flip-flop

D Flip-Flop:

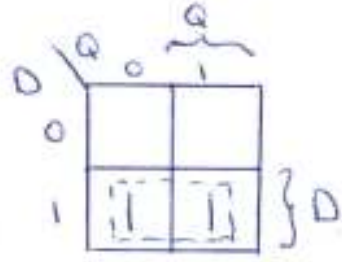
One way to eliminate the undesirable condition of the indeterminate state in the SR flip-flop is to ensure that inputs S and R are never equal to 1 at the same time. This is done in the D flip-flop by applying D input to the input and its complement to the R input.



- Logic Diagram -

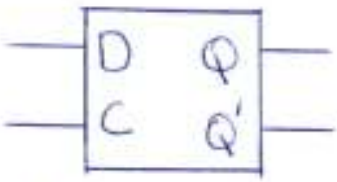
D	Q(t)	Q(t+1)
0	0	0
0	1	0
1	0	1
1	1	1

- Characteristic Table -



$Q(t+1) = D$

- Characteristic Equation -



- Graphic Symbol -

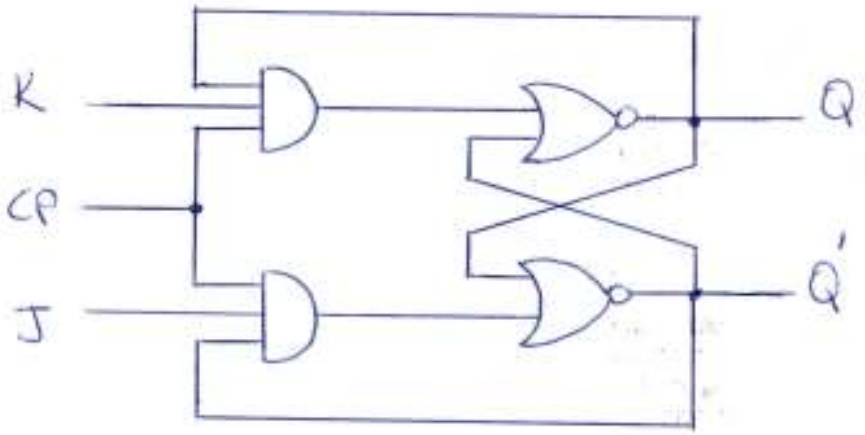
D	Q(t+1)
0	0
1	1

- characteristic Table of the D flip-flop

- As long as CP=0, the circuit cannot change state. When CP=1, the output Q follows the D input (i.e. Q=0 if D=0; and Q=1 if D=1)

JK Flip-Flop:

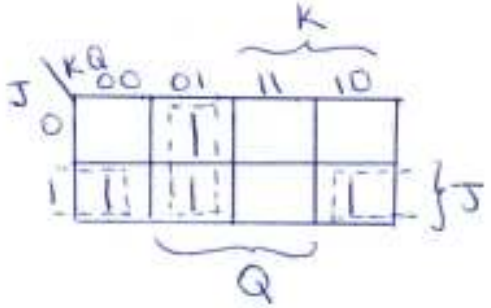
A JK flip-flop is a refinement of the SR flip-flop to eliminate the indeterminate state of the SR type.



- Logic Diagram

J	K	Q(t)	Q(t+1)	
0	0	0	0	No change
0	0	1	1	
0	1	0	0	Reset
0	1	1	0	
1	0	0	1	Set
1	0	1	1	
1	1	0	1	Toggle (Q')
1	1	1	0	

- Characteristic Table -



$$Q(t+1) = JQ' + K'Q$$

- Characteristic Equation -

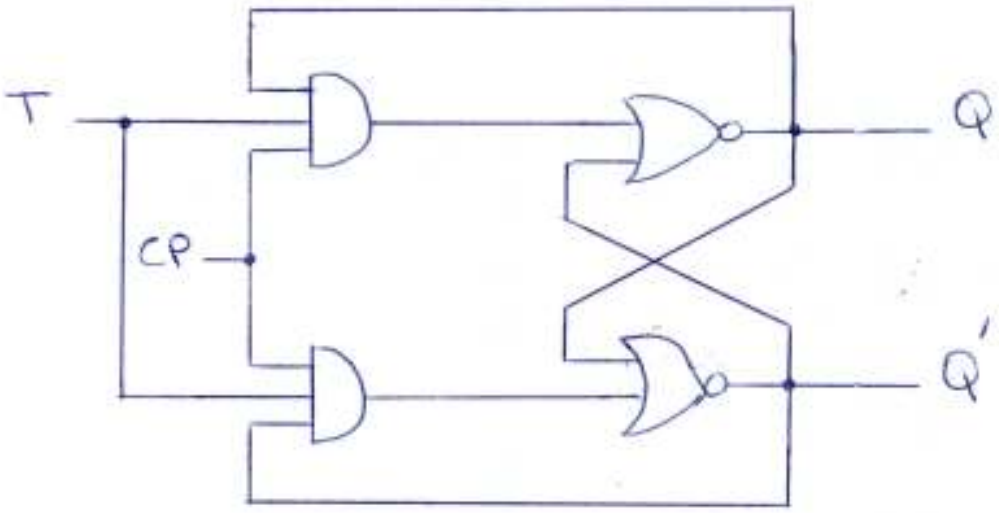
- Graphic Symbol -

J	K	Q(t+1)	
0	0	Q(t)	No change
0	1	0	Reset
1	0	1	Set
1	1	Q'(t)	Toggle (Complement)

- Characteristic Table of the JK Flip-Flop -

T Flip-Flop:

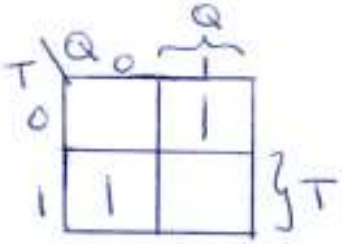
The T flip-flop is a single-input version of the JK flip flop. It is obtained from the JK flip-flop when both inputs are tied together.



- Logic Diagram -

T	Q(t)	Q(t+1)	
0	0	0	No change
0	1	1	
1	0	1	Toggle
1	1	0	

- Characteristic Table -



$$Q(t+1) = TQ' + T'Q$$
$$= T \oplus Q$$

- Characteristic Equation -

- Graphic Symbol -

T	Q(t+1)
0	Q(t) No change
1	Q'(t) Toggle

- Characteristic Table of the T Flip-Flop -

- Regardless of the present state, the T flip-flop complements its output when CP = 1 and T = 1.

In summary;

SR-FF $\Rightarrow$ $Q(t+1) = S + R'Q$

D-FF $\Rightarrow$ $Q(t+1) = D$

JK-FF $\Rightarrow$ $Q(t+1) = JQ' + K'Q$

T-FF $\Rightarrow$ $Q(t+1) = TQ' + T'Q$

You can design and define your own flip-flop:

Example: Design a T-FF using a D-FF and some logic.

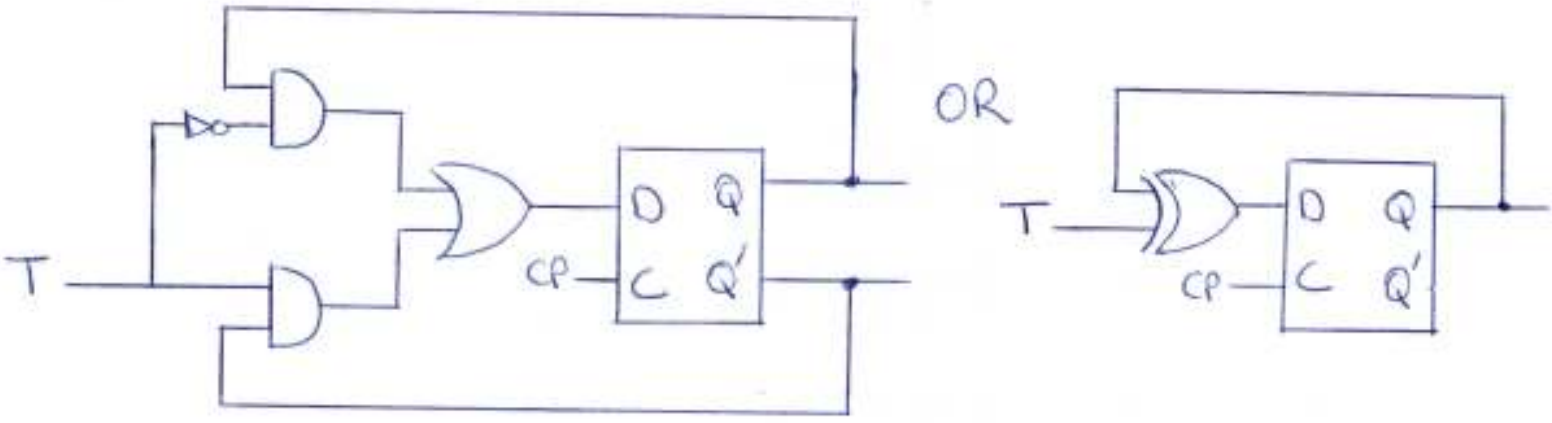
Soln: Remember;

D	Q(t+1)
0	0
1	1

$Q(t+1) = D$

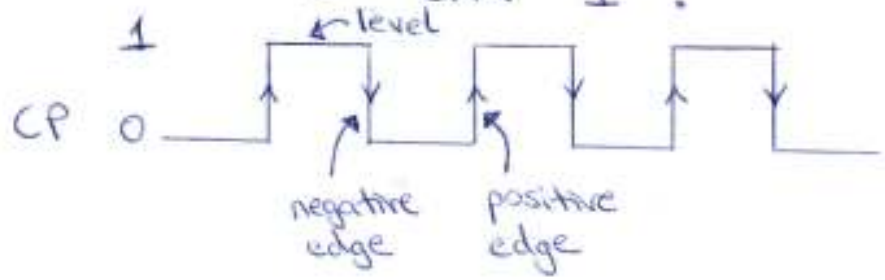
T	Q(t+1)
0	Q(t)
1	Q'(t)

$Q(t+1) = TQ' + T'Q = T \oplus Q$



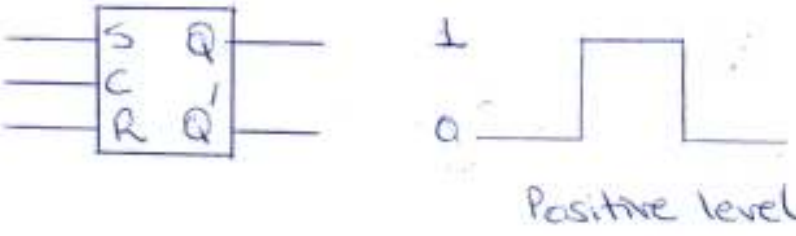
* Triggering of Flip-Flops

The state of a flip-flop is switched by a momentary change in the clock pulse input signal. This momentary change is called a trigger. The clock pulse alternates between "0" and "1".



Level Triggered Flip-Flop:

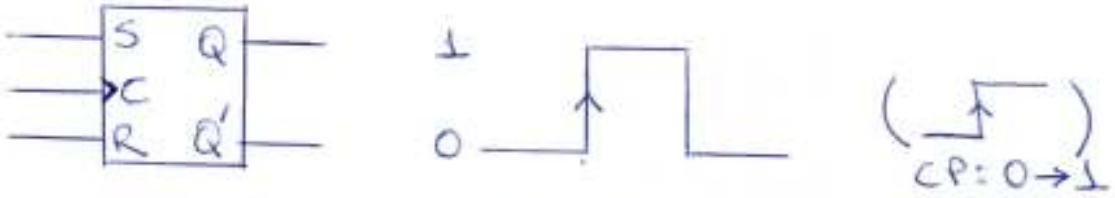
The flip-flop responds to input changes during the entire pulse duration.



Positive level triggered

Positive-Edge Triggered Flip-Flop:

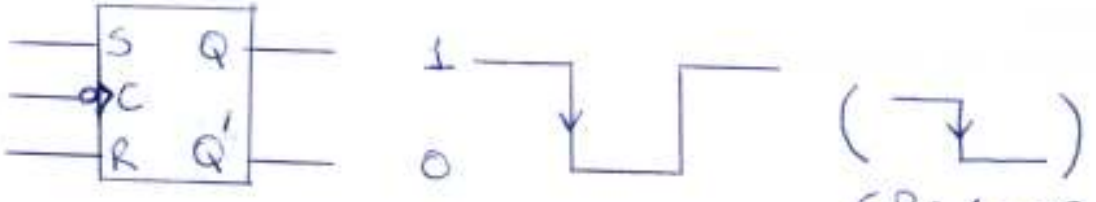
The flip-flop responds to input changes only at the positive edge of the clock pulse.



Positive-edge triggered

Negative-Edge Triggered Flip-Flop:

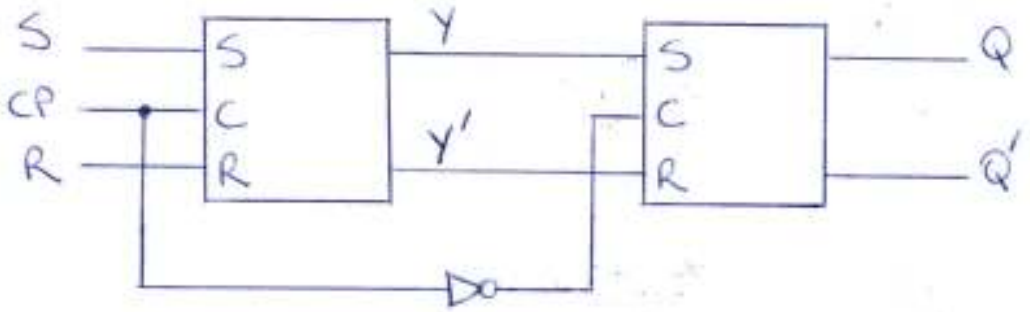
The flip-flop responds to input changes only at the negative edge of the clock pulse.



Negative-edge triggered

Master - Slave Flip-Flop:

A Master - Slave flip-flop is constructed from two flip-flops and an inverter.



S	R	Q(t+1)
0	0	Q(t)
0	1	0
1	0	1
1	1	Indeterminate

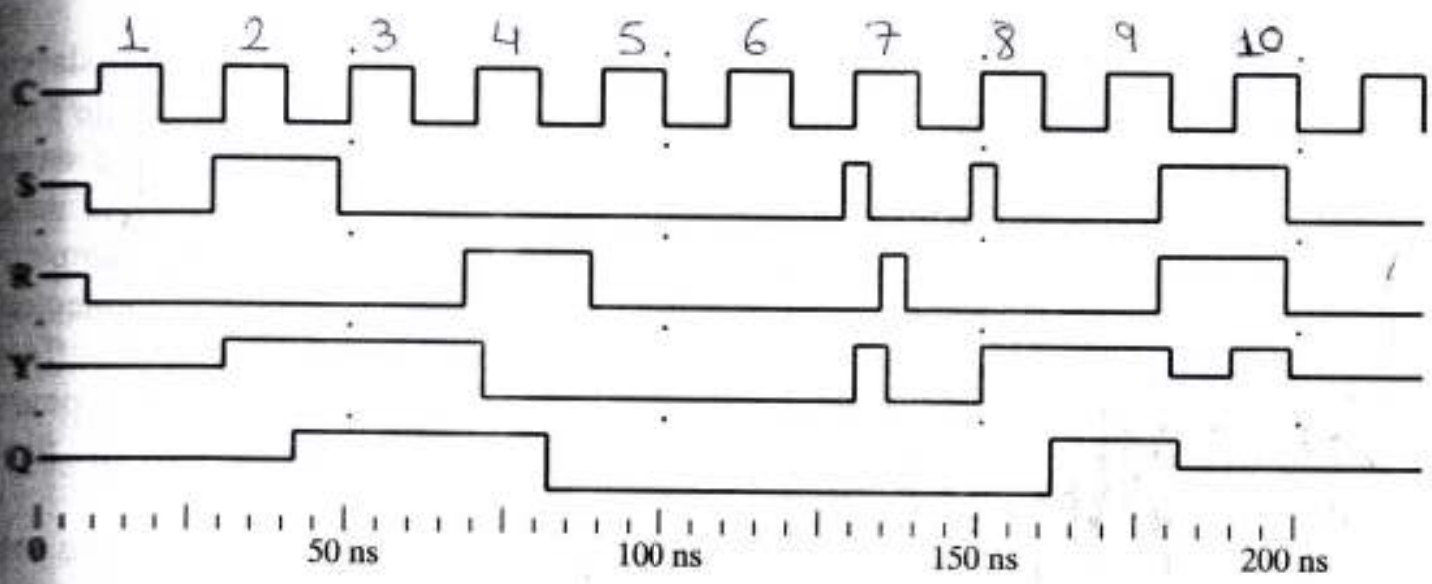
— Logic Diagram of a Master-Slave SR Flip-Flop —

- When CP=0, the slave flip-flop is enabled, and output Q is equal to the master output Y. The master flip-flop is disabled.
- When CP=1, the values on S and R control the value stored in the master flip-flop Y, but cannot affect the slave output Q.

Example: Master - Slave SR flip-flop. Logic simulation is shown in Figure 5-10, page 11.

Truth table of Figure 5-10 is:

CLK	S	R	C	Y	Q	
1-2						

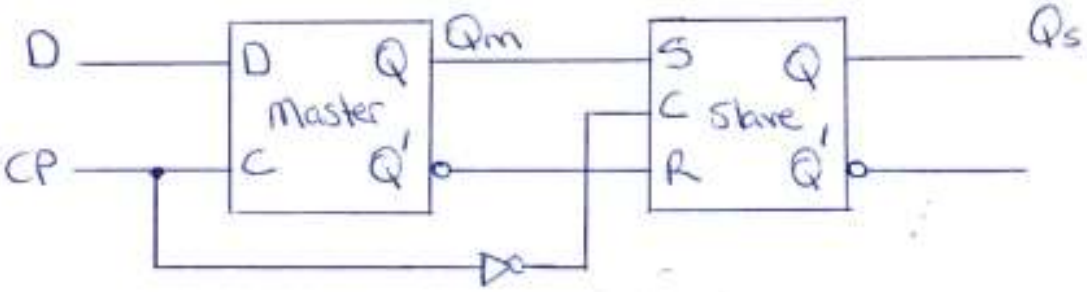


□ **FIGURE 5-10**
Logic Simulation of an *SR* Master–Slave Flip-Flop

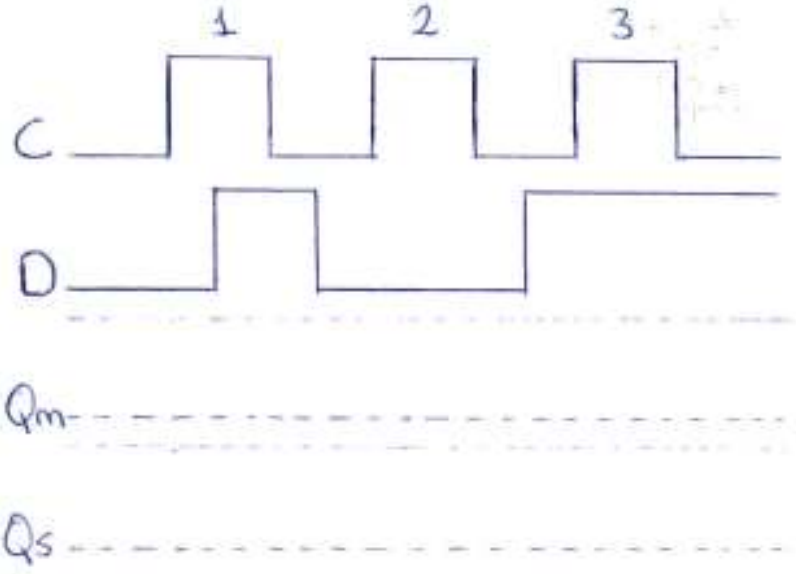
Note that these changes are delayed from the pulse changes by gate delays. Also, the external inputs S and R can change anytime after the clock pulse goes through its negative transition. This is because, as the C input reaches 0, the master is disabled, and S and R have no effect until the next clock pulse.

The next sequence of signal changes illustrates the "1s catching" behavior of the *SR* master–slave flip-flop. A narrow pulse to 1 occurs on S at the beginning of a clock pulse. The master latch responds to the 1 on S by changing Y to 1. Then S goes to 0 and a narrow 1 pulse occurs on R. The master latch responds to the 1 on R by changing Y back to 0. Since there are no further 1 values on S or R, the master continues to store 0, which is copied to the slave latch, changing Q to 0, in response to the clock's change to 0. Thus, the master latch "caught" both the 1 on S and the 1 on R. Since the 1 on R was caught last, the output Q remained at 0. In

Master-Slave D Flip-Flop:



Timing diagram is:

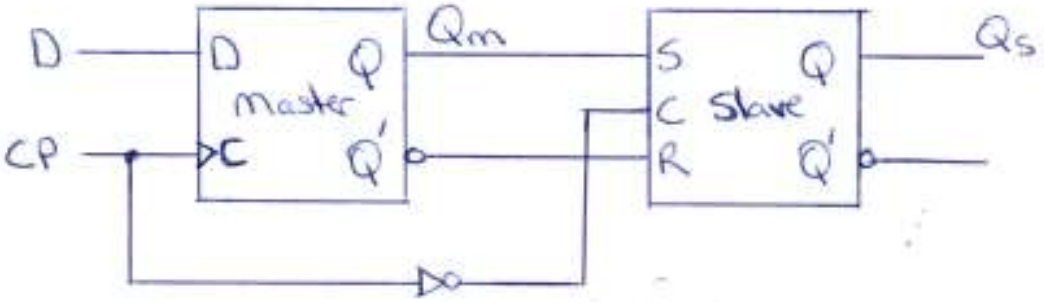


CLK	D	C	Qm	Qs
1.1				
1.2				

Edge-Triggered Flip-Flop:

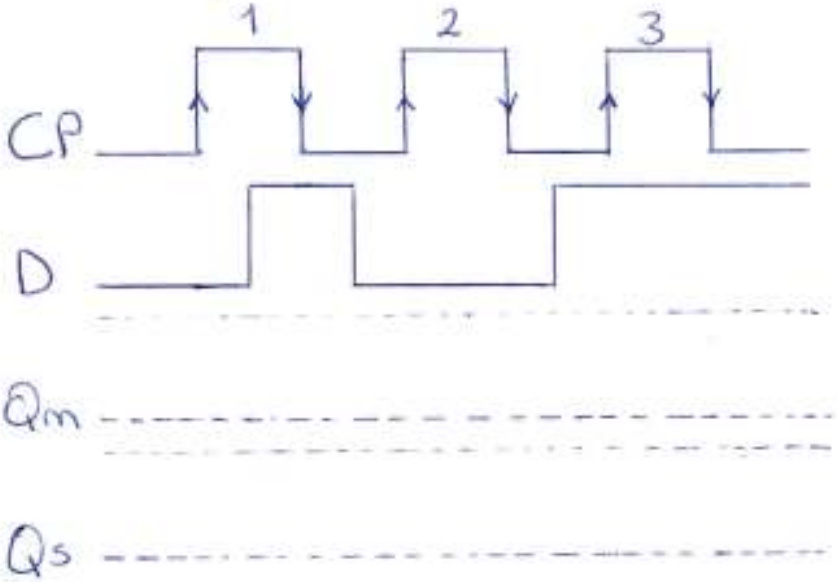
An edge-triggered flip-flop ignores the pulse while it is at a constant level and triggers only during a transition of the clock signal (0→1) or (1→0).

Example: Negative-Edge-Triggered D Flip-Flop.

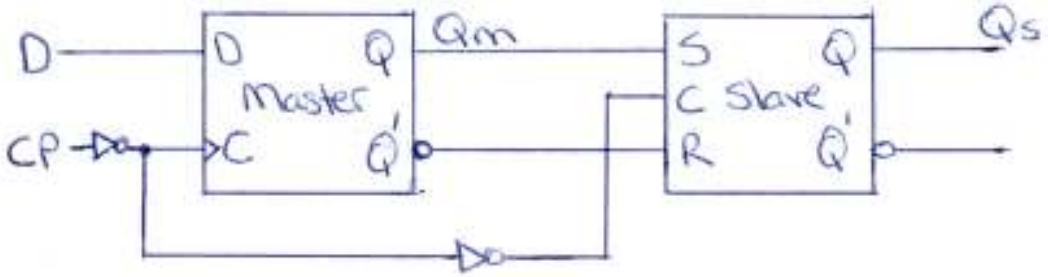


When CP → 1 / 0 ⌐¯|_, the circuit changes it value, Qs.

Timing diagram is:

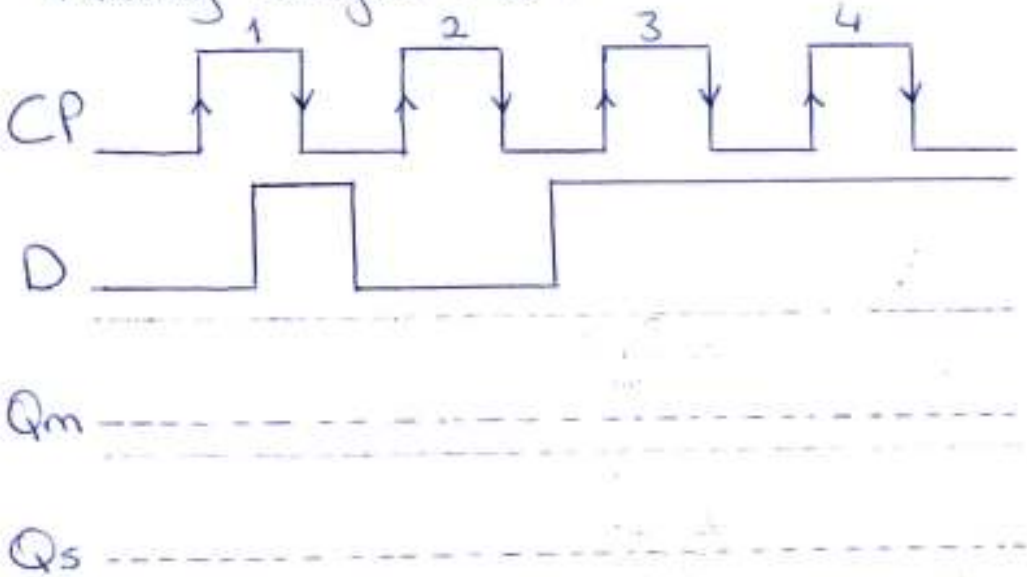


Example: Positive-Edge-Triggered D Flip-Flop.



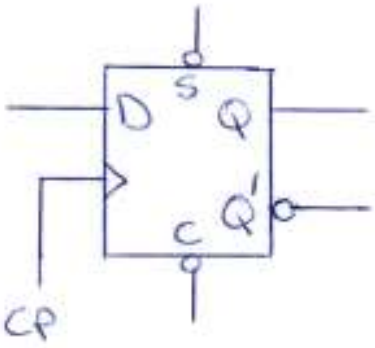
When CP → _|‾|_, the circuit changes its value, Qs.

Timing diagram is:



Direct Inputs:

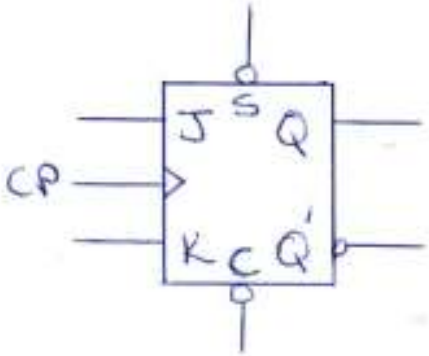
Flip-flops provide two special inputs, set or reset (clear) to force the circuit to an initial state.



- Graphic Symbol -

S	R	CP	D	Q	Q'
0	1	X	X	1	0
1	0	X	X	0	1
0	0	X	X	Undefined	
1	1	↓	0	0	1
1	1	↓	1	1	0

- Function Table -



- Graphic Symbol -

S	R	CP	J	K	Q	Q'
0	1	X	X	X	1	0
1	0	X	X	X	0	1
1	1	X	X	X	Undefined	
1	1	↓	0	0	Q	Q'
1	1	↓	0	1	0	1
1	1	↓	1	0	1	0
1	1	↓	1	1	Q'	Q

- Function Table -