We can observe the first 8 steps below so in simulation scenario we completed “a” to “i”.

a. Reset the circuit

b. Inset the debit card by pressing *BTN3*

c. Enter the password correctly and go to the ATM menu state

d. Go to the money operation state by pressing *BTN3*

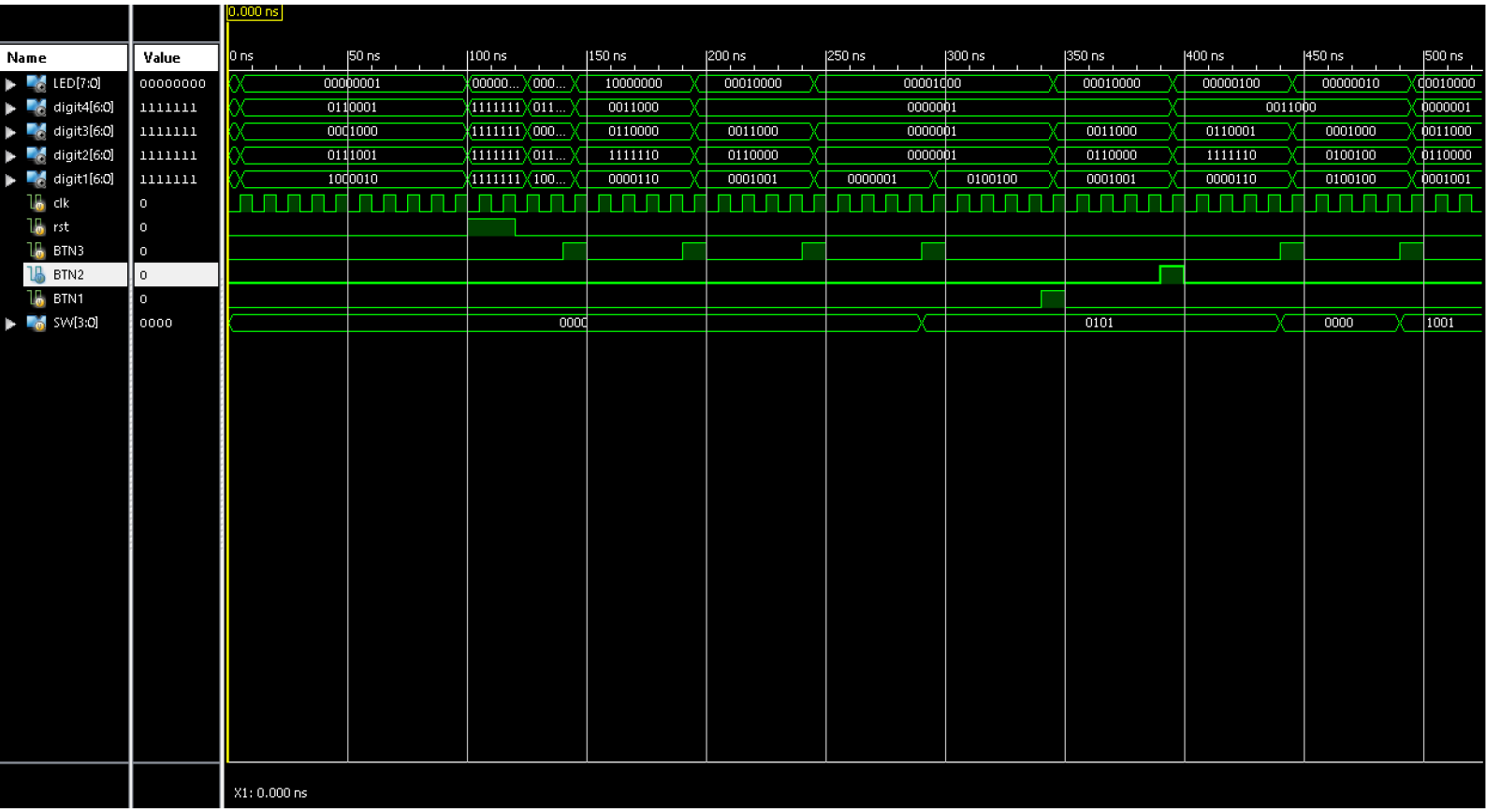
e. Deposit 5 into your account (by setting the *SW* and pressing *BTN3*)

f. Go back to the ATM menu state by pressing *BTN1*

g. Go to password change state by pressing *BTN2*

h. Enter the current password correctly (by setting the *SW* and pressing *BTN3*)

i. Enter the new password (by setting the *SW* and pressing *BTN3*)

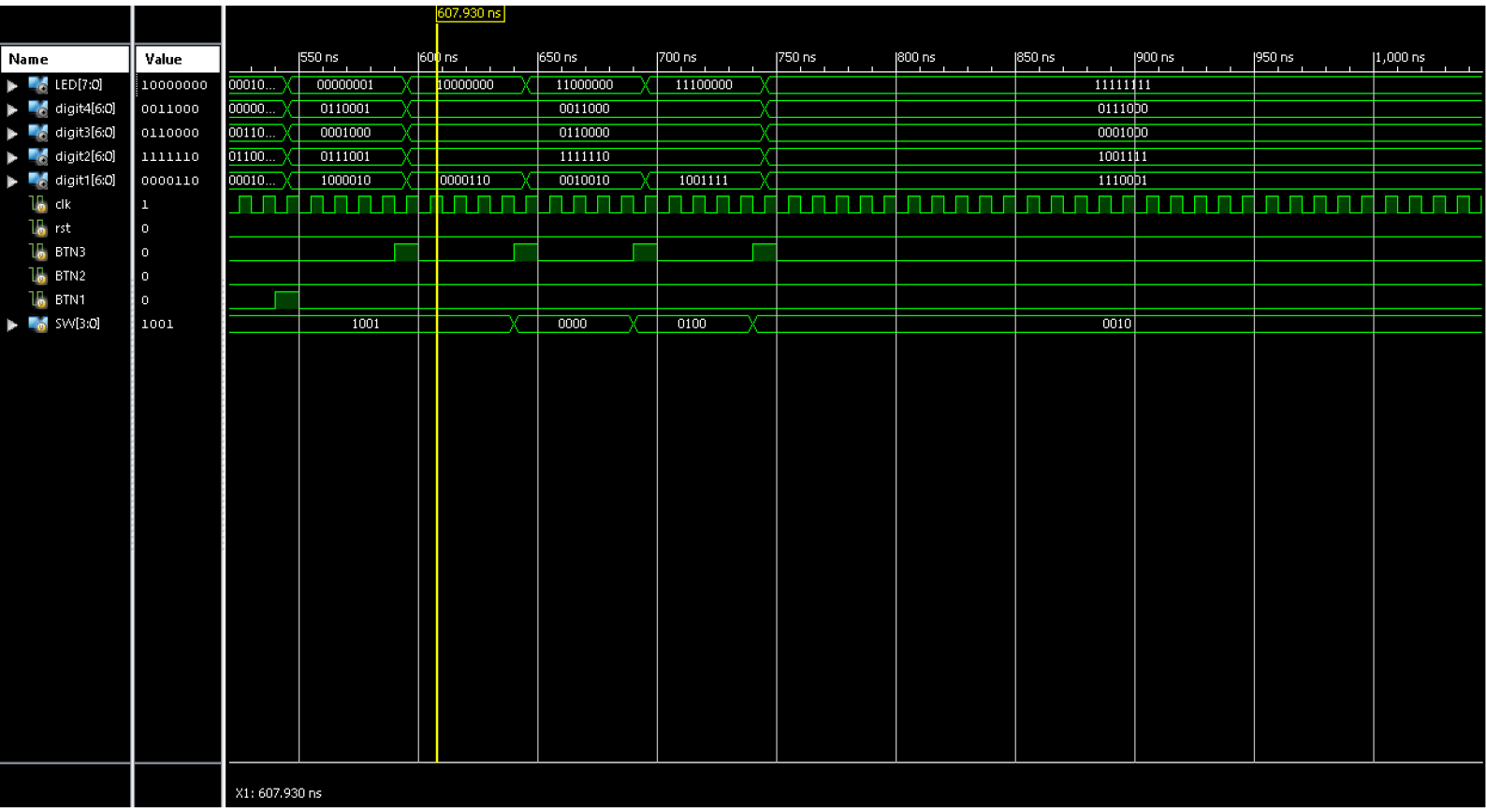


We can observe the 3 steps below so in simulation scenario we completed “j” to “l”.

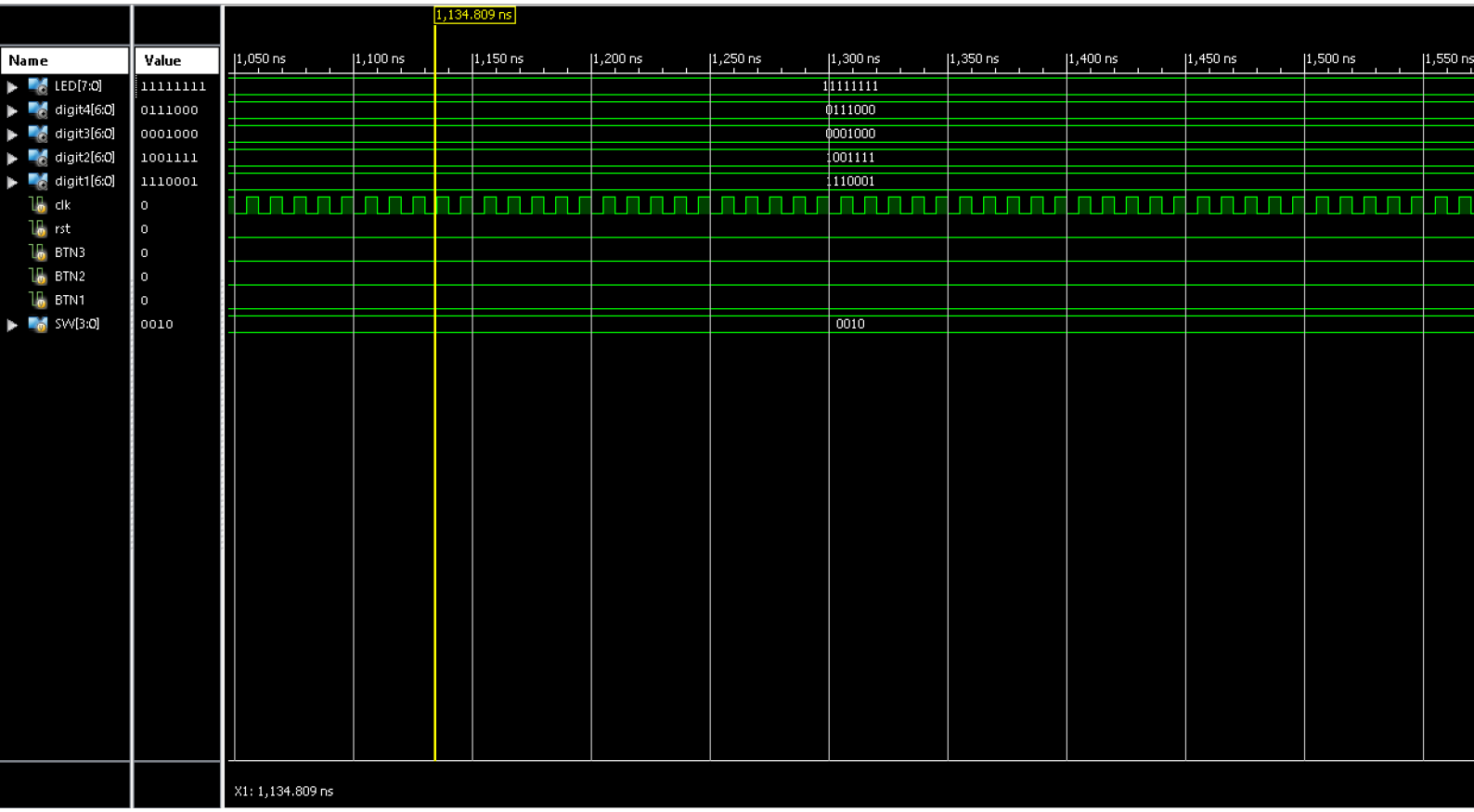
j. Log out from the ATM by pressing *BTN1*

k. Inset the debit card by pressing *BTN3*

l. Enter the password wrong for 3 times (by setting the *SW* and pressing *BTN3*)



We can observe waiting 5 second below.



We can observe the 5 steps below so in simulation scenario we completed “m” to “q”.

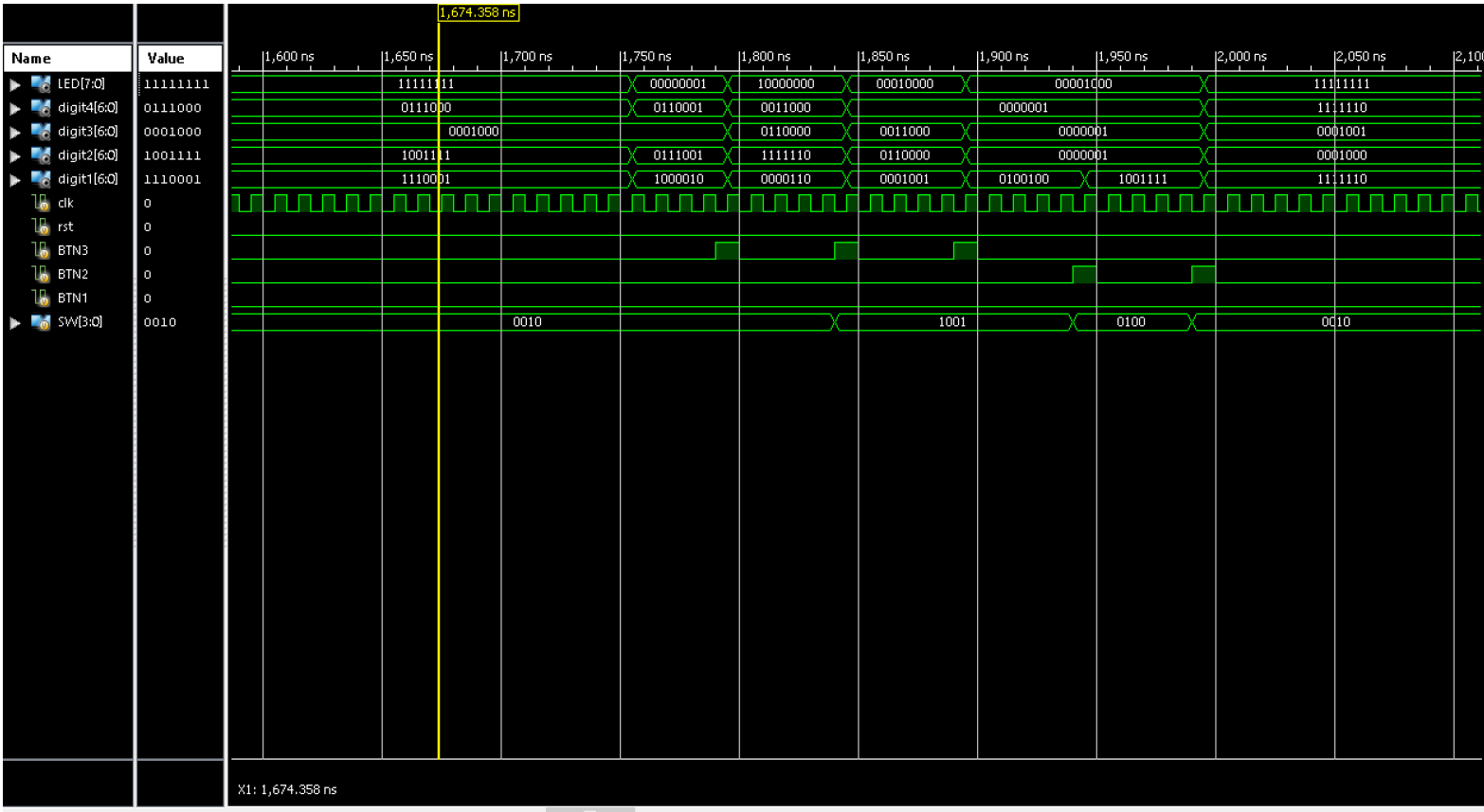
m. Inset the debit card by pressing *BTN3*

n. Enter the password correctly and go to the ATM menu state (by setting the *SW* and pressing *BTN3*)

o. Go to the money operation state by pressing *BTN3*

p. Withdraw 4 from your account (by setting the *SW* and pressing *BTN2*)

q. Withdraw 2 from your account (by setting the *SW* and pressing *BTN2*)

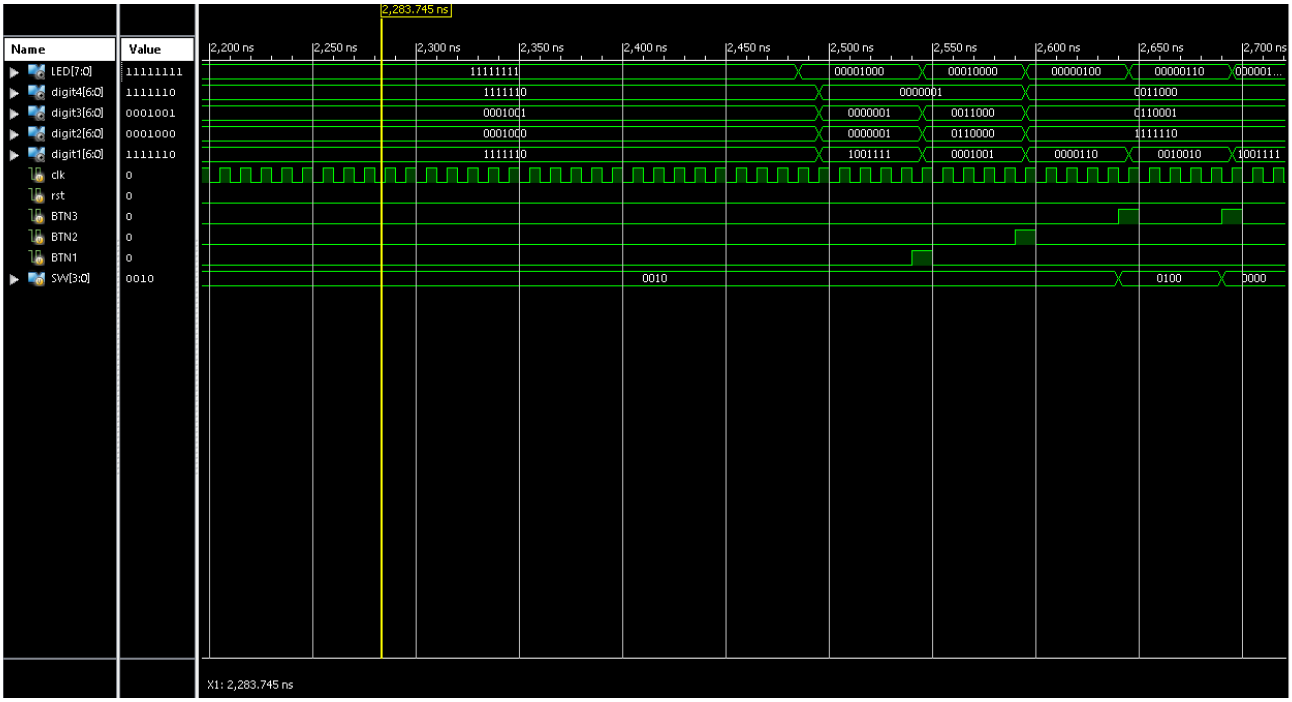


We can observe the 3 steps below so in simulation scenario we completed “r” to “t” but didn’t finished last password entrance.

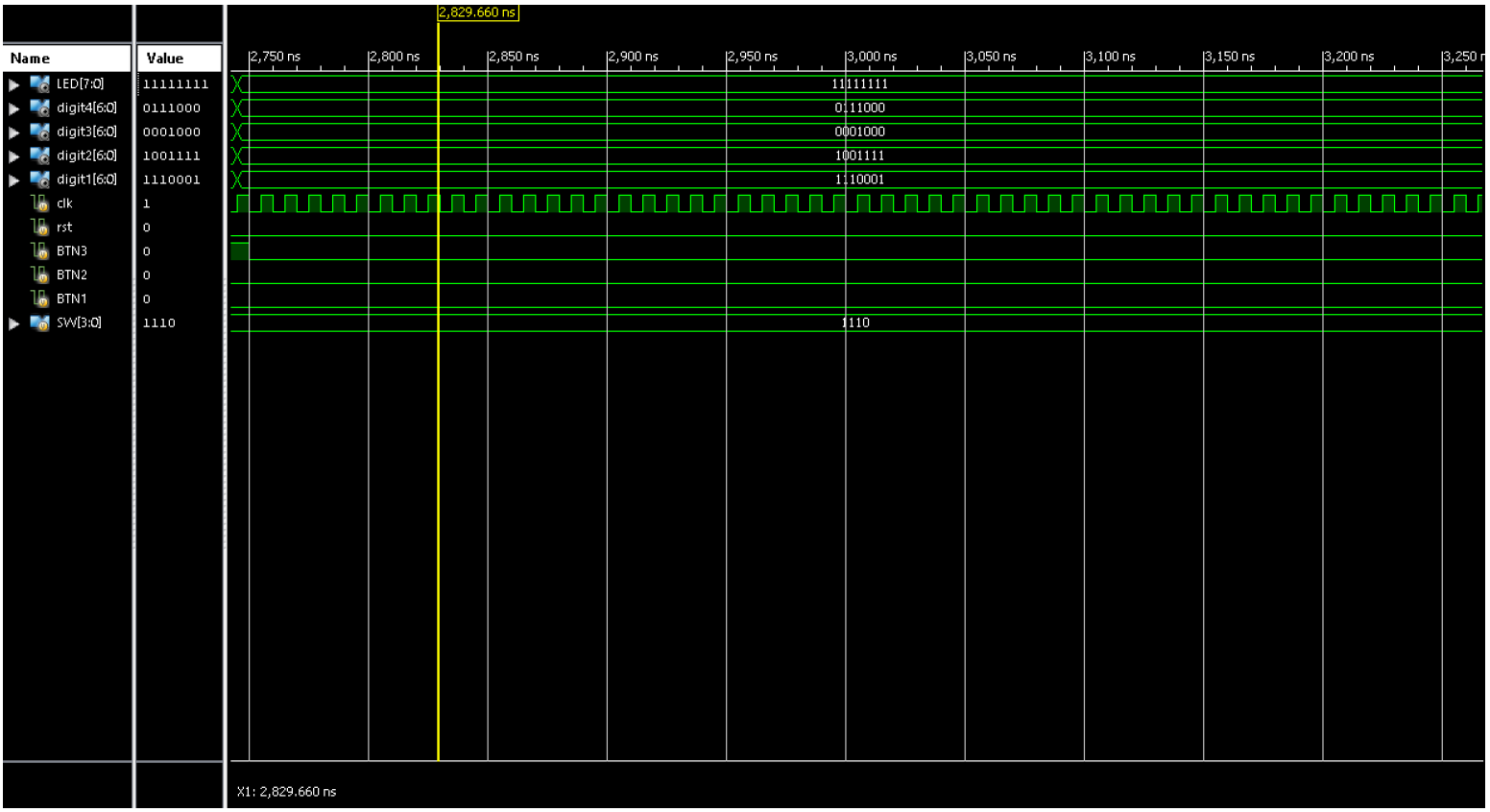
r. Go back to the ATM menu state by pressing *BTN1*

s. Go to the password change state by pressing *BTN2*

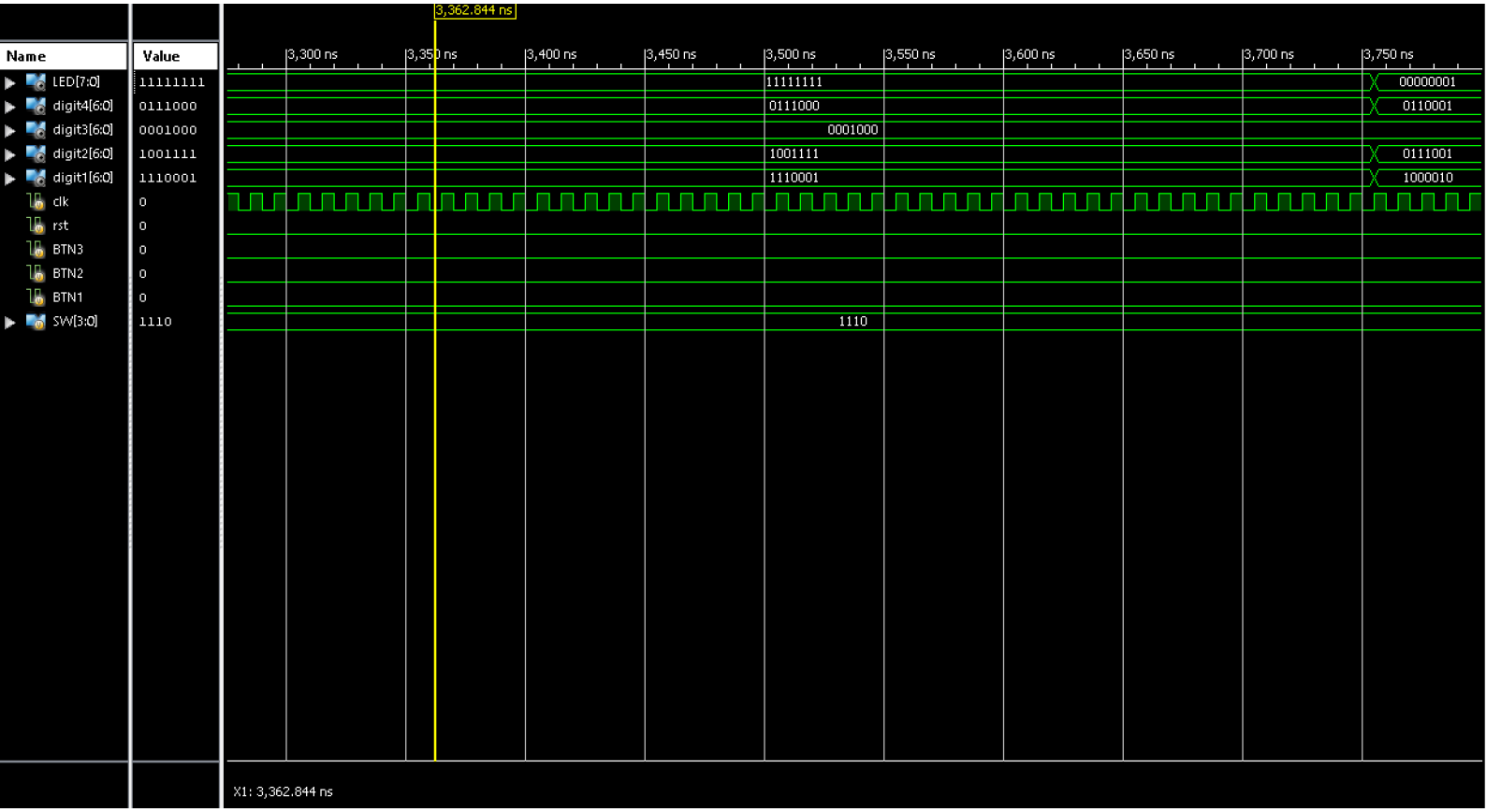
t. Enter the current password wrong for 3 times (by setting the *SW* and pressing *BTN3* -- you should be logged out)



We can observe the last wrong password entrance and waiting phase.



We can see the going IDLE state after the FAIL.



Implementation details

Question: What is the delay for your circuit assumed by the synthesis?
Answer: 5.653 ns.

Question: What is the percentage of the utilized 4 input LUTs?
Answer: The percentage of the utilized 4 input LUTs is 11%.