Laboratory Assignment #4 – All Sections

Due: 13/11/2019, 10:30

Trade-offs in Combinational Circuit Design using Verilog: 15-bit Adder-Subtractor with Overflow Detector Circuit

Requirements:

You are required to design a circuit that can both add and subtract two 15-bit integers and realize whether there is an overflow or not. You will design two different adder-subtractors and compare their performances in terms of propagation time and area requirements. These two adder-subtractors are as follows:

1. 15-bit carry-ripple adder-subtractor using full adders
2. 15-bit hybrid adder-subtractor using a number of carry lookaheads of your own choice (e.g., you can use five 3-bit CLAs).

Both adder-subtractors must detect overflow.

You are also required to use hierarchical design method for these adder-subtractors, in which small building blocks are used to construct the entire circuitry. For example, to design an 15-bit carry-ripple adder-subtractor, you first design a full-adder**,** then instantiate it to top module.

Since this assignment aims you to practice with Verilog language, you will perform both **bitwise operations** and **operations on buses** for computation. You are **not allowed** to use **arithmetic operations** (e.g. addition). For CLA, you **MUST precisely follow** the order below for the computations:

1. Compute the carry information using bitwise operations,
2. Compute any other desired value using arrays.

The performances of your designs are important. They must take up the *minimum area* while *being as fast as possible*. Before coming to the lab you must synthesize your designs for BASYS FGPA boards and include implementation results in your report. Note that the implementation results must be expressed in terms of *time and area*. The time will be in terms of nano-seconds and the area will be expressed as amount of resources on the FPGA device (i.e., number of LUTs).

Compare two designs as follows:

1. Which one of the two is better in terms of area?
2. Which one of the two is better in terms of time?

3. Define a new metric to measure the time-area tradeoff in two designs by multiplying the number of LUTs and time. Which one of the two designs is better in terms of this new metric?
4. State the requirements of a *good* design in terms of area, time and the new metric you've defined.

The following summarizes what you should do before and during the lab session.

Before the lab

1. Work on your designs.
2. Enter your designs using **Verilog**.
3. Simulate your design using Isim. For better visualization, you are required to group the inputs and represent them as signed decimal numbers.
4. Simulation inputs **must** contain one example for each of the following:
    a. addition without a carry and without an overflow,
    b. addition without a carry and with an overflow,
    c. addition with a carry and without an overflow,
    d. addition with a carry and with an overflow.
    e. subtraction without a carry and without an overflow,
    f. subtraction without a carry and with an overflow,
    g. subtraction with a carry and without an overflow,
    h. subtraction with a carry and with an overflow.
5. Synthesize your designs and put the implementation results in your report.
6. Compare the results of the two designs and include an interpretation of these results in your report.
7. Submit your work, as much as you've done, through SUCourse as explained in the document "*Submission Guidance for the FPGA-based Lab Assignments*" in SUCourse.

At the lab

1. Simulate your designs for the input combinations given by your TA.
2. Demonstrate Step 7 for the TA.

Notes

- You will work in groups.
- You will be required to demonstrate your work to the lab assistant as (s)he instructs.
- You do not have to show the operation of your circuit on the FPGA boards. Therefore, you will not actually use the FPGA boards.