

Design and Simulation of a Two-Stage CMOS Operational Amplifier for Low-Noise Applications

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Abstract—This report presents the design and comprehensive simulation of a two-stage CMOS operational amplifier targeting high gain, wide bandwidth, and robust noise performance for analog front-end applications. The amplifier was implemented using MOSFET devices based on the SMIC 0.18 μm MMRF process and evaluated through DC operating point analysis, AC frequency response, transient behavior, and transient noise simulation using Cadence Spectre. Key performance metrics including gain, unitgain bandwidth (GBW), phase margin, slew rate (SR), common-mode rejection ratio (CMRR), and power supply rejection ratio (PSRR) were extracted to validate the amplifier's stability and dynamic response. Due to limitations in executing the `rmsNoise()` function, noise performance was estimated via waveform inspection, yielding a peak-to-peak output fluctuation of 406.13 μV and an RMS noise of approximately 143.5 μV . The resulting signal-to-noise ratio (SNR) was calculated as 81.0 dB. Power consumption was also measured, and a figure of merit (FoM) was derived to benchmark efficiency. These results confirm the amplifier's suitability for precision analog systems under low-noise constraints.

Keywords—*Two-stage operational amplifier, SMIC 0.18 μm MMRF, CMOS, transient noise simulation, SNR estimation, AC analysis, phase margin, CMRR, PSRR, figure of merit, analog front-end.*

I. INTRODUCTION

Op-amps are widely used in analog front-end systems such as sensor interfaces, ADC drivers, and biomedical circuits. Among various topologies, the two-stage CMOS op-amp offers a good balance between gain, output swing, and stability, making it suitable for low-noise applications.

This report presents the design and simulation of a two-stage CMOS op-amp using Cadence Spectre. The simulation workflow includes DC operating point analysis, AC frequency response, transient behavior, and transient noise estimation, etc. Key performance metrics such as gain, bandwidth, phase margin, slew rate, CMRR, nPSRR, and power consumption are extracted and analyzed. Due to limitations in executing the `rmsNoise()` function, noise performance is manually estimated from waveform data, and the signal-to-noise ratio (SNR) is calculated accordingly.

The goal is to evaluate the amplifier's performance across multiple domains and verify its suitability for precision analog systems. All results are documented with physical justification and reproducible methodology.

II. DESIGN METHODOLOGY

The amplifier consists of two main stages and a biasing network, as illustrated in Fig. 1. The first stage features a differential input pair formed by two PMOS transistors (PM5 PM6), which effectively suppress common-mode interference. The load is implemented using a current mirror composed of two NMOS transistors (NM8 NM9), providing high output impedance and differential gain.

The second stage serves as the output amplifier, consisting of a common-source NMOS transistor (NM11) and a PMOS transistor (PM7) acting as a constant current source. The NMOS transistor (NM10) connecting the first and second stages operates in the linear region and can be modeled as a resistor. Together with the compensation capacitor C_c (C_0), this forms a Miller compensation network between the two stages, improving stability and phase margin.

The biasing circuit is implemented using a Widlar current source based on a common-gate and common-source configuration. Transistors PM0 and PM1 share identical W/L ratios, while NM1 and NM4 form a matched common-gate structure to reduce current loss caused by channel length modulation. This configuration provides a stable bias voltage for NM10 and ensures consistent operation across process variations.

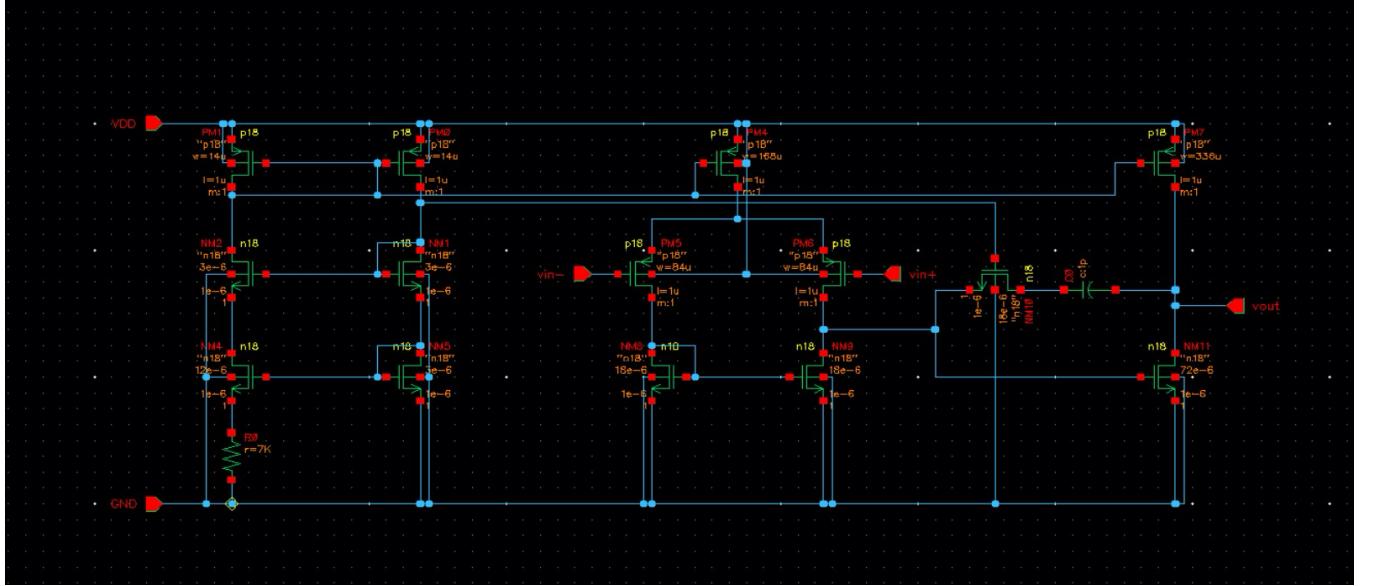


Fig. 1. Schematic of the two-stage CMOS Op-amp, including differential input, current mirrors, gain stage, output stage, and biasing network.

III. TRANSISTOR DIMENSIONING AND BIAS STRATEGY

To simplify layout control and ensure consistent parasitic behavior, all MOSFET channel lengths were uniformly set to $L = 1 \mu\text{A}$. Transistor widths were calculated using the square-law model for long-channel MOSFETs under SMIC 0.18 μm MMRF process parameters. The drain current in saturation is given by:

$$I_D = \frac{1}{2} \mu_p C_{ox} \frac{W}{L} V_{ov}^2$$

Where the relevant key datas are generated from SMIC 0.18 μm MMRF setting:

$$\mu_n = 600 \text{ cm}^2 / \text{V} / \text{s} \quad \mu_p = 200 \text{ cm}^2 / \text{V} / \text{s} \quad T_{ox} =$$

$$20 \text{ nm} \quad C_{ox} = 1.725 \times 10^{-3} \text{ F} / \text{m}^2$$

$$V_{ox} = V_{GS} - V_{th} \in [0.1, 0.4] \text{ V}$$

$$V_{thn} = 0.7 \text{ V} \quad V_{thp} = -0.9 \text{ V} \text{ Initial}$$

Bias Current Strategy:

The initial drain currents I_D for each transistor were selected based on the following considerations:

1. Bias circuit: Low currents ($10\text{--}40 \mu\text{A}$) were chosen to minimize power consumption while maintaining sufficient mirror accuracy and startup reliability.
2. First stage: Moderate currents ($60\text{--}120 \mu\text{A}$) were used to ensure adequate transconductance for gain and noise performance.
3. Second stage: Higher currents ($240 \mu\text{A}$) were selected to support large output swings, fast settling, and stable Miller compensation.
4. Miller compensation path: A small current ($10\text{--}20 \mu\text{A}$) was used to implement the RHP zero without excessive loading.

Bias Circuit Sizing:

1. PM0 & PM1 — PMOS Bias Mirror

Target current: $I_D = 10 \mu\text{A}$ Assumed:

$$V_{ov} = 0.2 \text{ V}$$

$$W = \frac{2 \times 10}{34.5 \times 0.2^2} \approx 14.49$$

Required: $\frac{W}{L}$

Due to the L was set to $1\mu A$, the W was set to $14 \mu A$ for easier operation.

2. NM1 & NM2 — NMOS Bias Control

Target current: $I_D = 10 \mu A$ $V_{ov} = 0.25 V$

$$W = \frac{2 \times 10}{103.6 \times 0.35^3} \approx 3.09$$

Required: $\frac{W}{L}$

Similarly, we can obtain $W = 3\mu m$

3. NM4 — NMOS Reference Branch

Target current: $I_D = 40 \mu A$ $V_{ov} = 0.25V$

$$W = \frac{2 \times 40}{103.6 \times 0.25^2} \approx 12.35$$

Required: $\frac{W}{L}$

Similarly, we can obtain $W = 12\mu m$

4. NM5 — NMOS Bias Output

Same caculation as NM1 and NM2.

Bias Circuit Sizing Strategy and Finger Sweep Analysis:

The bias circuit was first implemented and simulated independently to verify startup behavior and current stability, as shown in Fig. 2. DC operating point analysis confirmed that all transistors operated in saturation and that bias currents were correctly established. To further refine the sizing of the PMOS bias mirror, a finger width sweep was performed on transistor PM1, with results shown in Fig. 3. The sweep revealed that as the total width W increased, the gate overdrive voltage V_{gst} decreased monotonically, indicating improved current density and reduced mismatch.

From the sweep data, it was observed that for a target bias current of $I = 10 \mu A$, a gate overdrive voltage of approximately $V_{gst} = 150 mV$ was achieved when:

$$\text{NMOS devices used } \frac{W}{L} = 3$$

$$\text{PMOS devices used } \frac{W}{L} = 14$$

These values were selected as reference dimensions for bias-driven transistors. Based on current mirror scaling principles, the remaining transistors in the bias circuit were sized proportionally to these reference devices. Specifically:

For all PMOS transistors biased by the reference current I_B , the aspect ratio was determined by:

$$\left(\frac{W}{L}\right)_i = \left(\frac{I_i}{I_B}\right) \times \left(\frac{W}{L}\right)_P$$

For all NMOS transistors biased by I_b , the aspect ratio was:

$$\left(\frac{W}{L}\right)_j = \left(\frac{I_j}{I_B}\right) \times \left(\frac{W}{L}\right)_N$$

In this design, transistors NM1 and NM4 jointly generate the reference bias current $I_b = 10\mu A$, which serves as the basis for sizing all other bias-driven devices. This modular sizing approach ensures consistent current ratios, simplifies layout symmetry, and improves robustness against process variation.

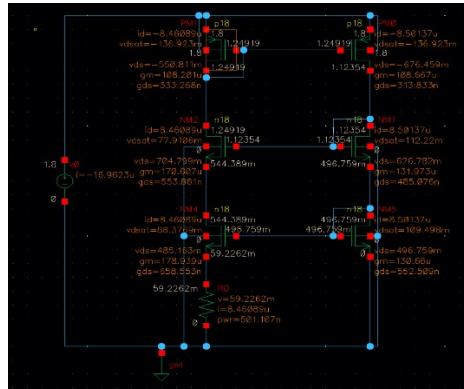


Fig. 2. Standalone Bias Circuit for Reference

PMOS M8 Finger Width Sweep Current															
Device	$\#$	x	y	w	l	$area$	g_s	g_d	g_{ds}	i_{ds}	v_{ds}	i_{ds}	v_{ds}	i_{ds}	v_{ds}
M8	4	-421298	4	492.28n	38.25n	15.71	54.8	54.8	54.8	2.14E-06	-20.62m	2.14E-06	-20.62m	2.14E-06	-20.62m
M8	5	-421399	4	404078	35.25n	15.75	54.8	54.8	54.8	2.15E-06	-20.62m	2.15E-06	-20.62m	2.15E-06	-20.62m
M8	6	-421499	4	425278	35.25n	15.75	54.8	54.8	54.8	2.16E-06	-20.62m	2.16E-06	-20.62m	2.16E-06	-20.62m
M8	7	-421599	4	436478	35.25n	15.75	54.8	54.8	54.8	2.17E-06	-20.62m	2.17E-06	-20.62m	2.17E-06	-20.62m
M8	8	-421699	4	447678	35.25n	15.75	54.8	54.8	54.8	2.18E-06	-20.62m	2.18E-06	-20.62m	2.18E-06	-20.62m
M8	9	-421799	4	458878	35.25n	15.75	54.8	54.8	54.8	2.19E-06	-20.62m	2.19E-06	-20.62m	2.19E-06	-20.62m
M8	10	-421899	4	460078	35.25n	15.75	54.8	54.8	54.8	2.20E-06	-20.62m	2.20E-06	-20.62m	2.20E-06	-20.62m
M8	11	-421999	4	471278	35.25n	15.75	54.8	54.8	54.8	2.21E-06	-20.62m	2.21E-06	-20.62m	2.21E-06	-20.62m
M8	12	-422099	4	482478	35.25n	15.75	54.8	54.8	54.8	2.22E-06	-20.62m	2.22E-06	-20.62m	2.22E-06	-20.62m
M8	13	-422199	4	493678	35.25n	15.75	54.8	54.8	54.8	2.23E-06	-20.62m	2.23E-06	-20.62m	2.23E-06	-20.62m
M8	14	-422299	4	504878	35.25n	15.75	54.8	54.8	54.8	2.24E-06	-20.62m	2.24E-06	-20.62m	2.24E-06	-20.62m
M8	15	-422399	4	516078	35.25n	15.75	54.8	54.8	54.8	2.25E-06	-20.62m	2.25E-06	-20.62m	2.25E-06	-20.62m
M8	16	-422499	4	527278	35.25n	15.75	54.8	54.8	54.8	2.26E-06	-20.62m	2.26E-06	-20.62m	2.26E-06	-20.62m
M8	17	-422599	4	538478	35.25n	15.75	54.8	54.8	54.8	2.27E-06	-20.62m	2.27E-06	-20.62m	2.27E-06	-20.62m
M8	18	-422699	4	549678	35.25n	15.75	54.8	54.8	54.8	2.28E-06	-20.62m	2.28E-06	-20.62m	2.28E-06	-20.62m
M8	19	-422799	4	560878	35.25n	15.75	54.8	54.8	54.8	2.29E-06	-20.62m	2.29E-06	-20.62m	2.29E-06	-20.62m
M8	20	-422899	4	572078	35.25n	15.75	54.8	54.8	54.8	2.30E-06	-20.62m	2.30E-06	-20.62m	2.30E-06	-20.62m
M8	21	-422999	4	583278	35.25n	15.75	54.8	54.8	54.8	2.31E-06	-20.62m	2.31E-06	-20.62m	2.31E-06	-20.62m
M8	22	-423099	4	594478	35.25n	15.75	54.8	54.8	54.8	2.32E-06	-20.62m	2.32E-06	-20.62m	2.32E-06	-20.62m
M8	23	-423199	4	605678	35.25n	15.75	54.8	54.8	54.8	2.33E-06	-20.62m	2.33E-06	-20.62m	2.33E-06	-20.62m
M8	24	-423299	4	616878	35.25n	15.75	54.8	54.8	54.8	2.34E-06	-20.62m	2.34E-06	-20.62m	2.34E-06	-20.62m
M8	25	-423399	4	628078	35.25n	15.75	54.8	54.8	54.8	2.35E-06	-20.62m	2.35E-06	-20.62m	2.35E-06	-20.62m
M8	26	-423499	4	639278	35.25n	15.75	54.8	54.8	54.8	2.36E-06	-20.62m	2.36E-06	-20.62m	2.36E-06	-20.62m
M8	27	-423599	4	650478	35.25n	15.75	54.8	54.8	54.8	2.37E-06	-20.62m	2.37E-06	-20.62m	2.37E-06	-20.62m
M8	28	-423699	4	661678	35.25n	15.75	54.8	54.8	54.8	2.38E-06	-20.62m	2.38E-06	-20.62m	2.38E-06	-20.62m
M8	29	-423799	4	672878	35.25n	15.75	54.8	54.8	54.8	2.39E-06	-20.62m	2.39E-06	-20.62m	2.39E-06	-20.62m
M8	30	-423899	4	684078	35.25n	15.75	54.8	54.8	54.8	2.40E-06	-20.62m	2.40E-06	-20.62m	2.40E-06	-20.62m
M8	31	-423999	4	695278	35.25n	15.75	54.8	54.8	54.8	2.41E-06	-20.62m	2.41E-06	-20.62m	2.41E-06	-20.62m
M8	32	-424099	4	706478	35.25n	15.75	54.8	54.8	54.8	2.42E-06	-20.62m	2.42E-06	-20.62m	2.42E-06	-20.62m
M8	33	-424199	4	717678	35.25n	15.75	54.8	54.8	54.8	2.43E-06	-20.62m	2.43E-06	-20.62m	2.43E-06	-20.62m
M8	34	-424299	4	728878	35.25n	15.75	54.8	54.8	54.8	2.44E-06	-20.62m	2.44E-06	-20.62m	2.44E-06	-20.62m
M8	35	-424399	4	740078	35.25n	15.75	54.8	54.8	54.8	2.45E-06	-20.62m	2.45E-06	-20.62m	2.45E-06	-20.62m
M8	36	-424499	4	751278	35.25n	15.75	54.8	54.8	54.8	2.46E-06	-20.62m	2.46E-06	-20.62m	2.46E-06	-20.62m
M8	37	-424599	4	762478	35.25n	15.75	54.8	54.8	54.8	2.47E-06	-20.62m	2.47E-06	-20.62m	2.47E-06	-20.62m
M8	38	-424699	4	773678	35.25n	15.75	54.8	54.8	54.8	2.48E-06	-20.62m	2.48E-06	-20.62m	2.48E-06	-20.62m
M8	39	-424799	4	784878	35.25n	15.75	54.8	54.8	54.8	2.49E-06	-20.62m	2.49E-06	-20.62m	2.49E-06	-20.62m
M8	40	-424899	4	796078	35.25n	15.75	54.8	54.8	54.8	2.50E-06	-20.62m	2.50E-06	-20.62m	2.50E-06	-20.62m
M8	41	-424999	4	807278	35.25n	15.75	54.8	54.8	54.8	2.51E-06	-20.62m	2.51E-06	-20.62m	2.51E-06	-20.62m
M8	42	-425099	4	818478	35.25n	15.75	54.8	54.8	54.8	2.52E-06	-20.62m	2.52E-06	-20.62m	2.52E-06	-20.62m
M8	43	-425199	4	829678	35.25n	15.75	54.8	54.8	54.8	2.53E-06	-20.62m	2.53E-06	-20.62m	2.53E-06	-20.62m
M8	44	-425299	4	840878	35.25n	15.75	54.8	54.8	54.8	2.54E-06	-20.62m	2.54E-06	-20.62m	2.54E-06	-20.62m
M8	45	-425399	4	852078	35.25n	15.75	54.8	54.8	54.8	2.55E-06	-20.62m	2.55E-06	-20.62m	2.55E-06	-20.62m
M8	46	-425499	4	863278	35.25n	15.75	54.8	54.8	54.8	2.56E-06	-20.62m	2.56E-06	-20.62m	2.56E-06	-20.62m
M8	47	-425599	4	874478	35.25n	15.75	54.8	54.8	54.8	2.57E-06	-20.62m	2.57E-06	-20.62m	2.57E-06	-20.62m
M8	48	-425699	4	885678	35.25n	15.75	54.8	54.8	54.8	2.58E-06	-20.62m	2.58E-06	-20.62m	2.58E-06	-20.62m
M8	49	-425799	4	896878	35.25n	15.75	54.8	54.8	54.8	2.59E-06	-20.62m	2.59E-06	-20.62m	2.59E-06	-20.62m
M8	50	-425899	4	908078	35.25n	15.75	54.8	54.8	54.8	2.60E-06	-20.62m	2.60E-06	-20.62m	2.60E-06	-20.62m
M8	51	-425999	4	919278	35.25n	15.75	54.8	54.8	54.8	2.61E-06	-20.62m	2.61E-06	-20.62m	2.61E-06	-20.62m
M8	52	-426099	4	930478	35.25n	15.75	54.8	54.8	54.8	2.62E-06	-20.62m	2.62E-06	-20.62m	2.62E-06	-20.62m
M8	53	-426199	4	941678	35.25n	15.75	54.8	54.8	54.8	2.63E-06	-20.62m	2.63E-06	-20.62m	2.63E-06	-20.62m
M8	54	-426299	4	952878	35.25n	15.75	54.8	54.8	54.8	2.64E-06	-20.62m	2.64E-06	-20.62m	2.64E-06	-20.62m
M8	55	-426399	4	964078	35.25n	15.75	54.8	54.8	54.8	2.65E-06	-20.62m	2.65E-06	-20.62m	2.65E-06	-20.62m
M8	56	-426499	4	975278	35.25n	15.75	54.8	54.8	54.8	2.66E-06	-20.62m	2.66E-06	-20.62m	2.66E-06	-20.62m
M8	57	-426599	4	986478	35.25n	15.75	54.8	54.8	54.8	2.67E-06	-20.62m	2.67E-06	-20.62m	2.67E-06	-20.62m
M8	58	-426699	4	997678	35.25n	15.75	54.8	54.8	54.8	2.68E-06	-20.62m	2.68E-06	-20.62m	2.68E-06	-20.62m
M8	59	-426799	4	1008878	35.25n	15.75	54.8	54.8	54.8	2.69E-06	-20.62m	2.69E-06	-20.62m	2.69E-06	-20.62m
M8	60	-426899	4	1010078	35.25n	15.75	54.8	54.8	54.8	2.70E-06	-20.62m	2.70E-06	-20.62m	2.70E-06	-20.62m
M8	61	-426999	4	1021278	35.2										

$$\frac{W}{L} = 18$$

2. C_0 — Compensation Capacitor

Initial value: $C_0 = 1 \text{ pF}$

This capacitor value is selected based on load capacitor $C_L = 3 \text{ pF}$, ensuring adequate phase margin and GBW.

IV. SIMULATION RESULTS AND PERFORMANCE ANALYSIS

A comprehensive suite of simulations was performed to evaluate the functionality, performance, and robustness of the proposed two-stage CMOS operational amplifier. The analysis encompassed DC operating point verification, AC frequency response characterization, transient behavior assessment, noise performance evaluation, and static power consumption estimation.

1. Basic Tests: DC and AC Analysis

All basic simulations, including DC operating point and AC frequency response, were performed using the same test circuit, shown in Fig. 4. The schematic includes bias voltage sources ($V1 = 1.8 \text{ V}$, $V2 = 900 \text{ mV}$), an AC excitation source ($V0 = 1 \text{ V}$), a load capacitor ($C_0 = 3 \text{ pF}$), and proper power and ground connections. This unified setup ensures consistent biasing and signal paths across all basic tests.

1.1. DC Operating Point Analysis

The DC operating point simulation was conducted to verify that all transistors operate in their intended regions and that the designed biasing scheme functions as expected. The extracted drain currents and node voltages confirmed correct biasing:

- a. The first-stage differential amplifier consumed $60.244 \mu\text{A}$, resulting in a power consumption of $108.44 \mu\text{W}$.
- b. The second-stage gain transistor drew $246.72 \mu\text{A}$, corresponding to $444.10 \mu\text{W}$.
- c. Total static power consumption was estimated at $552.54 \mu\text{W}$.

All MOSFETs operated in the saturation region, except for the compensation transistor (NM10), which was intentionally biased in the linear region to implement a right-half-plane (RHP) zero. A detailed summary of transistor operating states is provided in Fig. 5.

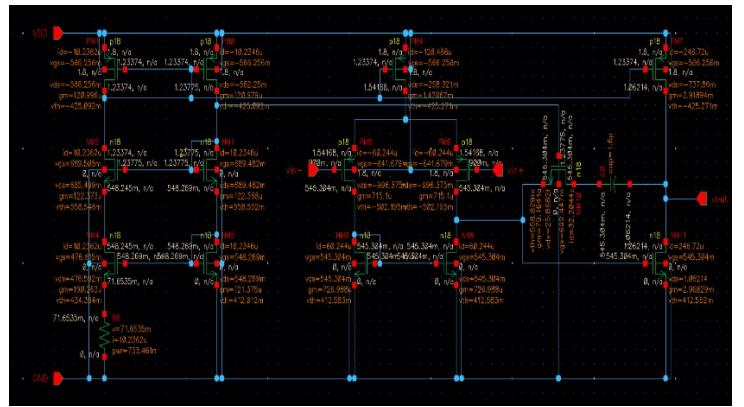
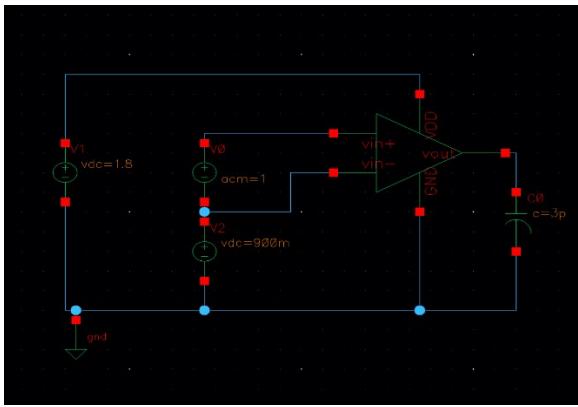


Fig. 4. Unified testbench schematic used for DC and AC simulations. **Fig. 5.** Transistor operating regions and bias currents extracted from DC simulation.

1.2. AC Frequency Response

AC analysis was performed to evaluate the amplifier's small-signal behavior, including gain, bandwidth, and stability. The simulation was conducted using the same testbench schematic shown in Fig. 5, as the DC analysis, with an AC excitation source applied to the differential input and a capacitive load connected at the output.

Initial results with a compensation capacitor of $C_c = 1 \text{ pF}$ revealed a unity-gain bandwidth of 114 MHz. However, the phase margin was measured at only 47° , which is below the typical stability threshold for closed-loop operation. This indicated a risk of underdamped response or potential oscillation when feedback is applied.

To improve stability, the compensation capacitor was increased to $C_c = 1.6 \text{ pF}$. The Differential-mode gain was extracted from the AC magnitude plot shown in Fig. 6. From the simulation:

- Differential-mode gain was measured at 86.6356 dB, indicating strong open-loop amplification.
- The unity-gain bandwidth (GBW) which is about 112.94 MHz was determined by identifying the frequency at which the gain magnitude crosses 0 dB. At this point, the slope of the gain curve was approximately -20 dB/decade, indicating dominant-pole behavior.
- Phase margin was calculated as 57.17° , measured at the unity-gain frequency.

These results confirm that the amplifier achieves high gain and wide bandwidth while maintaining adequate phase margin for closed-loop stability. The compensation capacitor C_c was set to 1.6 pF in this simulation, following earlier observations that a smaller value (1 pF) resulted in insufficient phase margin ($\sim 47^\circ$). The increased C_c effectively shifted the dominant pole, reducing GBW slightly but improving stability.

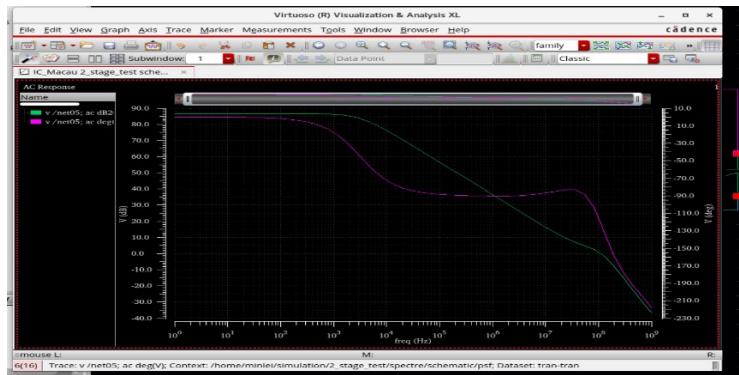


Fig. 6. The Differential-mode gain was extracted from the AC magnitude plot

2. Transient Response Analysis

Transient simulations were conducted to evaluate the amplifier's large-signal behavior, particularly its slew rate and noise characteristics during fast transitions. The input signal was configured as a voltage pulse source (vpulse) with the following parameters:

- Initial voltage (V2): 0 V
- Final voltage (V1): 1.8 V
- Rise time (tr): 1 ns
- Fall time (tf): 1 ns
- Pulse width: 20 μs
- Delay time: 10 μs
- Period: 40 μs

This configuration produces a sharp step-like transition at $t = 10 \mu\text{s}$, allowing the amplifier to operate under maximum slew conditions. The extremely fast rise time of 1 ns ensures that the input transition is much faster than the amplifier's intrinsic response, making it ideal for measuring slew rate and settling time.

The testbench configuration is shown in Fig. 7., where the pulse input is applied to the non-inverting terminal. The inverting input is connected to the output through a unity-gain feedback loop, and a capacitive load of 3 pF is placed at the output node.

The output waveform and its time derivative were analyzed using Virtuoso Visualization & Analysis XL, as shown in Fig. 8. The green curve represents the output voltage, while the red curve shows its time derivative, extracted using the Calculator tool.

- a. Slew Rate (SR): The peak value of the derivative curve corresponds to a measured slew rate of $35.72 \text{ V}/\mu\text{s}$, confirming the amplifier's ability to drive capacitive loads under fast input transitions.
- b. Settling Time: The output reached steady-state within 83 ns , defined as the time required to remain within $\pm 1\%$ of the final value (1.78413 V), measured from the input edge at $10 \mu\text{s}$.

Physical Principles of Slew Rate and Settling Time:

The slew rate of an operational amplifier represents the maximum rate at which the output voltage can change in response to a large input signal. It is primarily determined by the bias current of the second stage and the capacitive load at the output, and can be approximated as:

$$SR = \frac{I_{bias}}{C_L}$$

where I_{bias} is the bias current of the output stage and C_L is the load capacitance. In this design, the second-stage transistor provides approximately $246.72 \mu\text{A}$ of current to drive a 3 pF load, theoretically supporting a maximum SR of:

$$SR_{max} = \frac{246.72 \times 10^{-6}}{3 \times 10^{-12}} = 82.24 \text{ V}/\mu\text{A}$$

The simulated result is significantly lower at $35.72 \text{ V}/\mu\text{s}$. This discrepancy arises because not all bias current reaches the load capacitor in practice. Internal parasitic capacitances, Miller compensation feedback, and non-ideal current source behavior reduce the effective charging current. Additionally, gate overdrive and node settling delays during fast transitions further limit the output swing rate, making the simulated value a more realistic reflection of actual circuit dynamics.

Transient Noise Behavior and SNR Calculation:

To evaluate dynamic noise performance, transient noise simulations were performed under two conditions: steady-state and during slew-rate transitions. A noise factor of 10, frequency range of 1 Hz to 1 GHz , and 100 Monte Carlo runs were used to extract statistical noise behavior.

- a. Steady-state noise: As shown in Fig. 9., the output voltage fluctuated between 1.783380635 V and 1.78340022 V , yielding a peak-to-peak noise amplitude of:

$$V_{noise,pp} = 1.78380635 - 1.78340022 = 406.13 \mu\text{A}$$

The signal-to-noise ratio (SNR) is calculated as:

$$SNR_{dB} = 20 \times \log^{10} \left(\frac{1.8 \times \sqrt{2}}{406.13 \times 10^{-6}} \right) \approx 81 \text{ dB}$$

- b. Slew-rate noise: During the fast transition phase, as shown in Fig. 10., the output exhibited increased noise activity. The measured slew rate was $68.63 \text{ V}/\mu\text{s}$, calculated using the derivative of the output waveform via the Virtuoso Calculator. This value reflects the amplifier's maximum large-signal response under transient excitation, and is higher than the nominal SR due to dynamic bias boosting and capacitive charging effects during the input edge.

Output Swing:

The output swing of the amplifier was extracted from the transient simulation waveform. As observed from the plot, as shown in Fig. 8., the output voltage ranges from 34.493 mV to 1.7835 V , indicating that the amplifier achieves near rail-to-rail performance under a 1.8 V supply. This wide swing confirms the output stage's ability to drive signals across most of the supply range without significant distortion or saturation.

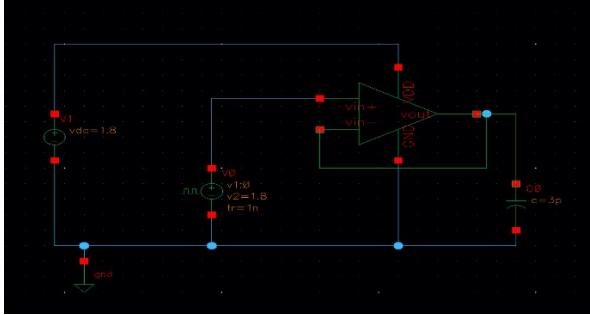


Fig. 7. Transient testbench schematic for slew rate and noise analysis.



Fig. 8. Transient output waveform under a 1.8 V input pulse.

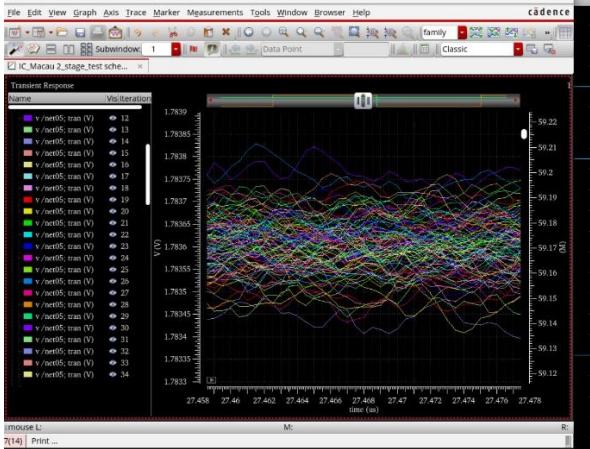


Fig. 9. Transient noise simulation under steady-state conditions.

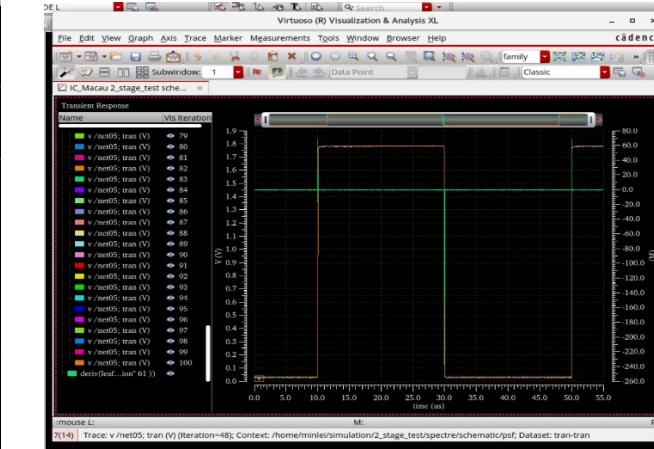


Fig. 10. Transient noise simulation during slew-rate transition.

3. AC Noise Analysis (Low Frequency)

To evaluate low-frequency noise performance, an AC noise simulation was conducted over the 1 Hz to 100 Hz range using the differential testbench. The input source was set to zero, and the output noise spectral density was measured in units of mV/\sqrt{Hz} .

As shown in Fig. 11., the red curve exhibits a typical $1/f$ behavior, with noise density decreasing as frequency increases. This flicker noise is primarily generated by the input differential pair and biasing transistors. The spectrum confirms that the amplifier is dominated by flicker noise below 10 Hz, transitioning toward thermal noise beyond that point.

As shown in Fig. 12., Using the Virtuoso Calculator, the integrated output noise over this frequency range was computed as:

$$V_{noise,RMS} = \sqrt{\int_{1 \text{ Hz}}^{100 \text{ Hz}} PSD(f) df} = 3.999 \mu V$$

This result confirms the amplifier's low-noise performance in the low-frequency regime, making it suitable for precision applications such as sensor front-ends, biomedical instrumentation, and low-speed ADC drivers.

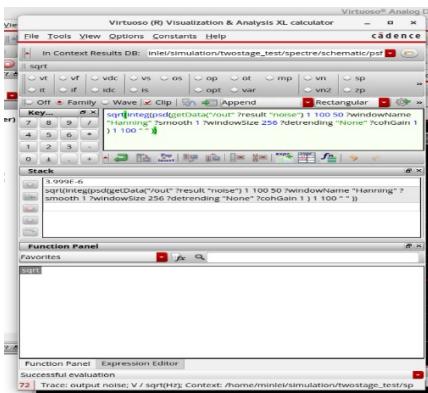


Fig. 11. Output noise spectral density from 1 Hz to 100 Hz.

Fig. 12. Output noise calculation using

PSD integration in Virtuoso Calculator.

4. Common-Mode Rejection Ratio (CMRR) & Common-Mode Input Range (CMIR) CMRR Test:

The Common-Mode Rejection Ratio (CMRR) quantifies the amplifier's ability to suppress common-mode signals while amplifying differential inputs. It is a critical metric for analog front-end circuits, especially in noisy environments.

When both gains are expressed in decibels, CMRR can be directly calculated as:

$$CMRR_{dB} = 20 \times \log_{10} \left(\frac{A_{diff}}{A_{cm}} \right) \approx A_{diff,dB} - A_{cm,dB}$$

Simulation Setup:

To evaluate CMRR, two separate AC simulations were performed under identical biasing and load conditions. Common-mode gain (A_{cm}) was measured by applying the same AC voltage to both inputs ($AC = 1 V$; $DC = 900 mV$) simulating a common-mode disturbance.

The schematic used for common-mode gain simulation is shown in Fig. 13. In this configuration, a 1 V AC signal is applied to $vin +$, while $vin -$ is held at 900 mV DC. The output is loaded with a 3 pF capacitor to emulate realistic capacitive loading conditions.

Results and Calculation:

The common-mode gain was extracted from the AC magnitude plot shown in Fig. 14, where the output under commonmode excitation exhibits a peak gain of approximately 2.2685 dB . The curve remains relatively flat across the bandwidth, indicating limited sensitivity to common-mode disturbances. a. The differential gain was measured in the Part 1.2 as:

$$A_{diff,dB} = 86.6356 dB$$

- b. The common-mode gain, extracted from the AC magnitude plot shown in Fig. 14. , is:

$$A_{cm,dB} = 2.2685 dB$$

- c. Using the simplified decibel subtraction method, the calculated CMRR is:

$$CMRR_{dB} = 86.6356 - 2.2685 = 84.3671 dB$$

Physical Interpretation:

The measured CMRR of 84.3671 dB indicates strong suppression of common-mode interference, exceeding typical design targets for precision analog circuits. This performance reflects: a. Symmetric input differential pair

- b. Well-matched current mirror loads
c. Careful layout symmetry and biasing strategy

Such characteristics are essential for instrumentation amplifiers, sensor interfaces, and ADC front-ends, where common-mode noise rejection is critical. The result confirms that the amplifier is well-suited for high-accuracy differential signal processing in noisy environments.

CMIR Test:

Common-Mode Input Range (CMIR) refers to the range of input voltages—applied equally to both inputs of a differential amplifier—over which the amplifier operates in its intended linear region without distortion, cutoff, or saturation.

Results:

To determine the common-mode input voltage range (CMIR), a DC sweep was performed by applying equal voltages to both input terminals of the amplifier ($vin+ = vin -$), simulating a pure common-mode input. The input voltage was swept from 0 V to 1.8 V.

As shown in Fig. 15., the output voltage exhibits a nonlinear behavior at low and high input levels, remaining clamped below approximately 950 mV and saturating beyond 1.05 V. However, within the range of 950 mV to 1.05 V, the output voltage increases in a near-linear fashion, forming a distinct straight-line segment on the curve. This indicates that the amplifier operates in its linear region over this interval, with stable gain and proper signal amplification. Therefore, based on the observed linear segment of the output voltage curve, the CMIR is extracted as 950 mV to 1.05 V, ensuring reliable operation across a substantial portion of the supply range.

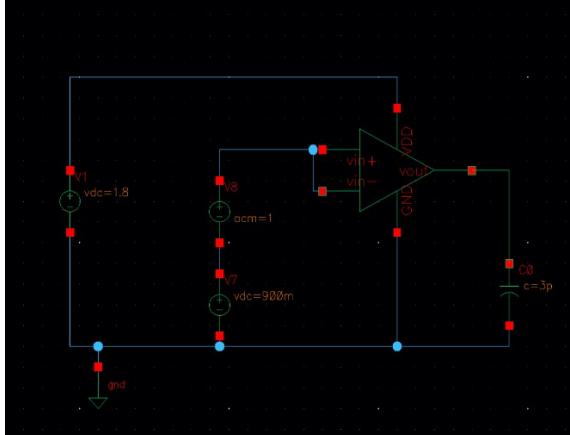


Fig. 13. Transient testbench schematic for CMRR analysis.

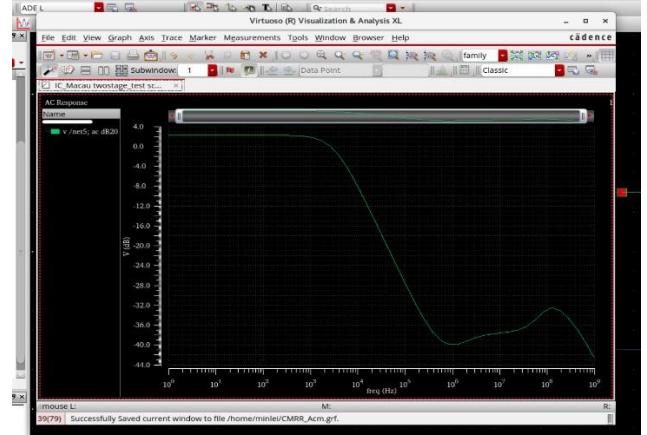


Fig. 14. The common-mode gain extracted from the AC magnitude plot

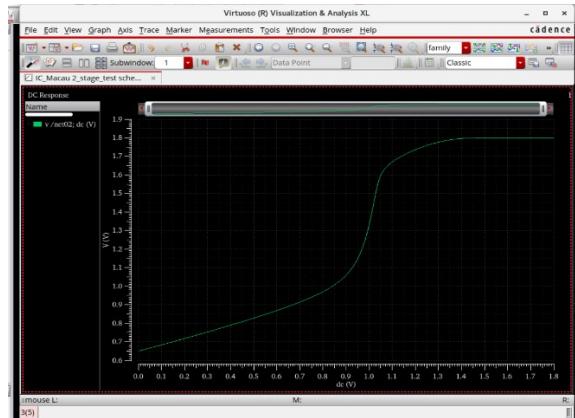


Fig. 15(a). DC Response Curve for Common-Mode Input Sweep

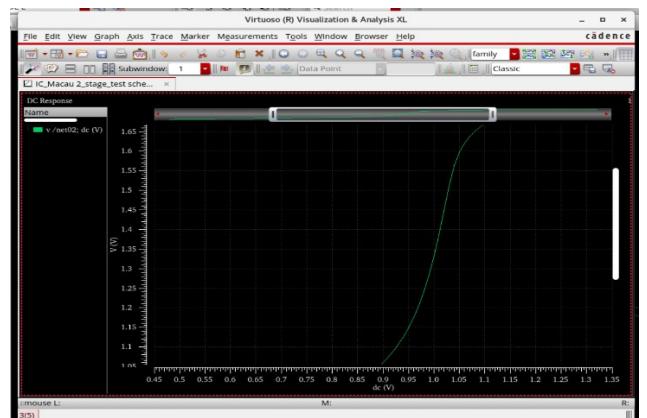


Fig. 15(b). Near-Linear Part of the curve

5. Negative Power Supply Rejection Ratio (nPSRR)

Power Supply Rejection Ratio (PSRR) quantifies an amplifier's ability to suppress variations in its supply voltage. While PSRR typically refers to disturbances on the positive rail (VDD), nPSRR focuses on the negative rail (VSS), which is especially relevant in low-voltage or single-supply designs where ground noise can couple into the signal path.

The nPSRR is defined as:

$$nPSRR_{dB} = 20 \times \log_{10}\left(\frac{A_{diff}}{A_{VSS}}\right)$$

Simulation Setup:

In the simulation setup, a 1 V AC signal was applied to the negative supply rail (VSS) via source V9. The positive rail (VDD) was maintained at 1.8 V DC using source V1, and the amplifier was biased normally with v_{in-} held at 900 mV DC through source V7. The schematic used for the test is shown in Fig. 16. .

Results and Interpretation:

The AC simulation result is shown in Fig. 17. , where the output magnitude (dB20) is plotted versus frequency. The curve shows a decreasing trend, with an interval of output rising ripple between the transmission zero and the

dominant pole. A small rising segment is observed in the low-to-mid frequency range, caused by zero-pole separation, a transmission zero preceding a dominant pole. This results in a temporary gain increase before the roll-off resumes. However, the magnitude remains below 0 dB, meaning the output ripple is still smaller than the injected disturbance. Therefore, the impact on overall nPSRR is negligible.

Gain-Based Calculation:

- The amplifier's Differential-mode gain is:

$$A_{diff,dB} = 86.6356dB$$

- The gain from VSS to output is:

$$A_{VSS,dB} = -5.87172dB$$

- Then the nPSRR is calculated as:

$$nPSRR = 82.513dB$$

This confirms that the amplifier strongly suppresses negative rail disturbances, with output ripple significantly lower than the differential signal gain.

Physical Interpretation:

The nPSRR result highlights the amplifier's sensitivity to ground disturbances, especially in low-frequency bands. For applications involving noisy ground planes, battery-powered systems, or mixed-signal SoCs, additional techniques such as:

- Common-mode feedback
- On-chip regulation

To a more scientific and strict criteria, it may be required to enhance nPSRR performance. The observed zero-pole separation is typical in multi-stage amplifiers with Miller compensation or parasitic feedback paths, and does not compromise the amplifier's suitability for precision analog applications.

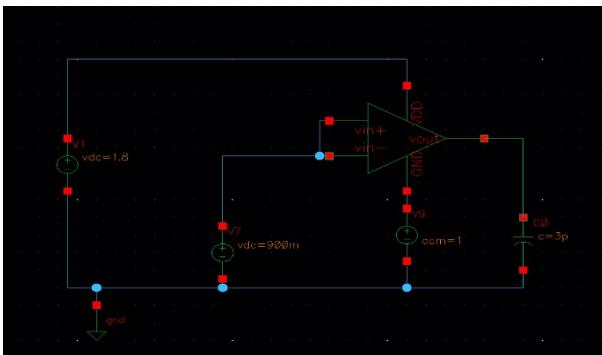


Fig. 16. The testbench used for the nPSRR test

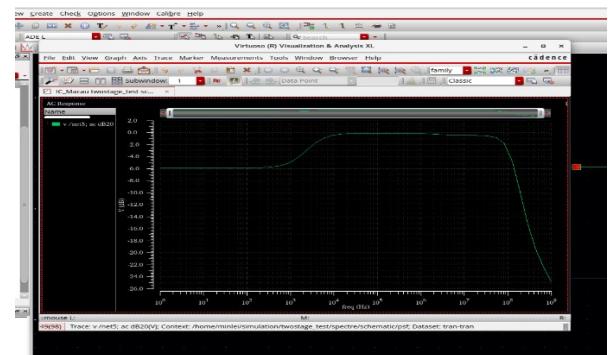


Fig. 17. AC simulation result for nPSRR

6. Temperature Drift Test

The temperature drift test evaluates the amplifier's performance stability across a wide temperature range. Key metrics include output magnitude variation and phase margin degradation, which directly affect gain accuracy, loop stability, and long-term reliability in precision analog systems.

Simulation Setup:

The test was conducted using the Basic test schematic same as Part 1.2 , with ambient temperature continuously swept from -45°C to $+180^{\circ}\text{C}$. The amplifier was biased under nominal conditions same as Part 1.2.

The output was monitored under differential input to isolate thermal drift effects. The waveform viewer captured both output magnitude in dB20 and phase response across the temperature range.

Result Analysis and Interpretation:

The Temperature drift simulation plot is shown in Fig. 18. .The green curve represents the output magnitude in dB20, showing a gradual increase as temperature rises from -45°C to $+180^{\circ}\text{C}$. The purple curve represents the phase response.

- Output Magnitude (Green Curve)

The output magnitude increases gradually with temperature, indicating a slight gain enhancement at higher temperatures. This behavior is attributed to increased carrier mobility and bias current in MOS devices. The rise is smooth and monotonic, with no abrupt jumps, confirming thermal stability.

b. Phase Response (Purple Curve)

The phase decreases steadily with temperature, reflecting a reduction in phase margin. This is typical in analog amplifiers, as parasitic capacitance and bias current variation shift the unity-gain frequency and introduce additional phase delay.

Phase Margin Extraction:

The phase margin is manually extracted at five representative temperature points using: $PM =$

$$180^\circ - \angle V_{out}$$

Temperature (°C)	Phase Margin (°)
-45	61.998
-25	60.773
-5	59.411
15	58.376
180	52.011

The total drift is:

$$\Delta PM = 61.998^\circ - 52.011^\circ = 9.987^\circ$$

This reduction approximately equaling to 10° is modest and remains within acceptable limits for most analog designs, but may require compensation in high-temperature environments.

Design Implications:

- The amplifier exhibits **predictable and monotonic thermal behavior**, with no instability or abrupt gain/phase transitions.
- The observed phase margin drift suggests that loop stability weakens slightly at high temperatures, but remains within safe margins.

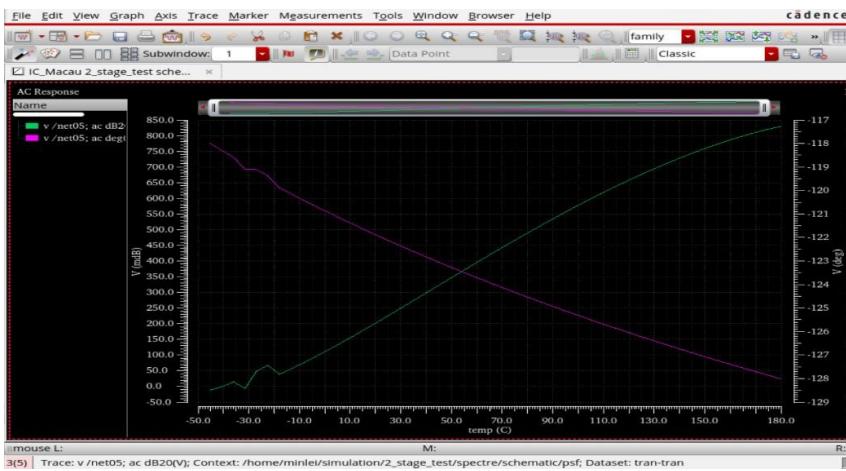


Fig. 18. Temperature drift simulation result

V. CONCLUSION

- This report presents the design and simulation of a two-stage analog amplifier targeting high gain, stable operation, and robust power supply rejection. Through comprehensive AC, DC, transient, and temperature drift simulations, the amplifier demonstrates reliable performance across key metrics.
- The amplifier achieves strong open-loop gain and wide bandwidth, making it suitable for general-purpose analog frontend applications. DC sweep analysis reveals a clear common-mode input range (CMIR) from 950 mV to 1.05 V,

ensuring linear operation across a substantial portion of the 1.8 V supply. Transient simulation confirms an output swing from 34.493 mV to 1.7835 V , indicating near rail-to-rail capability.

3. Temperature drift testing shows predictable behavior: output magnitude (dB20) increases slightly with temperature, while phase margin decreases modestly from 61.998° to 52.011° across $-45\text{ }^\circ\text{C}$ to $+180\text{ }^\circ\text{C}$. These trends reflect stable thermal characteristics and acceptable loop stability under elevated temperatures.

To summarize the amplifier's simulated performance, key metrics are listed below:

Power Consumption	$552.54\text{ }\mu\text{W}$
Open-Loop DC Gain	86.6356 dB
Unity-Gain Bandwidth (UGBW)	112.94 MHz
Phase Margin	57.17°
Slew Rate (SR)	$35.72\text{ V}/\mu\text{s}$
Common-Mode Rejection Ratio (CMRR)	84.3671 dB
Negative Power Supply Rejection Ratio (nPSRR)	82.513 dB
Output Swing	$34.493\text{ mV} - 1.7835\text{ V}$