

Hardware Implementation of Polyphase-Decomposition-Based Wavelet Filters for Power System Harmonics Estimation

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Abstract—Computational time and hardware resource are key issues in hardware implementation of any signal-processing algorithm. This paper presents the design and implementation of a polyphase-decomposition-based new architecture of wavelet filter for power system harmonics estimation using discrete wavelet packet transform (DWPT). Usually, DWPT provides coefficients as the output; however, the proposed architecture also includes provision for providing root mean square values directly. The proposed method reduces computational requirements and save memory resources. Xilinx system generator, a higher abstraction level tool, has been used to simulate and implement the proposed scheme on the Xilinx Artix-7 field-programming gate array AC701 board. Performance of the proposed architecture has been validated and compared through hardware cosimulation with variety of synthetic and experimental signals.

Index Terms—Discrete wavelet packet transform (DWPT), field-programming gate array (FPGA), finite impulse response (FIR) filter, power quality (PQ), root mean square (rms), Xilinx system generator (XSG).

I. INTRODUCTION

RAPID growth in high-power semiconductor devices and power electronic converters facilitate more efficient and better utilization of distributed and renewable energy sources in modern power system. However, extensive use of power-electronics-based nonlinear loads and process control equipment in residential, commercial, and industrial sectors causes a severe problem of power supply waveform distortion and injection of harmonics and interharmonics into the system [1], [2]. Due to significant rise in nonlinear loads, stringent regulations [3], sensitive devices, and increased consumer awareness, power system research community has shown considerable interest in power quality (PQ) monitoring and control [2], [4]–[6]. In one of the reports on modern grid initiative, PQ has been identified as one of the seven principal characteristics in a systems view of the modern grid [7]. Amongst many PQ issues, waveform distortion is considered as more severe because it leads to many other operational problems, such as increased losses, malfunctioning of protection

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and control circuits, and interference with communication line. Therefore, as a requirement of smart electricity transmission and distribution systems, accurate estimation, monitoring, and control of waveform distortion are very important.

The IEC standard 61000-4-7 [8] recommends the fast Fourier transform (FFT) as a basic signal-processing tool for the estimation of magnitudes of fundamental and harmonic components. However, FFT has its own limits and restriction and produces inaccurate results in case of nonstationary signal, especially fundamental frequency variation [9]. In addition, computing groups and subgroups need additional computation. Many signal-processing tools have been proposed for harmonic estimation of nonstationary signal, such as windowed and interpolated discrete Fourier transform (DFT) [10]–[13], wavelet transforms (WTs) [14]–[20], Hilbert–Huang transform (HHT) [20], [21], Kalman filter (KF) [22], Prony/Multiple Signal Classification (MUSIC) [23], sliding-window Estimation of Signal Parameters via Rotational Invariance Technique (ESPRIT) [24]–[26], and neural networks [27]–[30]. Each of these has their own pros and cons [31] and is suitable for different applications. The HHT is preferred for nonlinear and nonstationary data because it uses adaptive basis functions for decomposition; however, additional tools are required for exact interpretation of the results and its accuracy is dependent on the exact spline fitting, which is difficult. KF can be applied for continuous tracking of time-varying harmonics, but exact modeling is required for accurate results. One of the drawbacks of KF is the problem of filter dropping off, which makes it insensitive against sudden changes of state variables if the estimation parameters are not changing for a long time. The parametric techniques, such as Prony, MUSIC, and ESPRIT, provide high-resolution estimates with relatively short data sample size. Further, these techniques do not require synchronized sampling and specific number of data samples; however, their high computational time and sensitivity to noise and modeling errors restrict their application for online cases.

Easy implementation using filters banks provides an edge to the WT over others for many online practical applications. As a result, WT has been successfully applied in number of applications for the analysis of a signal in time-frequency domain. Because of digital implementation, discrete WT (DWT), and hence, discrete wavelet packet transform (DWPT) is more popular in analysis of power system harmonics [14]–[16]. Although, the reported WPT-based methods

claimed satisfactory performance, and their hardware implementation confronts with many issues, such as very high computational complexity, response time, and high hardware resources requirement. There have been works [32], [33] on hardware implementation of WT, which are focused on audio signal and image processing applications. Garcia *et al.* [34] have proposed a flexible architecture for WPT implementation; however, it is not optimized for power system harmonics estimation because it is a generalized approach in modular form that is suitable for medical imaging applications. Further, this paper does not discuss anything about quantization of coefficient. It is obvious fact that high precision floating-point filter coefficients provide more accurate results, even for quantized input signal, compared with fixed-point quantized coefficients; however, the hardware requirements rise enormously [33]. A cost effective instrument implementation has been proposed in [35] that is based on digital filter bank approach [36]. It adopts second-order Butterworth digital filter. The major concern in this paper is inherent drawbacks of Butterworth filter, such as possibility of instability due to quantization error and nonlinear phase response. In contrast, finite impulse response (FIR) filters have increasing signal resolution, a linear phase, and inherent stability; however, the required filter order is higher leading to greater delay.

This paper proposes a polyphase and transpose form structure-based digital implementation of DWPT using FIR filter bank architecture for power system harmonics estimation. The symmetry of the FIR filter has been exploited to implement an optimal form of the filter bank using resource sharing with polyphase decomposition. Downsampling before the filtering operation reduces the computations and makes the response faster. The proposed scheme has been successfully implemented on Xilinx Artix-7 field-programming gate array (FPGA) AC701 board after proper synthesis in Xilinx system generator (XSG)/Simulink domain. The proposed hardware design not only minimizes the computational requirements relative to similar designs but also provides stable operation and linear phase response. The performance of the proposed hardware implementation has been validated using various synthetic and experimental test signals in hardware cosimulation environment.

II. FPGA-BASED HARMONIC ESTIMATION APPROACH

A. Review of Discrete Wavelet Packet Transform

The DWPT, a more general form of the DWT, is the preferred technique for harmonic estimation as it provides uniform frequency bands and can be easily implemented using multistage filter bank. With adequate sampling frequency and wavelet decomposition tree, output frequency band from a DWPT can be aligned to the specific harmonic components for measuring their magnitudes [15]. Fig. 1 depicts a three-level decomposition tree that provides eight frequency bands.

The filter bank consists of wavelet functions as the low-pass filter $h(n)$ and its dual high-pass filter $g(n)$. The decomposition is performed on both the approximation coefficient and detail coefficient of the input signal at any level. The

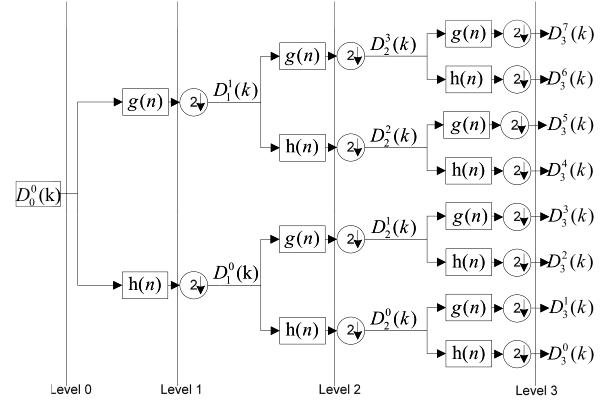


Fig. 1. Three-level DWPT decomposition tree.

wavelet coefficients of input signal at the l th level, k th point, and $2i$ th node can be represented as

$$D_l^{2i}(k) = \sum_n h(n) D_{l-1}^i(2k - n) \quad (1)$$

$$D_l^{2i+1}(k) = \sum_n g(n) D_{l-1}^i(2k - n) \quad (2)$$

where $i = 0, 1 \dots (2^{l-1} - 1)$ and $h(n)$ and $g(n)$ are low-pass and high-pass filters, respectively. The wavelet coefficient at any level is retrieved from the convolution of input signal sequence at previous level with low-pass/high-pass filter and then downsampling by a factor of two.

The accuracy of harmonic measurement depends upon the choice of mother wavelet. Since the choice of mother wavelet depends upon the required application and its properties, Vaidyanathan with 24 coefficients [37], db20 with 40 coefficients [15], and db10 with 20 coefficients [16] have been proposed as the most suitable mother wavelet for power system harmonic analysis; however, the authors have not included the quantization effect of filter coefficients for wavelet filter in their analysis, which is an important parameter during hardware implementation. In general, a large number of filter coefficients provide more accurate harmonic measurement due to low spectral leakage, but it requires considerable amount of resources and more computation, which reduce the speed of computational process. The main objective of this paper is to study quantization effect, reduce computational complexity, and required resources for its efficient implementation on hardware.

B. Polyphase Implementation of Wavelet Filters

Convolution between input sample and coefficient of filter can be implemented through polyphase structure or nonpolyphase structure as shown in Fig. 2 [33]. Equations (1) and (2) are wavelet coefficients of input signal using nonpolyphase structure. In nonpolyphase, structure computations between input samples and filter coefficients are done before downsampling as shown in Fig. 2(a), while in polyphase, computations between input samples and filter coefficients are done after downsampling as shown in Fig. 2(c), as a result, the computations are reduced by a factor of

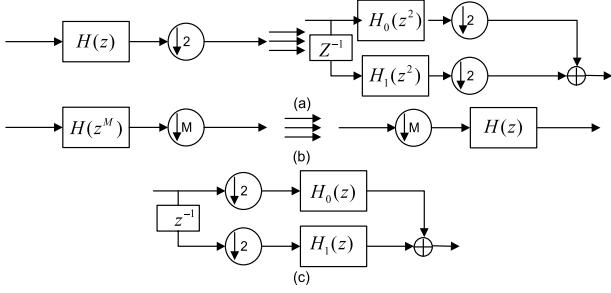


Fig. 2. (a) Nonpolyphase implementation of transfer function $H(z)$. (b) Noble identity. (c) Polyphase implementation of transfer function $H(z)$.

two in polyphase structure. Transfer function of a filter can be expressed as

$$H(z) = h_0 + h_1 z^{-1} + h_2 z^{-2} + \dots + h_{(N-2)} z^{-(N-2)} + h_{(N-1)} z^{-(N-1)}. \quad (3)$$

Above mathematical equation can be rearranged as a sum of two terms, the first term from the even indexed coefficients and the second term from the odd indexed coefficients. Then, it can be expressed as

$$H(z) = h_0 + h_2 z^{-2} + h_4 z^{-4} + \dots + h_{(N-3)} z^{-(N-3)} + h_{(N-1)} z^{-(N-1)} + z^{-1}(h_1 + h_3 z^{-2} + \dots + h_{(N-4)} z^{-(N-5)} + h_{(N-2)} z^{-(N-3)}). \quad (4)$$

Combining odd and even terms separately, (4) can be expressed as sum of two phase components $H_0(z)$ and $H_1(z)$ as

$$H(z) = H_0(z^2) + z^{-1} H_1(z^2) \quad (5)$$

where

$$H_0(z) = h_0 + h_2 z^{-1} + \dots + h_{(N-3)} z^{-(N-3)/2} + h_{(N-1)} z^{-(N-1)/2} \quad (6)$$

$$H_1(z) = h_1 + h_3 z^{-1} + \dots + h_{(N-4)} z^{-(N-5)/2} + h_{(N-2)} z^{-(N-3)/2}. \quad (7)$$

Using noble identity as shown in Fig. 2(b), efficient polyphase implementation of FIR filter is possible as shown in Fig. 2(c).

C. Cost Effective Implementation of Polyphase Structure

It is known that infinite impulse response (IIR) filter requires lesser hardware resources because of low filter order. However, for ensuring stable operation even with quantization and linear phase response, FIR filters are better choice. Therefore, FIR filters are chosen for DWPT implementation in this paper, and suitable techniques such as polyphase and transposed form structure have been used to make hardware implementation competitive with that of the IIRs.

Usually, the number of computations and memory requirements determine the cost of implementation of any algorithm. In order to save memory on FPGAs, polyphase structure is used, which makes it possible to reduce the delay elements in FIR filter and the number of computations is also reduced to half. Similarly, transposed form structure is better option than

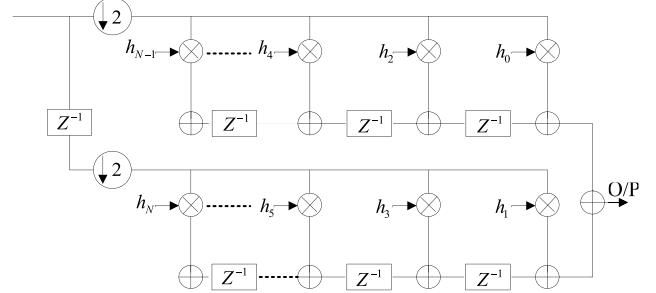


Fig. 3. Polyphase implementation of FIR filter $H(z)$ in transposed form.

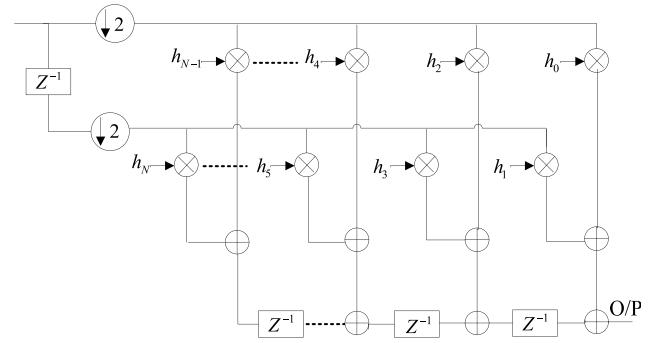


Fig. 4. Proposed polyphase structure in transposed form.

TABLE I
COMPARISON OF COMPUTATIONAL COMPLEXITY

Wavelet filter	Number of multiplications (additions)	
	For [15]	For the proposed work
db20	76800 (74880)	38400 (37440)
db30	115200 (113280)	57600 (56640)
DFT (320 points)		
Radix-2 FFT	4608 (9216)	
Direct DFT	102400 (102080)	

direct form structure [38] for FIR filter implementation for high-speed hardware such as FPGAs or application-specified integrated circuits. Fig. 3 shows the polyphase implementation of FIR filter in transposed form as used in this paper.

Two polyphase components of transfer function $H(z)$ can be implemented in transposed form structure as depicted in Fig. 3. Samples from the two delay strings are combined together for getting output. Therefore, separate delay string can be mixed together into a single one. In this way, polyphase structure save considerable resources on implementation, as presented in Fig. 4.

Computational complexity is defined as the number of multiplications and additions per input sample, if there are N coefficients in filter, and then N multiplications and $N - 1$ additions per input sample are required for a single filter. For comparison purpose, the number of multiplications and additions required for total ten cycles' data at sampling rate of 32 samples per cycle for the DFT and a three-level DWPT with two different mother wavelets, namely, db20 and db30, are listed in Table I. It can be noticed that computational complexity is reduced by half with the proposed implementation.

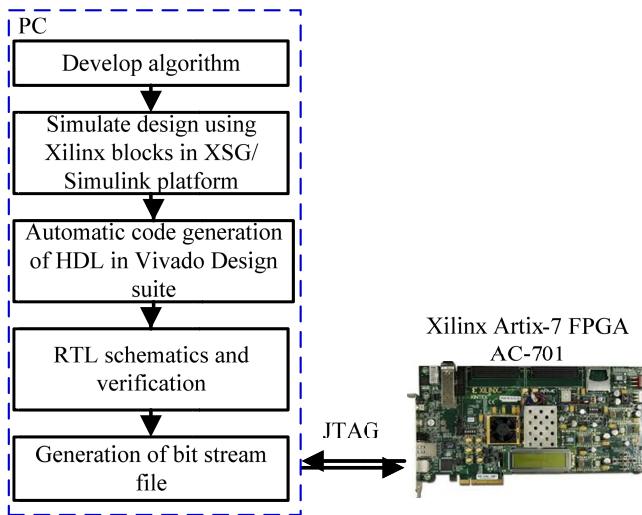


Fig. 5. Design and implementation flow.

The number of computations is considerably small for the Radix-2 FFT; however, its accuracy is low because of spectral leakage due to noninteger number of cycles and/or zero padding for meeting the requirement of power-of-two N (i.e., $N = 2^v$). In Table I, the number within parenthesis represents the required number of additions.

III. FPGA-BASED DESIGN FOR HARMONIC ESTIMATION

This section explains model-based design approach to rapidly implement harmonic estimation algorithm with the proposed hardware structure on FPGA platform. This section also describes the steps used for modeling, simulating, implementing, and verifying the proposed scheme in real time using the Xilinx Artix-7 FPGA AC701 board, connected to a PC with MATLAB/Simulink, XSG, via JTAG interface.

Fig. 5 shows design and implementation flow using XSG. Digital design for the DWPT-based harmonic estimation on the XSG for its implementation on FPGA is shown in Fig. 6. It enables hardware cosimulation through the Gateway In and Gateway out blocks that Simulink data types (integer, double, single, and fixed) into system generator data types (fixed point or floating point) and vice versa. These define top-level input and output ports, respectively, and acts as virtual analog-to-digital and digital-to-analog converters during hardware cosimulation. Registering the input and output data has been used that allows the register to be packed into input–output buffer [39].

Wavelet Filter: Daubechies filter coefficients are used for implementation of wavelet FIR filters. Wavelet filters are implemented on FPGA using transposed polyphase form architecture. Fig. 7 shows digital design of six-tap FIR filter in transposed form, and the proposed digital design with polyphase structure is shown in Fig. 8. Filter coefficients are quantized using 2's complement signed 18-bit fixed-point format having 12 fractional bits with adequate quantization and overflow option in order to save resource utilization on FPGA. Pipelining process is also used in both architecture for higher performance FPGA design; therefore, all the timing constraints are met for Xilinx Artix-7 FPGA AC701 board for

a clock frequency of 50 MHz. The Cast blocks are necessary to transform output signal from wavelet filter to an 18-bit fixed-point format (the same that the input of Gateway in block).

RMS Calculation: The root mean square (rms) magnitude of fundamental and each odd harmonics can be calculated by taking square root of the mean square of wavelet coefficients obtained from the wavelet filter. Digital architecture for rms calculation is developed as proposed in [40] and its digital design shown in Fig. 9. Convert block is used for converting 18-bit fixed-point format into single precision floating point format, because divide and square root block available from Xilinx support only for single precision floating format and double precision floating point format.

The architecture has been synthesized and implemented on FPGA by XSG/Vivado design suite 2015.1 using db20 and db30 wavelet filters, Table II shows resource utilization summary for above architecture with 18-bit fixed-point format. It can be observed that the proposed polyphase transpose form require less resources (FF, LUT, memory LUT) in comparison with traditional transpose form in both cases, viz., db20 and db30.

IV. PERFORMANCE EVALUATION

In this section, the simulation and experimental results have been presented to investigate performance of the digital hardware based on the proposed method for power system harmonic estimation. Synthetic and measured test signals have been used with cost effective hardware cosimulation approach on the experimental setup consisting of MATLAB/Simulink software platform (running on a desktop personal computer with 2.4-GHz Intel core i5 processor, with 4-GB random access memory), and Xilinx Artix-7 FPGA AC701 board as hardware platform, both interconnected via JTAG.

Synthetic signals are generated in MATLAB/Simulink platform and sampled at 1.6 kHz rate with window width of 200 ms (ten cycles of the fundamental frequency) in accordance with the IEC standard 61000-4-7 [8]. The signal that is generated in the MATLAB/Simulink is in double precision floating point format and it is quantized by Gateway In block in 18-bit fixed-point format to feed it to the implemented algorithm on the Xilinx Artix-7 FPGA AC701 hardware board, in real time, with the help of cosimulation process.

A. Test 1: Stationary Signal

First test examines the performance of the implemented digital hardware on stationary signal at nominal and off-nominal fundamental frequencies. The synthesized signal was composed of odd integer harmonics along with the fundamental component, as shown in Fig. 10, and is generated using (8) at three different fundamental frequency values of 49.5, 50, and 50.5 Hz. In (8), $\omega = 2\pi f$, where f is the fundamental frequency

$$V(t) = \sqrt{2} \times [\sin(\omega t) + 0.2 \sin(3\omega t) + 0.2 \sin(5\omega t) + 0.1 \sin(7\omega t) + 0.1 \sin(11\omega t) + 0.1 \sin(13\omega t)]. \quad (8)$$

Table III reports the results obtained from the proposed method for db20 and db30 as a wavelet filter coefficients

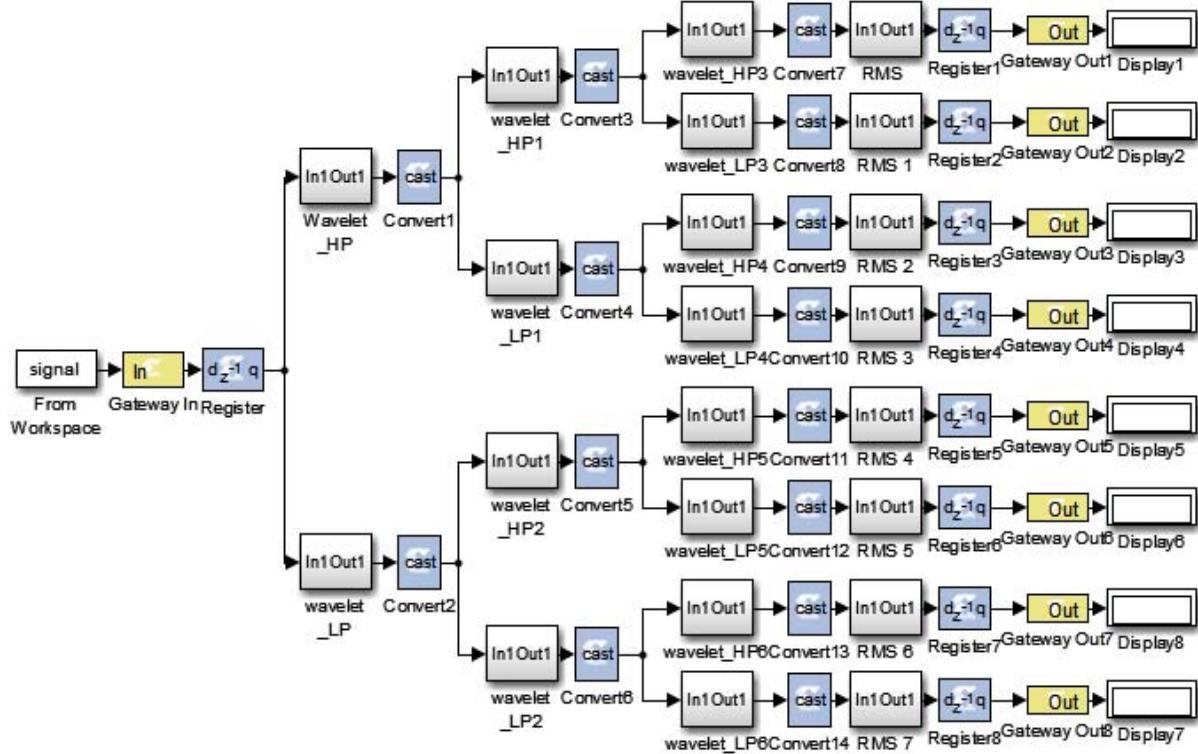


Fig. 6. Digital design of three-level DWPT decomposition tree on XSG.

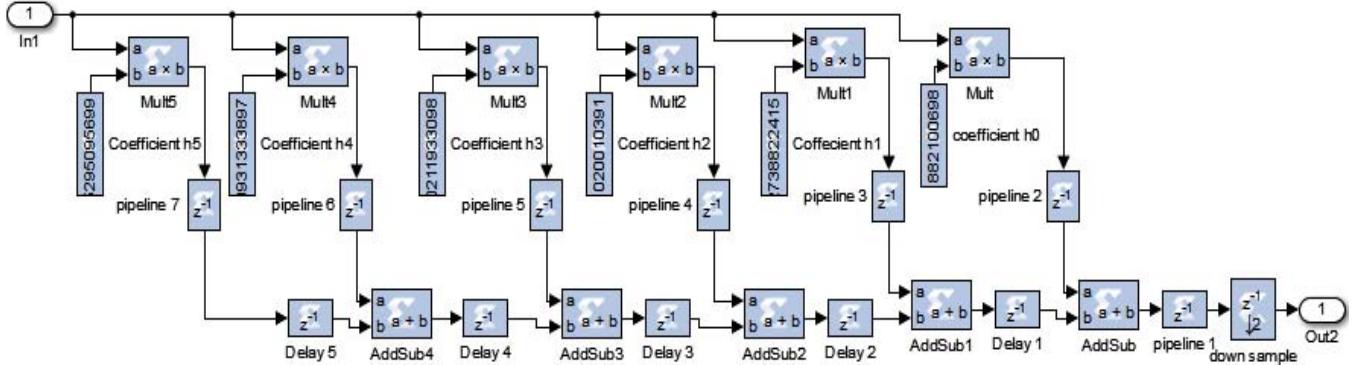


Fig. 7. Digital design of six-tap FIR filter in traditional transposed form on XSG.

at three different fundamental frequency values. Table IV provides the performance comparison of the proposed method with that of DFT and IEC harmonic group (HG) method in terms of estimation error. It can be observed that absolute estimation error is negligible for the DFT and IEC HG method for idealistic case of nominal fundamental frequency, whereas the error increases significantly for off-nominal fundamental frequency cases. Although, these noncoherency errors can be reduced using interpolated DFT, and the proposed method performance is better at off-nominal fundamental frequency cases. Response time of the proposed method is presented in Table V, which indicates suitability of the proposed method for online applications.

B. Test 2: Nonstationary Signal (Amplitude Step Change)

Second test signal, with an amplitude step change, is taken from the IEC standard [8] (Example-1 of section C.3) to illustrate the robustness of the proposed digital hardware for

fluctuating harmonic amplitude. In this example, the signal contains only fifth harmonic that is changed from 3.536A (rms) to 0.7071A (rms) at 21.25 periods of fifth harmonic, as shown in Fig. 11. Average of rms value of the test signals is computed over ten cycle of fundamental frequency, which comes out to be 2.355 A (at 1.6-kHz sampling frequency), and it is used for comparison of the results obtained from the proposed architecture.

To validate the robustness of the proposed method against noise, a zero mean white Gaussian noise (WGN) with signal-to-noise ratio (SNR) of 60 and 40 dB is added into the signal and test is repeated for 25 times. Table VI reports the resulting mean values and standard deviation (SD) of the estimated rms amplitudes for this test signal using the proposed polyphase-decomposition-based method on Xilinx Artix-7 FPGA AC701 board with db20 and db30 wavelet filter coefficients. The respective estimation errors for the proposed method, DFT, and IEC-based HG and harmonic subgroup

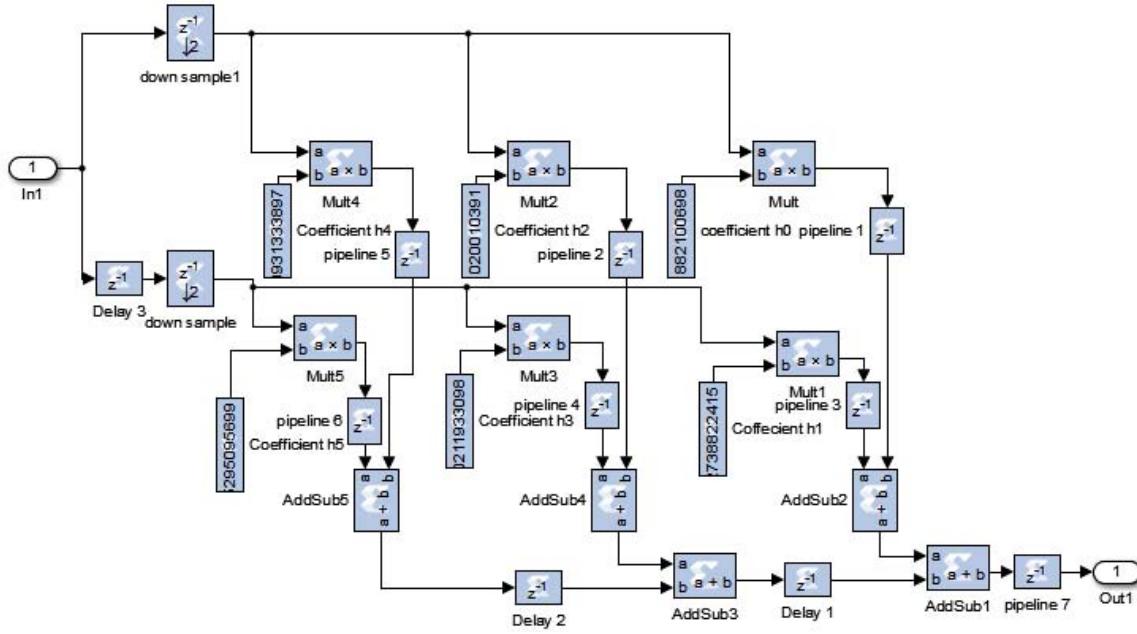


Fig. 8. Proposed digital design of six-tap FIR filter in polyphase transposed form on XSG for improved performance.

TABLE II
RESOURCE UTILIZATION SUMMARY AFTER IMPLEMENTATION FOR XILINX ARTIX-7 FPGA AC701 BOARD

Resource type	Utilization				Available
	(db20)	Proposed polyphase transpose form	(db30)	Proposed polyphase transpose form	
FF	57009 (21.3 %)	38655 (14.45 %)	91309 (34.12 %)	57219 (21.38 %)	267600
LUT	43624 (32.6 %)	35208 (26.31 %)	67667 (50.57 %)	49165 (36.75 %)	133800
Memory LUT	180 (0.39 %)	178 (0.39 %)	183 (0.40 %)	182 (.39 %)	46200
I/O	2 (0.50 %)	2 (0.50 %)	2 (0.50 %)	2 (0.50 %)	400
BRAM	2 (0.55 %)	2 (0.55 %)	2 (0.55 %)	2 (0.55 %)	365
BUFG	4 (12.5 %)	4 (12.5 %)	4 (12.5 %)	4 (12.5 %)	32
MMCM	1 (10 %)	1 (10 %)	1 (10 %)	1 (10 %)	10

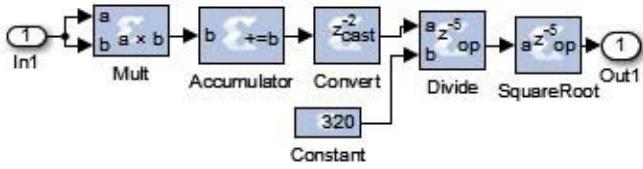


Fig. 9. Digital design of rms block based on DWPT.

algorithms are presented in Table VII. It can be noticed that due to spectrum leakage, DFT performs poorly, which is taken care to some extent by the IEC grouping methods, but the results of the proposed method are much better.

C. Test 3: Measured Voltage Signal

In this test case, a measured voltage signal of a distribution system of an academic institution has been considered. The voltage has been measured at a low voltage feeder of the power and control lab and the measurement point (MP) is marked in the single line diagram of the distribution system, shown in Fig. 12. The signals have been acquired at the designated MP using the Agilent made differential voltage

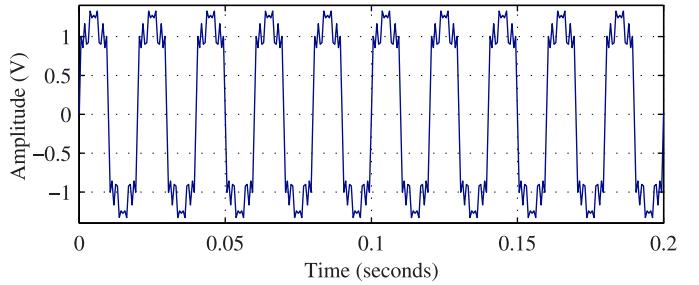


Fig. 10. Test signal 1: synthetic stationary signal.

probe (N2791A) and data acquisition system (U2353A) at the sampling rate of 6.4 kHz, which is downsampled by a factor of four to suit the proposed method. Fig. 13 shows few cycles of the measured voltage signal, which is attenuated during acquisition by a factor of 180.

The acquired voltage signal of approximately 1-s duration is analyzed using the proposed method with window width of 200 ms and the obtained mean and SD values of estimates

TABLE III
HARMONIC AMPLITUDE ESTIMATION RESULTS USING db20 AND db30 ON FPGA FOR STATIONARY SIGNAL

Frequency band (Hz)	Harmonic order	True RMS (V)	Proposed Polyphase form db20 (V)			Proposed Polyphase form db30 (V)		
			(49.5Hz)	(50Hz)	(50.5Hz)	(49.5Hz)	(50Hz)	(50.5Hz)
0-100	1st	1.0000	1.00075	1.001109	1.002164	1.000422	1.000287	1.00229
100-200	3rd	0.2000	0.203883	0.184515	0.210335	0.20113	0.194638	0.204865
200-300	5th	0.2000	0.195304	0.209739	0.196598	0.195922	0.200691	0.198114
300-400	7th	0.1000	0.095852	0.09324	0.092564	0.097975	0.096136	0.096327
400-500	9th	0.0000	0.033938	0.036387	0.040343	0.025253	0.029622	0.029733
500-600	11th	0.1000	0.098872	0.091862	0.100767	0.098643	0.096101	0.100894
600-700	13th	0.1000	0.099425	0.107863	0.101218	0.100212	0.103237	0.100884
700-800	15th	0.0000	0.017927	0.01858	0.014448	0.01697	0.018943	0.014935

TABLE IV
ABSOLUTE ESTIMATION ERROR (%) FOR THE STATIONARY TEST SIGNAL 1

Frequency band (Hz)	Harmonic order	Proposed Polyphase form db20 (V)			Proposed Polyphase form db30 (V)			DFT			IEC HG		
		(49.5Hz)	(50Hz)	(50.5Hz)	(49.5Hz)	(50Hz)	(50.5Hz)	(49.5Hz)	(50Hz)	(50.5Hz)	(49.5Hz)	(50Hz)	(50.5Hz)
0-100	1st	0.075	0.1109	0.2164	0.0422	0.0287	0.229	2.754	1.8e-10	0.939	1.311	1.8e-10	0.463
100-200	3rd	0.3883	1.5485	1.0335	0.113	0.5362	0.4865	3.554	1.0e-10	3.883	0.958	1.0e-10	1.220
200-300	5th	0.4696	0.9739	0.3402	0.4078	0.0691	0.1886	9.869	4.0e-11	10.68	2.010	4.0e-11	2.233
300-400	7th	0.4148	0.676	0.7436	0.2025	0.3864	0.3673	8.654	2.5e-11	9.758	0.771	2.5e-11	0.422
400-500	9th	3.3938	3.387	4.0343	2.5253	2.9622	2.9733	0.580	5.4e-12	0.763	1.004	1.4e-12	1.323
500-600	11th	0.1128	0.8138	0.0767	0.1357	0.3899	0.0894	12.432	9.0e-11	12.364	0.367	8.3e-11	0.424
600-700	13th	0.0575	0.7863	0.1218	0.0212	0.3237	0.0884	10.535	1.3e-10	11.212	0.916	1.3e-10	1.423
700-800	15th	1.7927	1.858	1.4448	1.697	1.8943	1.4935	0.726	1.7e-10	0.301	1.258	3.0e-10	0.522

TABLE V

CLOCK CYCLES REQUIRED FOR ESTIMATION OF POWER SYSTEM HARMONICS FOR TEST SIGNAL 1

Harmonic order	Clock cycles	FPGA (μ s)
1st	643	12.86
3rd	515	10.30
5th	443	8.86
7th	563	11.26
11th	419	8.38
13th	650	13.0

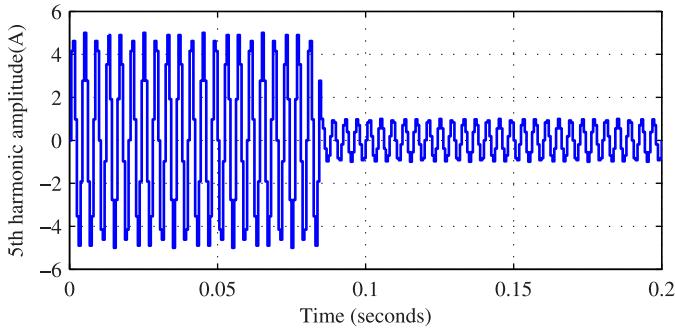


Fig. 11. Test signal 2: synthetic fifth harmonic current signal with large step change.

of the harmonic components are presented in Table VIII. The measured signal at original sampling rate (6.4 kHz) has been analyzed with the high resolution parametric method [25] whose results were assumed as the true values for computing the errors, which are also provided in Table VIII. It is worth mentioning here that accuracy of the true values have been confirmed using very low values of the reconstruction

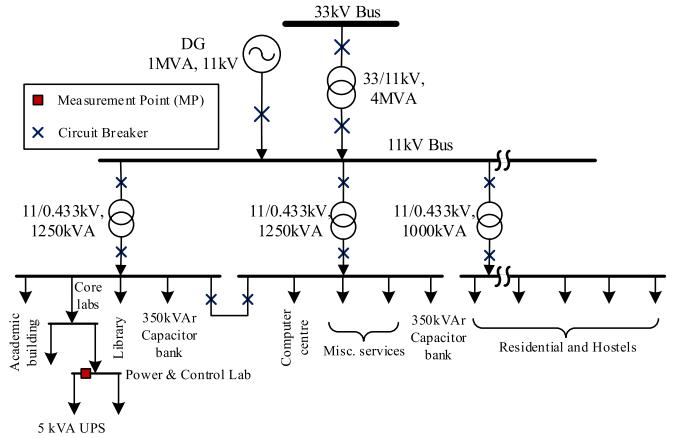


Fig. 12. Single line diagram of the distribution system for voltage signal acquisition.

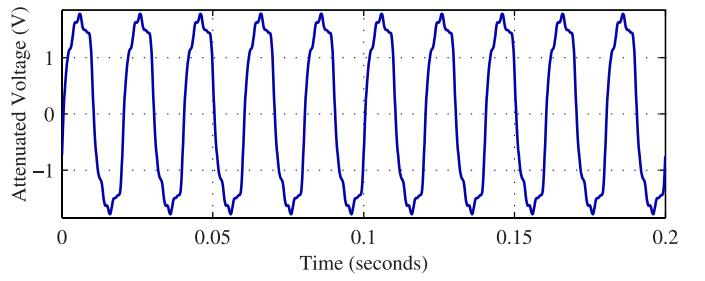


Fig. 13. Test signal 3: acquired voltage signal.

error with these values. The low values of absolute error and SD confirms accuracy and reliability of the proposed method.

TABLE VI
AMPLITUDE ESTIMATION RESULTS FOR TEST SIGNAL 2 WITH ZERO MEAN WGN

Output bands (Hz)	Proposed Polyphase form db20 (A) rms with SNR 40 dB		Proposed Polyphase form db30 (A) rms with SNR 40 dB		Proposed Polyphase form db20 (A) rms with SNR 60 dB		Proposed Polyphase form db30 (A) rms with SNR 60 dB	
	Mean	SD	Mean	SD	Mean	SD	Mean	SD
0-100	0.117292	5.97E-07	0.104968	1.85E-06	0.11691	1.19E-08	0.104882	2.41E-08
100-200	0.280804	8.04E-07	0.197095	2.31E-06	0.280617	1.16E-08	0.197153	3.28E-08
200-300	2.327735	1.68E-06	2.335735	1.2E-06	2.327336	3.79E-08	2.336099	2.27E-08
300-400	0.197501	1.43E-06	0.178756	1.46E-06	0.196901	2.76E-08	0.178798	2.27E-08
400-500	0.085733	1.39E-06	0.110171	1.64E-06	0.085384	2.69E-08	0.109831	2.06E-08
500-600	0.080251	1.12E-06	0.058976	1.58E-06	0.079823	4.25E-08	0.058075	4.5E-08
600-700	0.045236	1.13E-06	0.054812	1.59E-06	0.044866	2.17E-08	0.054032	2.44E-08
700-800	0.049069	1.26E-06	0.04808	1.44E-06	0.048791	1.54E-08	0.047361	2.83E-08

TABLE VII
ERRORS (%) IN AMPLITUDE ESTIMATION OF FIFTH HARMONIC OF TEST SIGNAL 2

Proposed Method	SNR 40.45 dB	Error	
		db20	db30
	SNR 57.4 dB	db20	.17
		db30	.80
IEC Standard	Harmonic group (without any noise)		1.47
	Harmonic subgroup (without any noise)		3.84
DFT	(as reported in IEC 61000-4-7)		19.3

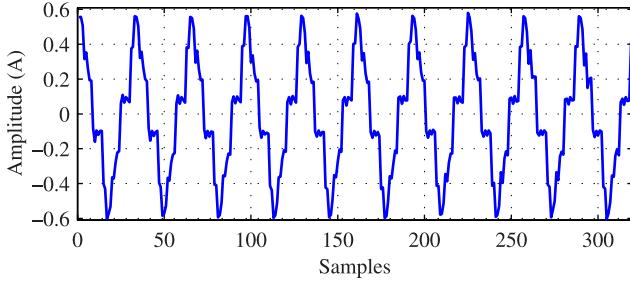


Fig. 14. Test signal 4: measured current signal.

D. Measured Real Time Current Signal

A real time measured current signal from [29], shown in Fig. 14, is considered as the fourth test signal for validation of the proposed digital hardware with actual experimental signal at off-nominal fundamental frequency. As reported in [29] and confirmed through simulation results, the measured current signal was composed of four dominant harmonics, namely, fundamental, 3rd, 5th, and 11th harmonics. In this signal, fundamental frequency is also not at nominal value of 50 Hz and deviates between 49.94 and 50.12 Hz. The proposed method has been applied on the real current signal of total 5-s duration with the window width of 200 ms and the results are presented in Table IX. It can be observed that estimates harmonic amplitudes are accurate and consistent.

E. Effect of Gaussian Noise on Estimation

Real-time measurements invariably introduce noise that can be significant or reasonable depending up on the quality of the measuring instruments. Therefore, it is important to evaluate uncertainty of estimations due to noise. For this purpose,

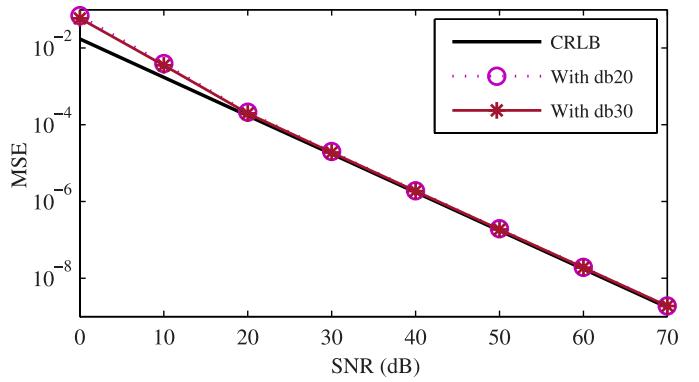


Fig. 15. MSE plot for fifth harmonic amplitude estimation.

a WGN with zero mean and variance σ^2 is added in the signal model; and computer simulations have been performed to compute the mean squared error (MSE) in amplitude estimation for 200 independent trials at each noise levels. Fig. 15 depicts the MSE in the fifth harmonic amplitude estimation of test signal 2 from the proposed algorithm using db20 and db30 wavelet filters and compares it with the Cramér–Rao lower bounds (CRLBs). It can be observed that beyond SNR of 20 dB, the MSE is close to the respective CRLBs with both wavelet filters, which confirms estimation accuracy in the presence of noise.

F. Effect of Quantization

Quantization is the necessity of digital systems, which reduces accuracy of computations compared with infinite precision data. With higher resolution, the accuracy will be relatively better; however, it requires significant hardware resources. Therefore, choosing correct resolution is vital for any digital design. For a given system, this choice is to be made for ADCs that converts analog input signal to digital form, and for filter coefficients that participate in computation. Resolution of filter coefficients plays greater role in estimation accuracy compared with ADC. The reason for this can be explained by the fact that in case of power system harmonics estimation, quantization of input signal will cause some amount of error (only at the entry point), however, resolution of the filter coefficients will amplify/introduce errors due to

TABLE VIII
AMPLITUDE ESTIMATION RESULTS FOR TEST SIGNAL 3

Harmonic Component	True value	Proposed Polyphase form db20 (A) rms			Proposed Polyphase form db30 (A) rms		
		Mean	SD	Error (%)	Mean	SD	Error (%)
1st	1.3232	1.3244158	3.45e-06	0.12158	1.3237418	3.69e-06	0.05418
3rd	0.1907	0.1992946	1.28e-05	0.85946	0.1966337	2.47e-06	0.59337
5th	0.1363	0.1342022	7.15e-06	0.20978	0.1361073	4.94e-06	0.01927
7th	0.0521	0.0609209	5.47e-06	0.88209	0.0537878	1.10e-06	0.16878
9th	0.001	0.0169552	1.57e-07	1.59552	0.0269523	3.09e-06	2.59523
11th	0.0353	0.0433732	1.16e-06	0.80732	0.0404838	7.33e-07	0.51838
13th	0.001	0.0171847	3.08e-07	1.61847	0.0215107	4.36e-07	1.05107
15th	0.001	0.019492	1.13e-06	1.8492	0.0139242	8.81e-07	1.29242

TABLE IX
AMPLITUDE ESTIMATION RESULTS FOR THE TEST SIGNAL 4

Harmonic Component	True value	Proposed Polyphase form db20 (A) rms			Proposed Polyphase form db30 (A) rms		
		Mean	SD	Error	Mean	SD	Error
1st	0.3102	0.309361	3.67e-05	0.0839	0.309621	3.66e-05	0.0579
3rd	0.0637	0.070168	2.76e-05	0.6468	0.068465	2.17e-05	0.4765
5th	0.0619	0.056694	3.54e-05	0.5206	0.06114	2.37e-05	0.076
7th	0.0122	0.019034	3e-05	0.6834	0.01527	1.33e-05	0.307
9th	6.6e-4	0.008705	5.39e-05	0.8045	0.016	4.51e-05	1.534
11th	0.0011	0.03048	3.06e-05	2.938	0.02979	3e-05	2.869
13th	5.4e-4	0.01733	4.42e-05	1.679	0.01615	4.85e-05	1.561
15th	0.0016	0.022951	1.7e-05	2.1351	0.022731	1.74e-05	2.1131

EFFECT OF QUANTIZATION DUE TO FILTER COEFFICIENTS AND ADC RESOLUTION TAKING db30 AS FILTER COEFFICIENTS FOR TEST SIGNAL 4

Harmonic order	True value	F fixed 18 12		F fixed 14 10		F fixed 12 8	
		A_fixed_18_12	A_fixed_12_8	A_fixed_18_12	A_fixed_14_10	A_fixed_18_12	A_fixed_12_8
1st	0.3102	0.3096846	0.3096548	0.3084544	0.3084514	0.3084352	0.3062501
3rd	0.0637	0.0703591	0.0705419	0.0706104	0.0706038	0.0713568	0.0723323
5th	0.0619	0.061129	0.0610909	0.0610318	0.0610104	0.0610605	0.0609942
7th	0.0122	0.0150678	0.0151871	0.0153515	0.0153581	0.0167153	0.0168733
9th	6.6e-4	0.0160003	0.0159421	0.015984	0.015948	0.0157827	0.0158678
11th	0.0011	0.0297905	0.0299045	0.0296773	0.0297137	0.0302836	0.0304315
13th	5.4e-4	0.0161503	0.0161539	0.0161709	0.0161832	0.015985	0.0160727
15th	0.0016	0.0221735	0.0227717	0.0261883	0.0262169	0.0278294	0.0277792

truncation of data/accumulation of errors during computations (in multiple points of the processing chain), and hence it affects the accuracy more in processing of low resolution data.

A number of tests were carried out with the test signal 4 with 200-ms (320 samples) window length with different scenarios and combination of ADC and db30 wavelet filter coefficients resolution to illustrate the quantization effect due to filters coefficients and ADC resolution. Table X summarizes the results of this analysis, where F_fixed_18_12 signifies 18-bit fixed-point format having 12 fractional bits, 5 integer bits and 1 sign bit for filter coefficients and A_fixed_18_12 denotes in the same pattern resolution of ADC, and so on for all other cases. It can be observed from Table X that error in estimation of rms amplitude is more affected when resolution of filter coefficients is reduced compared with change in ADC resolution.

V. CONCLUSION

This paper presents an FIR wavelet filter bank-based efficient hardware implementation of DWPT harmonic estimation algorithm based on polyphase decomposition and transpose structure. The proposed design reduces the computational complexity by half, and meets the timing requirements for real time implementation and save significant hardware resources on FPGA implementation. The proposed design was implemented on Xilinx Artix AC701 FPGA board using XSG, and its performance was tested using hardware cosimulation on variety of synthetic and experimental signals of stationary and time-varying nature. The obtained results in terms of accuracy, robustness, hardware resource utilization, and response time confirm utility of the proposed method. The accuracy of the reported results is within the prescribed limit as mentioned in the applicable standards, viz., IEC standard 61000-4-7 [8]. With the reported performance parameters, the proposed

method can find its application in monitoring and source identification of critical harmonics [41], selective harmonic compensation schemes [42], harmonics metering [43], and distortion-based tariff realization.

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