

EE116C/CS151B Homework 5

Problem 1

This exercise is intended to help you understand the relationship between delay slots, control hazards, and branch execution in a pipelined processor. In this exercise, we assume that the following MIPS code is executed on a pipelined processor with a 5-stage pipeline, full forwarding, and a predict-taken branch predictor:

```
                lw r2,0(r1)
label1: beq r2,r0,label2 # not taken once, then taken
                lw r3,0(r2)
                beq r3,r0,label1 # taken
                add r1,r3,r1
label2: sw r1,0(r2)
```

Draw the pipeline execution diagram for this code, assuming there are no delay slots and that branches execute in the EX stage.

	Cycles													
	1	2	3	4	5	6	7	8	9	10	11	12	13	14
I1	IF	ID	EX	MEM	WB									
I2		IF	ID	*	EX	MEM	WB							
I3			IF	*	ID	EX	MEM	WB						
I4					IF	ID	*	EX	MEM	WB				
I5									IF	ID	EX	MEM	WB	
I6										IF	ID	EX	MEM	WB

Problem 2

This exercise examines the accuracy of various branch predictors for the following repeating pattern (e.g., in a loop) of branch outcomes: T, NT, T, T, NT

1. What is the accuracy of always-taken and always-not-taken predictors for this sequence of branch outcomes?

Always-taken predictor:

Actual: T, NT, T, T, NT

Predicted: T, T, T, T, T

Accuracy = $3/5 = 60\%$

Always-not-taken predictor:

Actual: T, NT, T, T, NT

Predicted: NT, NT, NT, NT, NT

Accuracy = $2/5 = 40\%$

2. What is the accuracy of the two-bit predictor for the first 4 branches in this pattern, assuming that the predictor starts off in the bottom left state from Figure 4.63 (predict not taken)?

Actual: T, NT, T, T

Predicted: 0, 1, 0, 0

Accuracy = number of hits / total braches = $1/4 = 25\%$

3. What is the accuracy of the two-bit predictor if this pattern is repeated forever?

For the outcome T, NT, T, T, NT, the predictor is:

1st round: 0, 1, 0, 1, 2

2nd round: 1, 2, 1, 2, 3

3rd round: 2, 3, 2, 3, 3

4th round: 2, 3, 2, 3, 3

We can see that the accuracy = $3/5 = 60\%$.

Problem 3

For the code sequence below, how many cycles would it take to execute this code on the 5-stage pipelined data path with forwarding logic?

```
add r5,r2,r1
lw r3,4(r5)
lw r2,0(r2)
or r3,r5,r3
sw r3,0(r5)
```

Draw the pipeline diagram to answer.

add	IF	ID	EX	ME	WB									
nop		IF	ID	EX	ME	WB								
nop			IF	ID	EX	ME	WB							
lw				IF	ID	EX	ME	WB						
lw					IF	ID	EX	ME	WB					
nop						IF	ID	EX	ME	WB				
or							IF	ID	EX	ME	WB			
nop								IF	ID	EX	ME	WB		
nop									IF	ID	EX	ME	WB	
sw										IF	ID	EX	ME	WB

Problem 4

For the code sequence below, show the pipeline diagram for the following cases:

```

                lw r2,0(r1)
label1: beq r2,r0,label2 # not taken once, then taken
                lw r3,0(r2)
                beq r3,r0,label1 # taken
                add r1,r3,r1
                label2: sw r1,0(r2)

```

a) full forwarding, branches resolved in EX

Cycle	1	2	3	4	5	6	7	8	9	10	11	12	13	14
lw r2,0(r1)	IF	ID	E	M	W									
label1: beq r2,r0,label2		IF	ID	E	M	W								
lw r3,0(r2)			IF	ID	E	M	W							
beq r3,r0				IF	ID	E	M	W						
add r1,r3,r1					IF	ID	-	-	E	M	W			

b) full forwarding, branches resolved in ID

Cycle	1	2	3	4	5	6	7	8	9	10	11	12	13	14
lw r2,0(r1)	IF	ID	E	M	W									
label1: beq r2,r0,label2		IF	ID	E	M	W								
lw r3,0(r2)			IF	ID	E	M	W							
beq r3,r0				IF	ID	-	-	-	E	M	W			
add r1,r3,r1					IF	ID	-	-	-	E	M	W		
label2: sw r1,0(r2)						IF	-	-	-	-	ID	E	M	W