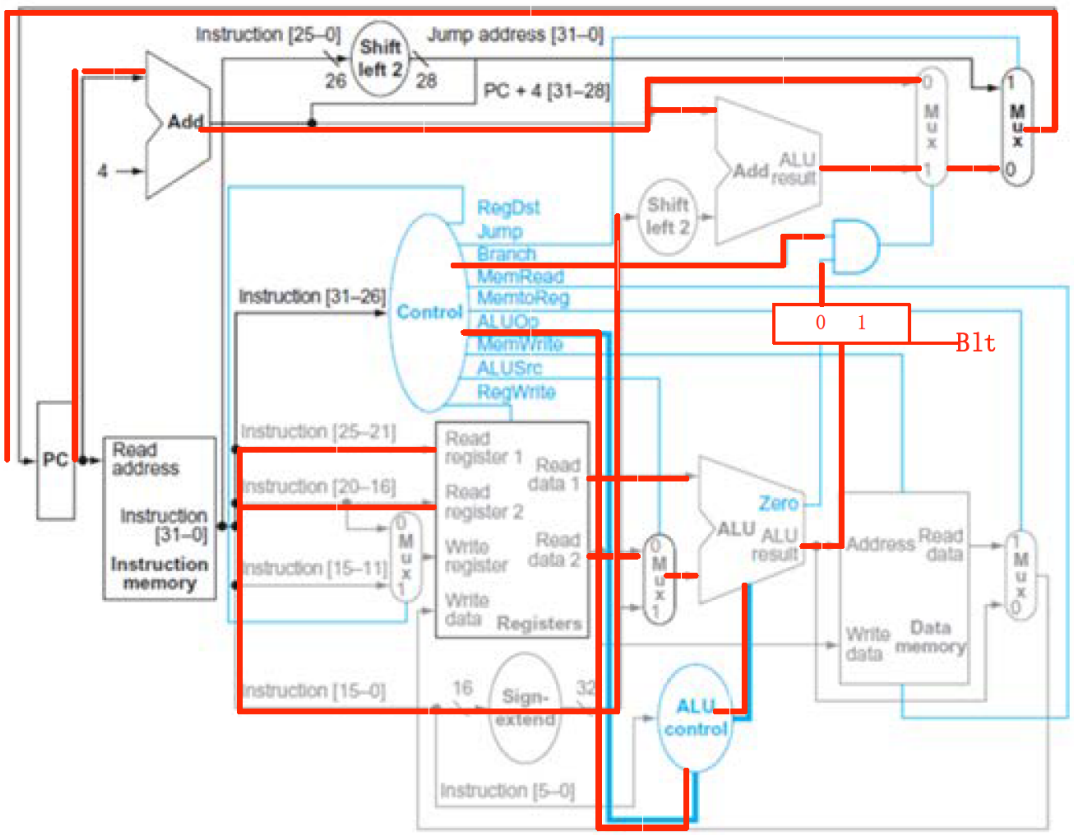
EE116C/CS151B Homework 4

Problem 1

Implement the MIPS instructions on the single cycle datapath. Specify all the control signals.

```
if (R[rs] < R[rt])
   PC = PC + 4 + SE(I)
else
   PC = PC + 4
```

Implement this instruction based on SLT function and I-type jump function.



Main Controller:

	R-format	Lw	Sw	Beq	Blt
Opcode	000000	100011	101011	000100	110000
RegDest	1	0	X	X	X
ALUSrc	0	1	1	0	0
MemtoReg	0	1	X	X	X
RegWrite	1	1	0	0	0
MemRead	0	1	0	0	0
MemWrite	0	0	1	0	0
Branch	0	0	0	1	1
ALUOp	10	00	00	01	11
Blt	0	0	0	0	1

ALU Controller:

Opcode	ALUOp	Operation	Funct	ALUfunction	ALU control
Lw	00	Load word	XXXXX	Add	0010
Sw	00	Store word	XXXXX	Add	0010
Beq	01	Branchequal	XXXXX	Subtract	0110
Rtype	10	Add	100000	Add	0010
	10	Subtract	100010	Subtract	0110
	10	And	100100	And	0000
	10	Or	100101	Or	0001
	10	setonlessthen	101010	setonlessthen	0111
Blt	11	setonlessthen	XXXXX	setonlessthen	0111

Problem 2

4.13 This is exercise is intended to help you understand the relationship between forwarding, hazard detection, and ISA design. Problems in this exercise refer to the following sequence of instructions, and assume that it is executed on a 5-stage pipelined data path:

```
add r5,r2,r1
lw r3,4(r5)
lw r2,0(r2)
or r3,r5,r3
sw r3,0(r5)
```

4.13.1 If there is no forwarding or hazard detection, insert nops to ensure correct execution.

add	IF	ID	EX	ME	WB									
nop		IF	ID	EX	ME	WB								
nop			IF	ID	EX	ME	WB							
lw				IF	ID	EX	ME	WB						
lw					IF	ID	EX	ME	WB					
nop						IF	ID	EX	ME	WB				
or							IF	ID	EX	ME	WB			
nop								IF	ID	EX	ME	WB		
nop									IF	ID	EX	ME	WB	
sw										IF	ID	EX	ME	WB