EE116C/CS151B Homework 7

Problem 1

For a direct-mapped cache design with a 32-bit address, the following bits of the address are used to access the cache.

Tag	Index	Offset
31-10	9-5	4-0

1 What is the cache block size (in words)?

2 How many entries does the cache have?

3 What is the ratio between total bits required for such a cache implementation over the data storage bits?

Address											
0	4	16	132	232	160	1024	30	140	3100	180	2180

4 Starting from power on, the following byte-addressed cache references are recorded as above table shows. How many blocks are replaced?

5 What is the hit ratio?

Problem 2

Media applications that play audio or video files are part of a class of workloads called "streaming" workloads; i.e., they bring in large amounts of data but do not reuse much of it. Consider a video streaming workload that accesses a 512 KB working set sequentially with the following address stream:
0, 2, 4, 6, 8, 10, 12, 14, 16 …

1 Assume a 64 KiB direct-mapped cache with a 32-byte block. What is the miss rate for the address stream above? How is this miss rate sensitive to the size of the cache or the working set? How would you categorize the misses this workload is experiencing, based on the 3C model?

2 Re-compute the miss rate when the cache block size is 16 bytes, 64 bytes, and 128 bytes. What kind of locality is this workload exploiting?