EE116C/CS151B Homework 2

Problem 1

Assume for a given processor the CPI of arithmetic instructions is 1, the CPI of load/store instructions is 10, and the CPI of branch instructions is 3. Assume a program has the following instruction breakdowns:

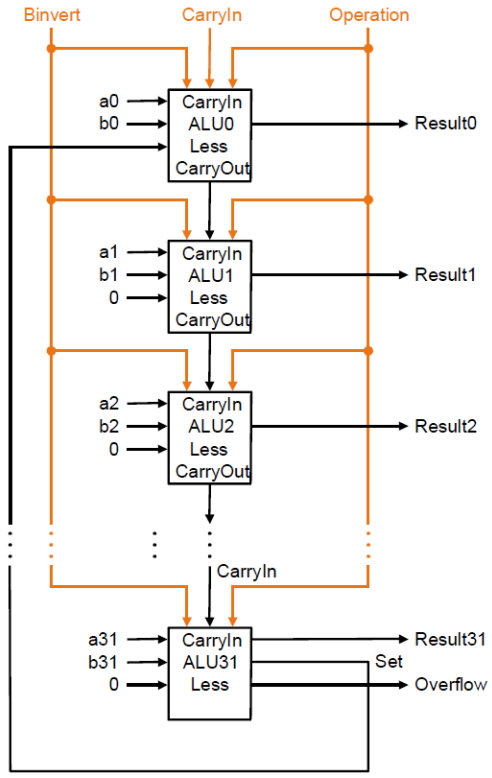
500 million arithmetic instructions, 300 million load/store instructions, 100 million branch instructions.

Suppose that new, more powerful arithmetic instructions are added to the instruction set. On average, through the use of these more powerful arithmetic instructions, we can reduce the number of arithmetic instructions needed to execute a program by 25%, and the cost of increasing the clock cycle time by only 10%. Is this a good design choice? Why?

Problem 2

The single cycle implementation of the MIPS processor uses for the mai n ALU the implementation shown in the figure below. Due to a circuit malfunction, the CarryIn signal to the least significant bit is always zero. The rest of the circuitry of the ALU and the rest of the processor operates normally.

Explain in full detail what will be the consequences of this fault when the processor executes programs — how will it change the behavior of the processor as observed by a user/ programmer who does not know a nd does not care how t he processor is implemented internally? Be sure to clearly identify each and every consequence of this fault.



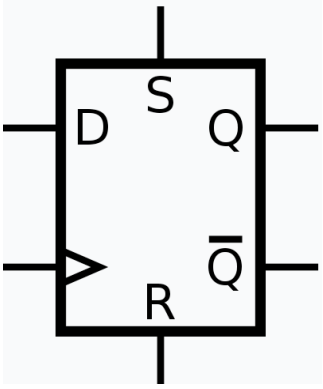
Problem 3

Draw a logic circuit of an adder of two 4 -bit numbers. Your design should be simple and modular.

problem 4

Using the circuit from problem 3 and D-flip-flops as a building blocks, show the design of a 4-bit counter that counts down.
The only external input to this circuit is the clock. The output four bits continuously follow the sequence: . . . , 11 , 10, 9, 8, 7, 6, 5, 4, 3, 2, 1, 0, 15, 14, 13, 12, 11, . . .
Your goal is to minimize the circuitry needed in addition to the module from problem 3.

D-flip-flop is as shown below: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