Design Specifications for TS1289 Diagnostic Board

This board has been designed to serve four purposes:

(1) Under ROM control, test basic functionality of host CPU.
(2) Under disk-based software control, verify basic functionality of an ST-5Ø6 hard disk controller/interface board.
(3) Under disk-based software control, verify basic functionality of an IDE (AT or XT) hard disk interface.
(4) Under ROM control, test basic functionality of floppy disk controller.

The board interfaces to the host CPU via a standard 62 pin XT-compatible card edge connector. There is one 34 pin card edge connector which is used for floppy and ST-5Ø6 hard drive controller testing, and one 4Ø pin header connector for IDE interface testing. Test points are provided for verification of system power supply voltages.

The board is addressed at five primary port locations, Ø8Øh (for LED power-on self-test (POST) displays) and 18Øh - 183h or 28Øh - 283h (for drive testing functions). The ports available for use as the drive testing ports and variable addressing for the diagnostic ROMS are jumper selectable.

Operation of the board in the system diagnostic mode is identical to the TS1288 board. The seven-segment LEDs will display the output at the system diagnostic port location Ø8Øh. Once the host machine has completed the POST testing and checks for the presence of additional ROMs, the diagnostic ROMs' code, if installed, will be executed, and the opening menu and tests available under ROM control will be displayed.

To access the drive testing portion of the board, the following port map should be used:

Port 18Øh/28Øh	bit 7:	Ø = select HD test circuitry, 1 = deselect HD
write:	bit 6:	Ø = select FD test circuitry, 1 = deselect FD
	bit 5:	Ø = HD READY*, FD RDY/DSKCHANGE*
	bit 4:	Ø = HD TRKØ*, FD TRKØ*
	bit 3:	Ø = HD FAULT*, FD WRTPRT*
	bit 2:	Ø = HD SC*
	bit 1:	Ø = read HD/FD input state
	bit Ø:	Ø = read HD/FD output state

Read HD input status (port 180h/280h):

```
bit 7:  not used
bit 6:  0 = DS*  (combination of all DS(1-4)* signals)
bit 5:  0 = DIR*
bit 4:  0 = STEP*
bit 3:  0 = HD3*
bit 2:  0 = HD2*
bit 1:  0 = HD1*
bit 0:  0 = HD0*
```

Read HD output status (port 180h/280h):

```
bit 7:  not used
bit 6:  not used
bit 5:  not used
bit 4:  not used
bit 3:  0 = READY*
bit 2:  0 = TRK0*
bit 1:  0 = FAULT*
bit 0:  0 = SC*
```

Read FD input status (port 180h/280h):

```
bit 7:  not used
bit 6:  not used
bit 5:  not used
bit 4:  not used
bit 3:  0 = SIDE*
bit 2:  0 = STEP*
bit 1:  0 = DIR*
bit 0:  0 = DS* (combination of DS(0-1)*)
```

Read FD output status (port 180h/280h):

```
bit 7:  not used
bit 6:  not used
bit 5:  not used
bit 4:  not used
bit 3:  not used
bit 2:  0 = RDY/DSKCHANGE*
bit 1:  0 = TRK0*
bit 0:  0 = WP*
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Port 181h/281h: R/W, IDE interface DØ-D7

bit 7: HDD7
bit 6: HDD6
bit 5: HDD5
bit 4: HDD4
bit 3: HDD3
bit 2: HDD2
bit 1: HDD1
bit Ø: HDDØ

Port 182h/282h: R/W, IDE interface D8-D15 (**AT IDE only!** Must be enabled for writes to IDE interface by setting bit 5 of control port 183h/283h to Ø.)

bit 7: HDD15
bit 6: HDD14
bit 5: HDD13
bit 4: HDD12
bit 3: HDD11
bit 2: HDD1Ø
bit 1: HDD9
bit Ø: HDD8

Port 183h/283h: Read, IDE control signals

AT IDE		XT IDE	
bit 7:	n/a	bit 7:	AEN
bit 6:	HDALE	bit 6:	n/a
bit 5:	n/a	bit 5:	DACK3*
bit 4:	HDCS1*	bit 4:	n/a
bit 3:	HDCSØ*	bit 3:	HDCSØ*
bit 2:	HDA2	bit 2:	n/a
bit 1:	HDA1	bit 1:	HDA1
bit Ø:	HDAØ	bit Ø:	HDAØ

Port 183h/283h: Write, IDE control signals (bits Ø-3) and port control (4-7)

Port Control:

Port Control Bit		Function
bit 7:	reserved	n/a
bit 6:	reserved	n/a
bit 5:	Ø	P182h on (AT IDE D8-D15 latch)
	1	P182h off (XT IDE)
bit 4:	Ø	Outgoing IDE control enable
	1	Outgoing IDE control disable

IDE Control Signals:

AT IDE		XT IDE	
bit 3:	n/a	bit 3:	DRQ3*
bit 2:	IOCS16*	bit 2:	n/a
bit 1:	HDRDY	bit 1:	n/a
bit Ø:	HDIRQ (IRQ14)	bit Ø:	HDIRQ (IRQ2 or IRQ5)

Sample Programming:

As an example of the operation of this portion of the board, let us say that the programmer wished to utilize the ST-506 hard drive section of the board, and assert READY*, TRK*, and SC*. He then wishes to check the status of the input lines from the hard drive controller, and of the output lines from the diagnostic board going back to the hard drive controller. The steps he would follow would be:

(1) Write port 180h (or 280h) with 01001001 binary. This says to select the hard drive circuitry, set READY*, TRK0*, and SC*, and on the next port 180h/280h read, read the input status from the hard drive controller.

(2) Send the command to the hard drive controller to perform whatever steps are needed to set the desired signals to the bubble.

(3) Do a port 180h/280h read for input status results.

(4) Write port 180h/280h with 01001010 binary. This says to keep the hard drive circuitry selected, leave READY*, TRK0*, and SC* active, and on the next port read, check the output status from the diagnostic board to the hard drive controller.

Do a port 180h read for output status results.

(5) Send the command to the controller to read bubble status and then compare those results to what was obtained in step (4).

Let us say the programmer wished to do a 16 bit write to the board for a read test of an AT IDE interface. The steps he would follow would be:

(1) Do a port 183h/283h write with at least bits 4 and 5 set to zero, and bit 2 set to zero. (For the example, we will write ØØØØØØ1Ø binary. This turns the high data port on, enables output control signals on an IDE port read, sets IOCS16* low to indicate to the system that a 16 bit data transfer is to take place, sets HDRDY so that no waits take place, and sets IRQ14 so that it is not asserted.)

(2) Write the desired eight bits of test data for HDDØ-HDD7 to port 181h/281h.

(3) Write the desired eight bits of test data for HDD8-HDD15 to port 182h/282h.

(4) Issue the apppropriate read command to the IDE interface.

(5) Write a ØØØ1Ø11Ø binary to port 183h/283h to turn the output control signals off, and turn IOCS16* off. Note that we have left the 182h/282h high data port enabled.

(6) Compare the data obtained by the IDE interface to that which was written to the test ports.

Theory of Operation:

(for Rev. PP1 schematic and wirewrap prototype, 3/6/90)

The board may roughly be divided into the following sections:

(1) System interface -- interfaces board to system bus.

(2) Main board decoding -- decodes port addressing for LED's or for drive interfaces; decodes memory addressing for onboard ROM's when installed.

(3) LED's and ROMS

(4) FD/ST-506 drive diagnostic section -- contains sufficient circuitry to allow verification of basic controller operation for ST-506 hard drives and floppy drives.

(5) IDE drive diagnostic section -- contains sufficient circuitry to allow verification of basic AT and XT IDE interface logic.

Each section will be discussed in turn.

System Interface

The system interface consists of J1, a 62 pin XT bus card edge connector, U22, U23, and U24, 74ALS244 buffers used to buffer address and control signals onto the board, U25, a 74ALS245 bidirectional transceiver for routing data to and from the board to the system bus, U17/A, a 74ALS08 two input AND gate, and U27/A, a 74LS21 four input AND gate, used for directional control of U25, and U15/E and U15/F, 74ALS04 inverting buffers used to buffer and invert the RESET DRV signal from the system bus.

The signals used by the board from the system bus (as they appear on J1) are as follows:

J1 pin 1:	n/c	pin 2:	GROUND
pin 3:	SD7	pin 4:	RESET DRV
pin 5:	SD6	pin 6:	+5V
pin 7:	SD5	pin 8:	n/c
pin 9:	SD4	pin 1Ø:	-5V
pin 11:	SD3	pin 12:	n/c
pin 13:	SD2	pin 14:	-12V
pin 15:	SD1	pin 16:	n/c
pin 17:	SDØ	pin 18:	+12V
pin 19:	n/c	pin 2Ø:	GROUND
pin 21:	AEN	pin 22:	n/c
pin 23:	SA19	pin 24:	SMEMR*
pin 25:	SA18	pin 26:	SIOW*
pin 27:	SA17	pin 28:	SIOR*
pin 29:	SA16	pin 3Ø:	n/c
pin 31:	SA15	pin 32:	n/c
pin 33:	SA14	pin 34:	n/c
pin 35:	SA13	pin 36:	n/c
pin 37:	SA12	pin 38:	n/c
pin 39:	SA11	pin 4Ø:	n/c
pin 41:	SA1Ø	pin 42:	n/c
pin 43:	SA9	pin 44:	n/c
pin 45:	SA8	pin 46:	n/c
pin 47:	SA7	pin 48:	n/c
pin 49:	SA6	pin 5Ø:	n/c
pin 51:	SA5	pin 52:	n/c
pin 53:	SA4	pin 54:	n/c
pin 55:	SA3	pin 56:	n/c
pin 57:	SA2	pin 58:	+5V
pin 59:	SA1	pin 6Ø:	n/c
pin 61:	SAØ	pin 62:	GROUND

The SA(Ø-19) lines are buffered by the permanently enabled buffers U22, U23, and U24 onto the board address bus BA(Ø-19). Similarly, the control lines AEN, SMEMR*, SIOR*, and SIOW* are buffered by one half of U24 to the board control lines AEN, MEMR*, IOR*, and IOW*. Data is routed to and from the board by the bidirectional transceiver at U25; this links the board data bus BD(Ø-7) to the system data bus SD(Ø-7). The last interface signal to be considered is RESET DRV; this is inverted once to become the board signal RESET* and inverted again to become RESET.

Main Decoding

The main decoding circuitry consists of the U17/B 74ALSØ8 AND gate, U15/A, U15/B, and U15/D 74ALSØ4 inverting buffers, U18/A 74LS26Ø five-input NOR gate, U7, U16, and U28 74LS138 3-to-8 decoders, U6/A, U6/B, and U6/C 74ALSØØ NAND gates, U29/A 74LS32 OR gate and jumpers E1-E15 and E16-E19.

Interaction with the board can take place in the following ways:

(1) Port Ø8Øh write -- for LED display
(2) Port 18Øh (or 28Øh) write -- for FD/ST-5Ø6 HD drive interface programming
(3) Port 18Øh (or 28Øh) read -- for reading FD/ST-5Ø6 HD drive interface status from controller or checking status of diagnostic board
(4) Port 181h (or 281h) read/write -- for reading/writing AT/XT IDE test data HDDØ-HDD7
(5) Port 182h (or 282h) read/write -- for reading/writing AT IDE test data HDD8-HDD15
(6) Port 183h (or 283h) read -- for reading AT/XT IDE control signals
(7) Port 183h (or 283h) write -- for writing AT/XT IDE control signals and for control of the IDE test interface
(8) Memory reads of ROM code if present. This may take place at a variety of addresses.

I/O port decoding is performed by U18/A, U17/B, U15/A, U15/B, U29/A, U16, and U28. The lines decoded by this circuitry are BAØ through BA9, AEN, IOW*, and IOR*.

The port at which the LED's may be accessed is fixed within the system architecture and the POST code in the BIOS ROMS at Ø8Øh. The PØ8ØW* signal is produced by U16 upon a successful decode of a port Ø8Øh I/O write and is used as an enable signal for the LED drivers at U14 and U26.

The drive interfaces may be accessed at either ports 18Øh - 183h or ports 28Øh - 283h. This selection is determined by the E16 through E19 jumpers.

For port 18xh access: E16-E17, E18-E19 (standard)
For port 28xh access: E16-E18, E17-E19

Upon successful decodes of either port 18Øh or port 28Øh reads or writes, U16 will produce the signal P18ØW* (for writes to the drive interface), or U28 will produce the signal P18ØR* (for reads of the drive interface). These signals are used for control functions within the FD/ST-5Ø6 drive interface circuitry.

Similarly, the control signals P181W*, P182W*, and P183W* are produced by U16 upon decodes of port 181h/281h, 182h/282h, and 183h/283h writes, and P181R*, P182R*, and P183R* upon decodes of these ports' reads.

The ROM decoding circuitry is comprised of U15/D, U7, U6/A, U6/B, and U6/C. The lines decoded are BA19 - BA15, AEN, and MEMR*. The jumper bank at E1 - E15 determines what addressing produces the enable signals for the ROMs, DROMEN* (Diag ROM ENable) and FDCROMEN* (FDC ROM ENable). Additionally, a composite signal is produced from these ROM enables and the MEMR* signal called ROMRD*; this signal and the P180R* - P183R* signals are used to control the direction of the main data transceiver U25.

ROM address jumpering is as follows:

For DIAG ROM access (U12):

E1-E2:	address C8000h	
E4-E5:	address D0000h	(standard)
E7-E8:	address D8000h	
E10-E11:	address E0000h	
E13-E14:	address E8000h	

For FDC ROM access (U13):

E2-E3:	address C8000h	(standard)
E5-E6:	address D0000h	
E8-E9:	address D8000h	
E11-E12:	address E0000h	
E14-E15:	address E8000h	

LEDs and ROMs

The LED circuitry is comprised of U14 and U26, MC14495 LED drivers, and DISP1 and DISP2, common cathode MAN74A 7 segment LEDs. The ROMs are located at U12 and U13, and are typically TMS27256 parts. Ordinarily, the DIAG ROM is installed at U12, and the FDC ROM at U13.

When enabled by the P080W* signal, the LED drivers U14 and U26 each read a nibble of the board data bus (U14 reading BD(0-3), U26 reading BD(4-7)) and produce the appropriate outputs to drive the LEDs at DISP1 and DISP2 to reflect the data read on the driver inputs. The MC14495 drivers have internal current limiting resistors, allowing them to be used without additional external current limiting resistors.

The ROMs are enabled by their respective enable signals, DROMEN* and FDCROMEN*, and gate data requested by the BA(0-14) lines onto the board data bus BD(0-7). This gating is performed by the MEMR* signal.

FD/ST-506 HD Drive Interface

The drive interface circuitry consists of U15/C, a 74ALS04 inverting buffer, U21, a 74LS374 octal latch, U5, a 74LS74 dual D latch, U9, a 74LS139 dual 2-to-4 decoder, U2, U3, U8, U10, U11, U19/A, and U20, 74ALS244 buffers, U4, a 74LS21 dual quad-input AND gate, U1, R1, R2, C1, C2, a 555 timer and associated support components, RP1, RP2, RP3, R3, and R4, which provide miscellaneous pullups, C28, preventing ringing on the P180W line, and the drive controller interface connector J2. Capacitors C31 and C32 are also present to prevent ringing on the RESET and RESET* lines respectively which may be induced by noisy option boards.

J2 is a dual purpose connector; depending on the mode in which the board is being used, it will emulate either a floppy drive or a hard drive control interface connector. Its pinout is as follows:

J2 pin 1:	n/c	pin 2:	HD HD3*
pin 3:	n/c	pin 4:	HD HD2*
pin 5:	n/c	pin 6:	n/c
pin 7:	n/c	pin 8:	HD SC*
pin 9:	n/c	pin 10:	HD TRK0*, FD DS0*
pin 11:	n/c	pin 12:	HD FAULT*, FD DS1*
pin 13:	GROUND	pin 14:	HD HD0*
pin 15:	GROUND	pin 16:	n/c
pin 17:	GROUND	pin 18:	HD HD1*, FD DIR*
pin 19:	GROUND	pin 20:	HD INDEX*, FD STEP*
pin 21:	GROUND	pin 22:	HD READY*
pin 23:	GROUND	pin 24:	HD STEP*
pin 25:	GROUND	pin 26:	HD DS1*, FD TRK0*
pin 27:	GROUND	pin 28:	HD DS2*, FD WP*
pin 29:	n/c	pin 30:	HD DS3*
pin 31:	n/c	pin 32:	HD DS4*, FD SIDE
pin 33:	n/c	pin 34:	HD DIR*, FD RDY*

Data written to the drive interface section of the board by either a port 180h or port 280h write will be latched by U21 (BD(0-5)) and U5 (BD(6-7)). BD6 and BD7 are latched separately since they provide enable signals for other portions of the drive circuitry; to guarantee intelligent behavior on power-on and front-panel reset, the SET* inputs of U5 are driven by the RESET* signal to force both the FSELECT* (sourced from BD6) and HSELECT* (sourced from BD7) signals high when the board is powered on or reset.

U21 provides the RDOUTPUT*, RDINPUT*, HSC* (HD Seek Complete), HFLTFWP* (HD FauLT, FD Write Protect), HFTRK0* (HD, FD TRacK 0), and HFREADY* (HD, FD READY). The HSC*, HFLTFWP*, HFTRK0*, and HFREADY* lines are provided to U20/A and U2 as hard drive outgoing status lines, and U20/B and U8/B as floppy drive outgoing status lines. U20/A and U20/B act as status registers for the outgoing lines and provide a way for the programmer to check the lines being sent to the controller against what the controller is receiving.

Controller input is handled by U3 and U4/A for hard drive controller input, and U8/A and U4/B for floppy drive controller input. U4 serves to produce a composite HDS* or FDS* signal made up from the individual drive select lines; this prevents the need for a "drive select" jumper on the board. Input to the board is enabled by the HSELECT* and FSELECT* lines; if these lines are not active, no data from the controller will be passed into the diagnostic board. Output from the diagnostic board is enabled by the composite drive select signals HDS* and FDS*.

Some additional decoding circuitry (U9) is used to determine whether incoming or outgoing, hard or floppy lines will be read on port 18Øh or 28Øh reads. The HSELECT* and FSELECT* signals are each used to enable one half of U9, which then decodes the RDOUTPUT* and RDINPUT* lines to produce HRDINPUT* and HRDOUTPUT* for reads of hard drive input and output information respectively, and FRDINPUT* and FRDOUTPUT* for reads of floppy drive input and output. U1Ø is used to buffer incoming hard drive lines, U19/A incoming floppy drive lines, U2Ø/A outgoing hard drive lines, and U2Ø/B outgoing floppy drive lines, back to the port 18Øh read register, U11.

1k pullups (RP1, RP2) are provided on all incoming drive lines. Since some lines are dual-purpose, this may imply termination on some outgoing lines as well. The 1k value was chosen since it is a fairly "light" termination value, and should not pose a major problem for a controller to overcome.

4.7k pullups are provided on critical enable signals for the various data transceivers to prevent "accidental" enabling. C28 is used to prevent ringing on the P18ØW line from inadvertently latching bad data into the port 18Øh write latches U21 and U5. Likewise, C31 and C32 are used to prevent ringing on the RESET and RESET* lines into U21 and U5 respectively, which may cause board malfunction when noisy option boards are present in the system.

The remaining circuitry on the board, U1, R1, R2, C1, and C2, make up a 555 timer circuit which provides a simulated index pulse to hard drive controllers. R2 is a Ø to 2Øk multiturn pot to align the circuit to provide a 16.67 msec period; this may be monitored during alignment at test point TP6.

IDE Drive Interface

The IDE drive interface consists of J3, a 40 pin header connector, U29/B, U29/C, and U29/D, 74LS32 OR gates, U6/D, a 74ALS00 NAND gate, U17/C, a 74ALS08 AND gate, U18/B, a 74LS260 five input NOR gate, U37/A and U37/B, 74ALS04 inverting buffers, U31 and U33 - U36, 74LS374 octal D latches, U32, a 74LS173 quad D latch, U30, a 74LS74 dual D latch, and RP4, RP5, R5, R6, C33, C34, C46 - C49, and C50, which provide miscellaneous pullups/pulldowns and ringing protection.

J3 is used to connect to both XT and AT type IDE interfaces. The pinout of this connector is as follows:

J3 pin 1:		HDRESET*	pin 2:		GROUND
pin 3:		HDD7	pin 4:	(A)	HDD8
pin 5:		HDD6	pin 6:	(A)	HDD9
pin 7:		HDD5	pin 8:	(A)	HDD10
pin 9:		HDD4	pin 10:	(A)	HDD11
pin 11:		HDD3	pin 12:	(A)	HDD12
pin 13:		HDD2	pin 14:	(A)	HDD13
pin 15:		HDD1	pin 16:	(A)	HDD14
pin 17:		HDD0	pin 18:	(A)	HDD15
pin 19:		GROUND	pin 20:		KEY
pin 21:	(X)	HDAEN	pin 22:		GROUND
pin 23:		HDIOW*	pin 24:		GROUND
pin 25:		HDIOR*	pin 26:		GROUND
pin 27:	(A/X)	HDRDY/DACK*	pin 28:	(A)	HDALE
pin 29:	(X)	DRQ3*	pin 30:		GROUND
pin 31:		HDIRQ	pin 32:	(A)	IOCS16*
pin 33:		HDA1	pin 34:		n/c
pin 35:		HDA0	pin 36:	(A)	HDA2
pin 37:		HDCS0*	pin 38:	(A)	HDCS1*
pin 39:		n/c	pin 40:		GROUND

The pins which are marked with (X) or (A) are used exclusively by either XT or AT IDE interfaces respectively. The pin which is marked (A/X) is used by both the AT and XT IDE interfaces, but for two different functions; pin 27 is input as HDRDY by the AT interface, and is used as the DACK3* output by the XT interface.

Three port addresses are used by the IDE interface. The low byte of IDE data may be written or read at port 181h (or 281h). This port may always be utilized to read and write data to or from both the XT and AT style IDE interface; no control bits must be set to access this port.

Data written to port 181h (281h) will be latched into U35 (BD(Ø-7)) by the signal P181W, which is derived by using U6/D to invert P181W*. The output enable for U35 is a derived signal called WRCLK* which is produced from the OR of IDESEL* and the HDIOR* signal. This signal WRCLK* will only be active during a read of the actual IDE interface in the computer. It is important to note that the IDE interface is very similar to a system bus, so it is important to guarantee that data only be output when the IDE port is actually being accessed. IDESEL* is produced by the AND of the IDE chip select lines, HDCSØ* and HDCS1*. IDESEL* will be active any time either or both of the HDCS(Ø-1)* lines are active. 4.7k pullups are present on the IDE chip selects so that IDESEL* will not float active unintentionally.

The low byte of data from the IDE interface will be latched into the board at U33 by the derived signal RDCLK. Since we must also be certain that only data destined for the IDE device is latched by U33, we take the NOR (U18/B) of IDESEL* and HDIOW* to produce this active high signal. The latch may then be read by performing a port 181h (281h) read, which activates the output enable signal for U33, P181R*.

The high byte of data is handled in a similar fashion at port 182h (282h). The major difference occurs on port writes. The even IDE interface pins 4 through 18 (HDD(8-15)) are tied to ground on the XT IDE interface. So that voltages are not passed to the ground plane indiscriminately, a bit in the control port (183h or 283h, bit 5) is defined such that this bit must be set low to enable the port for output. This bit is latched by U3Ø/B, and the resultant signal, HIDATA*, is OR'ed (U29/C) with the previously derived WRCLK* signal to enable the high data output latch, U36. Thus, even if data is written for output to the IDE interface at port 182h (282h), the IDE interface will not be able to read HDD(8-15) unless port 183h (283h), bit 5 is set low. **For AT use, port 183h, bit 5 should be <u>low</u>. For XT use, port 183h, bit 5 should be <u>high</u>.** Data written to port 182h (282h) will be latched into U36 by the P182W signal, produced by using U37/A to invert P182W*.

The high byte of data from the IDE interface will be latched into the board at U34 by the derived signal RDCLK. **(Note that on the XT interface, this byte will always be a ØØh, since these lines are tied to ground).** The latch may then be read by performing a port 182h (282h) read, which activates the latch outputs with the signal P182R*.

The IDE control signals are monitored by reading port 183h (283h). The control signals are latched onto the board at U31 by the RDCLK signal; the latch outputs are then enabled by performing a port 183h (283h) read, which activates the signal P183R*. Note that the definitions of this port are different for the XT and AT IDE interfaces!

Outgoing IDE signals are latched by U32, a 74LS173. This chip has a master reset input, tied to the board RESET line, which clears all latched values. There are two separate sets of enable lines; the clock enable inputs E1* and E2* are tied low so as to permanently enable the clock. Data (BD(Ø-3)) is clocked into the chip using the P183W signal, produced by inverting P183W* with U37/B. Output is enabled by writing a Ø to bit 4 of port 183h (283h); to disable output of the control signals, a 1 should be written to this location. In order to guarantee proper timing on the IOCS16* signal, the board version of this signal, BDIOCS16*, is OR'ed with the IDESEL* signal, producing an active IOCS16* out to the IDE interface only when both input signals are active. This guarantees that the IOCS16* line from this board will only be active during a read of the IDE device.

Pullups are provided on all output enable lines. Additionally, outgoing IDE control lines are pulled up or down as appropriate to guarantee their inactive conditions when not actually asserted. The port control latch U3Ø is reset (cleared) by the board RESET* signal; decoupling capacitors are used on the master reset input of U32 and on the U3Ø SET inputs to prevent triggering via noise. Decoupling capacitors are also used on all clock inputs to prevent latching improper data. A key is provided on the IDE connector to better allow correct cable orientation.

Power test points are provided on the board to allow checking of the +5V, -5V, +12V, -12V, and ground in the CPU in which the board is installed. The mapping of these test points is as follows:

Ground:	TP1
+5V:	TP2
-5V:	TP3
+12V:	TP4
-12V:	TP5

C3 - C27, C3Ø, and C35 - C45 are Ø.1µf bypass capacitors; C29 is a 1Øµf electrolytic capacitor. All of these are used to provide "quieting" of AC noise on the +5V power bus.

Parts List

Component Number	Type	Quantity
U22, U23, U24, U11, U10, U19, U20, U2, U3, U8	74ALS244 (or 'LS244)	10
U25	74ALS245	1
U17	74ALS08	1
U15, U37	74ALS04	2
U18	74LS260	1
U6	74ALS00	1
U7, U16, U28	74LS138	3
U12, U13	TMS27256	2
U14, U26	MC14495	2
DISP1, DISP2	7 segment LED, common cathode, MAN74A	2
U21, U31, U33 - U36	74LS374	6
U9	74LS139	1
U4, U27	74LS21	2
U1	555	1
U5, U30	74LS74	2
U29	74LS32	1
U32	74LS173	1
RP3, RP4, RP5	8 pin 4.7k SIP	3
RP1, RP2	8 pin 1k SIP	2
R1	2.2k, 5%, 1/4 watt	1
R2	0 to 20k multiturn pot	1
R3, R4, R6	4.7k, 5%, 1/4 watt	3
R5	1k, 5%, 1/4 watt	1
C1	1µf electrolytic	1
C2 - C27, C30, C35 - C45	0.1µf bypass cap	38
C28, C46 - C49	220pf ceramic cap	5
C29	10µf electrolytic	1
C31, C32, C33, C34, C50-C52	0.001µf ceramic cap	4
E1-E19, TP6	staking pins	20
ROM sockets	28 pin	2
LED sockets	14 pin	2
Power test point connectors (one each of five colors, TP(1-5))		5
Jumpers (2 for board addressing, 2 for ROM addressing)		4

Header strips may be used instead of discrete staking pins where appropriate in jumper groupings.