TANDY®

Technician Series
Diagnostics Software

EM

Extended Memory Diagnostic

01-0220 Computer Technical Services

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EM

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EM

TABLE OF CONTENTS

GENERAL DESCRIPTION

The Extended Memory (EM) diagnostic allows the testing of memory above the 1 Megabyte address space.

FEATURES

Capable of testing 15 Megabytes of Extended Memory.

Selectable test range allows user to concentrate testing on a particular memory section.

Multiple test patterns selectable from pop-up windows.

Supports single pass or continuous testing modes.

Variable verify delay allows checking for proper memory refreshing.

Graphic display of test range as well as passed and failed memory blocks.

EQUIPMENT REQUIRED

MS-DOS computer system with memory above 1 Megabyte.

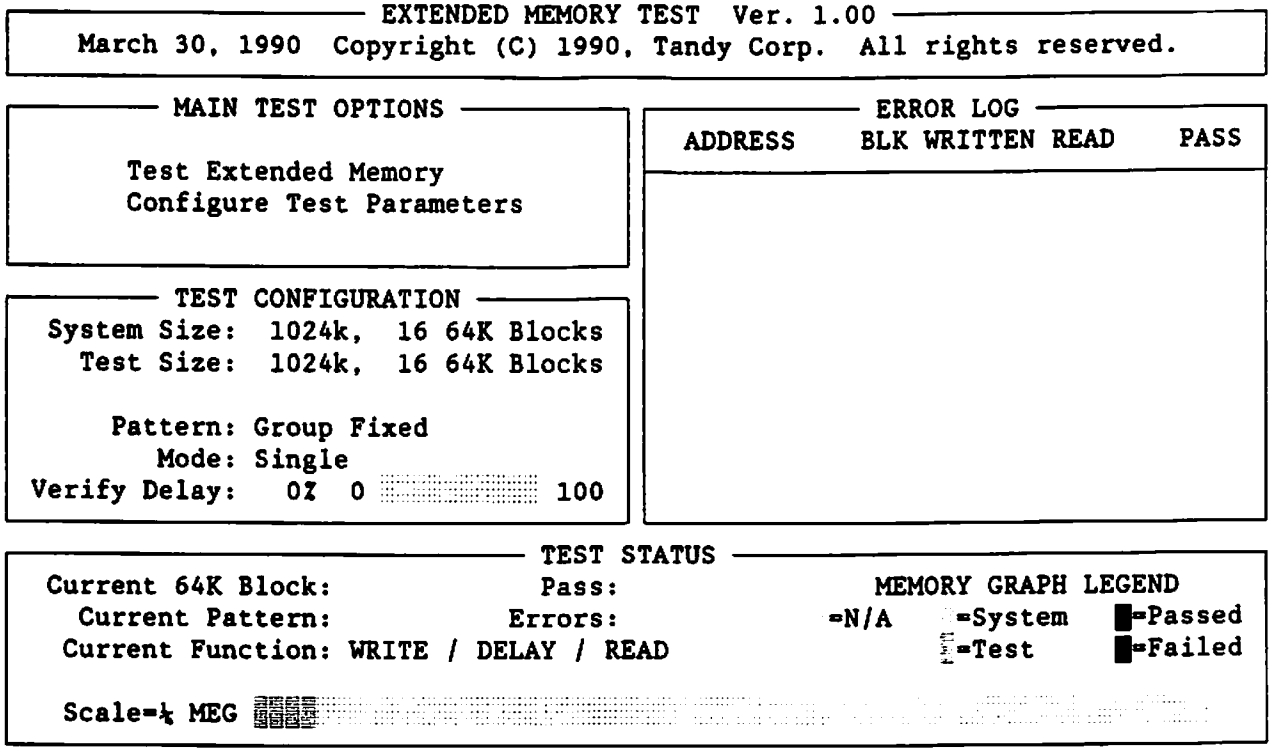
LOADING EM

The EM program can be loaded either by selecting the appropriate menu selection on a Diagnostic Diskette or at the DOS prompt by typing:

em<ENTER>

DISPLAY DESCRIPTION

Once loaded, the main screen is displayed:



NOTE: Memory values displayed may vary depending on amount of memory installed in the test machine.

The Main screen can be divided into five (5) sections:

Main Test Options **Error Log** **Test Configuration**
Test Status **Option Prompt Bar**

Main Test Options: Displays the primary options of the test. Refer to the Command Section of this manual for further details on the available options.

Error Log: Displays any errors that may occur in the following format:

ADDRESS: Displays the memory address of the error in Segment:Offset format.

BLOCK: Displays the 64K block number in which the error occurred.

WRITTEN: Displays the pattern written.

READ: Displays the pattern read back.

PASS: Displays the pass number in which the error occurred.

NOTE: If the error was something other than a data miscompare one of the following messages may appear in place of the Written & Read values:

ADDRESS LINE (Major Address line failed)
ADR LN xxxxh (Address Line at chip failed)
PARITY ERROR (Memory Parity error occurred)
EXCEPT. INT. (Exception Interrupt occurred)
GATE LINE 20 (Address Gate Line 20 Failed)

See the Memory Error Decoding section of this manual for more information on errors.

Test Configuration: Displays the current test parameters:

System Size: Displays the amount of system memory, as seen by BIOS during boot-up, in both kilobytes and the number of 64K blocks.

Test Size: Displays the amount of memory currently defined as the test range in both kilobytes and the number of 64K blocks. Default size is the same as the System size.

Pattern: Displays the currently selected test pattern. Default test pattern is Fixed & Rotating.

Mode: Displays the currently selected test mode. Default mode is Single Pass.

Verify Delay: Displays the amount of delay between write and read as a percentage of total delay available in both decimal form and as a graph. Default Verify Delay is 0%, or no delay implemented.

Test Status: Displays the progress of the current memory test. When the test is completed it displays the final results both as error counts and graphically.

Current 64K Block: Displays the current block being tested.

Current Pattern: Displays the current pattern being written to the block under test.

Current Function: Displays the current test operation.

Pass: Displays the current pass number.

Errors: Displays the current error count.

Graph: Displays the test progress graphically

NOTE: If an error occurs the address, block number, pattern written, pattern read and pass count are displayed under the Error Log and the Error count is incremented by one. The testing of the current block is then aborted and testing proceeds onto the next block. Therefore the Error count does not represent all of the bad memory locations but instead it represents how many 64K blocks had an error occur.

Each graph location represents 256K or 4-64K blocks. Therefore if one, or more, of the 4 blocks within that 256K of memory had an error the graph will indicate that 256K as failed.

Option Prompt Bar: Displays additional information on the current input requested from the user.

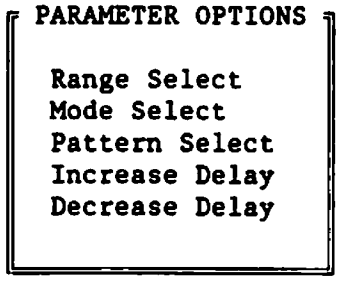
COMMANDS

The Main Option menu contains just two selections, Test Extended Memory and Configure Test Parameters.

Test Extended Memory: Selecting this option starts the testing of the Extended Memory within the currently selected Test Range using the selected Pattern(s) and Verify Delay parameters.

NOTE: Testing may be aborted at any time by pressing the <ESC> key.

Configure Test Parameters: This option permits the selection of the parameters used during testing. Once selected the Parameter Option menu window will be displayed:



Range Select: This option provides the selection of the Test Range. This is accomplished by using the memory graph in the Test Status section to select the beginning and ending block of memory. The smallest amount of memory selectable is 256K or 4 - 64K blocks.

Once this option is selected, the memory graph is redisplayed showing only the System Memory locations. A blinking arrow is then positioned over the first block. You are then requested to mark the beginning of the test range by using the left and right arrow keys to position the blinking arrow over the desired starting point and then pressing <ENTER>. With the beginning 256K block of memory selected the Test Configuration section of the main screen will show the Test Size in kilobytes as well as the number of 64K blocks. By using the left and right arrow keys again, you position the blinking arrow over the ending 256K block and press <ENTER>. Once the ending 256K block of memory has been defined the memory graph is redisplayed with the new Test Range values.

NOTES: The Test Range selection may be aborted at any time before the ending 256K block has been defined by pressing <ESC>. This will return the original Test Range values.

If at any time the Test Range Selection goes beyond the System memory location a message will appear within the Test Configuration area of the screen as follows:

TEST RANGE BEYOND SYSTEM MEMORY

This informs you that memory has been selected to be tested which is beyond the address area in which the computer system believes the installed memory resides.

Mode Select: This option provides the selection of Single Pass or Continuous mode.

Single: The memory is tested within the selected test range with the current pattern(s) once and then control is returned to the Main Options menu.

Continuous: The memory is tested within the selected test range with the current pattern(s) after which the Pass number is incremented and testing is restarted at the beginning of the test range. This cycle will repeat until the <ESC> key is pressed to abort the testing and return control to the Main Options menu.

Pattern Select: This option provides the selection of the test Pattern or group of patterns. When selected the Pattern Selection menu appears with the following patterns available:

Single Fixed: This option causes the memory within the test range to be tested with the same single word pattern. The single word pattern is selected from the pop-up window and may be either 0000h, 5555h, AAAAh or FFFFh. With this pattern selected each 64K block within the test range is tested once.

Group Fixed: This options causes the memory within the test range to be tested with each of the available Single Fixed patterns (0000h, 5555h, AAAAh and FFFFh). With this pattern selected each 64K block within the test range is tested four times, once with each fixed pattern, before the test proceeds to the next 64K block.

Rotating Bit: This option causes the memory within the test range to be tested multiple times by rotating a single bit through each bit location of the word. The starting test pattern is 0001h with each successive pattern having the bit rotated one position to the left. With this pattern selected each 64K block within the test range is tested sixteen times, once for each bit location of the word, before the test proceeds to the next 64K block.

Fixed & Rotating: This option causes the memory within the test range to be tested first with the patterns used in the Fixed Group test and then with the patterns of the Rotating Bit group. With this pattern selected each 64K block is tested twenty times, four for the Group Fixed and sixteen for the Rotating Bit, before the test proceeds to the next 64K block.

Quick Modified Address: A Modified Address test fills each byte within the 64K block with the XOR of the address and the current test pattern. In this way every byte within the 64K block contains a different value. The XOR test pattern is then decremented by one and the process is repeated. With this pattern selected the starting pattern for the XOR is 00FFh which means each 64K block is tested 256 times before the test proceeds to the next 64K block.

Long Modified Address: This option performs the same modified address test as the Quick Modified Address except the starting pattern for the XOR is FFFFh which means each 64K block is tested 65,536 times before the test proceeds to the next 64K block.

Increase Delay: Selecting this option will increase the Verify Delay by 10% of its full delay time until the maximum delay is reached at which time this option will no longer have an effect.

Decrease Delay: Selecting this option will decrease the Verify Delay by 10% of its full delay time until the delay value reaches zero at which time this option will no longer have an effect.

NOTE: The delay option provides a simple method of checking memory refresh. Normally a pattern is written into memory and then very quickly read back. Even if the refresh circuitry is not working properly this quick write/read may function correctly. By inserting a delay between the write/read we can insure a refresh must take place before the memory is read back.

Address Line Testing:

At the completion of testing a block with the selected test patterns, before proceeding onto the next block, a special test is performed. This test combines a rotating bit and modified address pattern designed to detect address line problems. It writes these special patterns to the current memory block and then checks all 64K blocks within the test range for these patterns. If the machine is functioning correctly the only block containing the patterns should be the one written to. If the test pattern is detected in a 64K block other than the current block, an ADDRESS LINE error message is displayed within the Error Log. If the test pattern read back within the current block is different than the written pattern, an ADR LN xxxxh error message is displayed.

APPENDIX

MEMORY ERROR DECODING

Following are examples of the possible memory error messages displayed by EM and how they are decoded:

ERROR LOG

	ADDRESS	BLK	WRITTEN	READ	PASS
Error Number 1 --->	20000:0000	17	FFFFh	FFFEh	1
Error Number 2 --->	21000:0000	18	ADR LN	FDFCh	1
Error Number 3 --->	20000:0000	19	ADDRESS LINE		1
Error Number 4 --->	23000:0000	20	PARITY ERROR		1
Error Number 5 --->	24000:0000	21	GATE LINE 20		1
Error Number 6 --->	25000:0000	22	EXCEPT. INT.		1

ERROR NUMBER 1:
A data error has occurred at address 20000:0000, which is the 17th 64K block of memory, during pass 1 of the test. The binary difference between FFFFh and FFFEh indicates bit 0 is being held low.

ERROR NUMBER 2:
An address line error has occurred at address 21000:0000, which is the 18th 64K block of memory, during pass 1 of the test. The binary difference between FDh (value written) and FCh (value read) indicates the RAM chip responsible for bit 0 has an addressing problem.

ERROR NUMBER 3:
When checking for possible address line problems the test pattern was detected in the 64K block of memory at address 20000:0000 (block 17) while testing memory block 19. This indicates a major address line problem which caused the test data to be written and read correctly but at the wrong memory address. This error occurred during pass 1 of the test.

ERROR NUMBER 4:
A parity error occurred at address 23000:0000, which is the 20th 64K block of memory, during pass 1 of the test.

NOTE:
EM is not capable of detecting Parity errors on computers that do not have an on-board port 80h, such as the 3000HL and 3000NL. With these computers the following message will appear within the error log section:

Warning: EM Can Not Detect A Parity
Error On This Computer!

ERROR NUMBER 5:
The enabling, or disabling, of Address Line 20 when entering, or exiting, protected mode failed while testing address 24000:0000, which is in the 21st 64K block of memory, during pass 1 of the test.

ERROR NUMBER 6:
While in protected mode testing address 25000:0000, which is in the 22nd 64K block of memory, an exception interrupt error (instruction could not be completed normally) occurred.

ERROR MESSAGES

EM ERROR: Insufficient Memory To Allocate 64K Transfer Buffer!
EM must have a 64K block of Standard memory (below 640K) in order to transfer information to the Extended memory (above 1 MEG). This error indicates it was unable to acquire the 64K of Standard memory required.

Remove any TSR (Terminate but Stay Resident) programs which may be holding this memory or install more Standard memory.

EM ERROR: This Machine Does Not Support Extended Memory!
This error indicates the machine does not support the use of Extended memory in which case the EM test is not required.

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