IP6502 - MOS Technology 6502 compliant IP core

Overview

The IP6502 RTL HDL IP core implements the MOS Technology 6502 feature and instruction set. This fast 8-bit databus wide microprocessor is capable of running most of its instruction in two clock cycle, with the most powerful direct and indirect zero-page addressing that are two bytes long. The external 64KB memory access is done via 16-bit wide address bus and 13 addressing modes for most of the instructions. External event interfacing is accomplished by separate non-maskable and maskable interrupt lines. Additional DMA modules can hold down the IP6502 core by the RDY line to allow memory access. Arithmetic is capable of signed, unsigned and BCD numbers manipulation. In order to communicate with external math unit the SO (Set Overflow) allows overflow flag setting.

Signals

Name	Width	Type	Description
clk	1	Input	Clock source for internal registers
res	1	Input	Reset for internal regsiters
rdy	1	Input	Ready line for holding CPU execution
irq	1	Input	Maskable interrupt request line
nmi	1	Input	Non-maskable interrupt request line
so	1	Input	Set overflow input from external math unit
addr	16	Output	Address bus
dataout	8	Output	Data bus output
datain	8	Input	Data bus input
rw	1	Output	Read/Write indication signal
sync	1	Output	Instruction fetch indication output signal

Features

- 56 instructions
- 151 instruction opcodes
- 13 addressing modes
- up to 64KB external memory
- 16-bit wide address bus
- 8-bit wide databus
- 3 general purpose registers
  - A - accumulator for most of the arithmetics
  - X,Y - index registers for memory index based access
- NMI non-maskable and IRQ maskable interrupt inputs
- RDY line for DMA interfacing

Applications

- Ultra-low power consumption and silicon area designs
- High-speed computation and control systems

Benefits

- Well known architecture
- Free C compiler
- Compatible with Motorola 6800

Deliverables

- Fully synthesizable VHDL/Verilog RTL core or reference technology netlist
- Complete testbench and reference chip waveforms to compare
- Full product documentation covering functionality and integration guideline
- Software development support
- IP core customization including new opcode specification
- Reference design

Diagram