# MX23C6410

## 64M-BIT Mask ROM (8/16 Bit Output)
## For SOP and TSOP Packages

### FEATURES

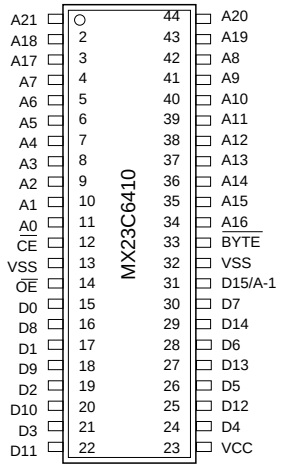
- Bit organization
  - 8M x 8 (byte mode)
  - 4M x 16 (word mode)
- Fast access time
  - Random access: 100ns (max.)
- Current
  - Operating: 70mA
  - Standby: 100uA (max.)
- Supply voltage
  - 5V±10%
- Package
  - 44 pin SOP (500 mil)
  - 48 pin TSOP (12mm x 20mm)

### ORDER INFORMATION

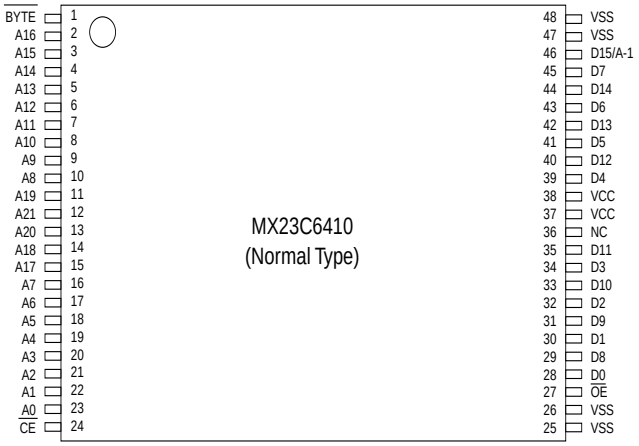
| Part No. | Access Time | Package |
|---|---|---|
| MX23C6410MC-10 | 100ns | 44 pin SOP |
| MX23C6410MC-12 | 120ns | 44 pin SOP |
| MX23C6410MC-15 | 150ns | 44 pin SOP |
| MX23C6410TC-10 | 100ns | 48 pin TSOP |
| MX23C6410TC-12 | 120ns | 48 pin TSOP |
| MX23C6410TC-15 | 150ns | 48 pin TSOP |
| MX23C6410RC-10 | 100ns | 48 pin TSOP (Reverse type) |
| MX23C6410RC-12 | 120ns | 48 pin TSOP (Reverse type) |
| MX23C6410RC-15 | 150ns | 48 pin TSOP (Reverse type) |

### PIN CONFIGURATION

#### 44 SOP




#### 48 TSOP (NORMAL TYPE)




#### 48 TSOP (REVERSE TYPE)

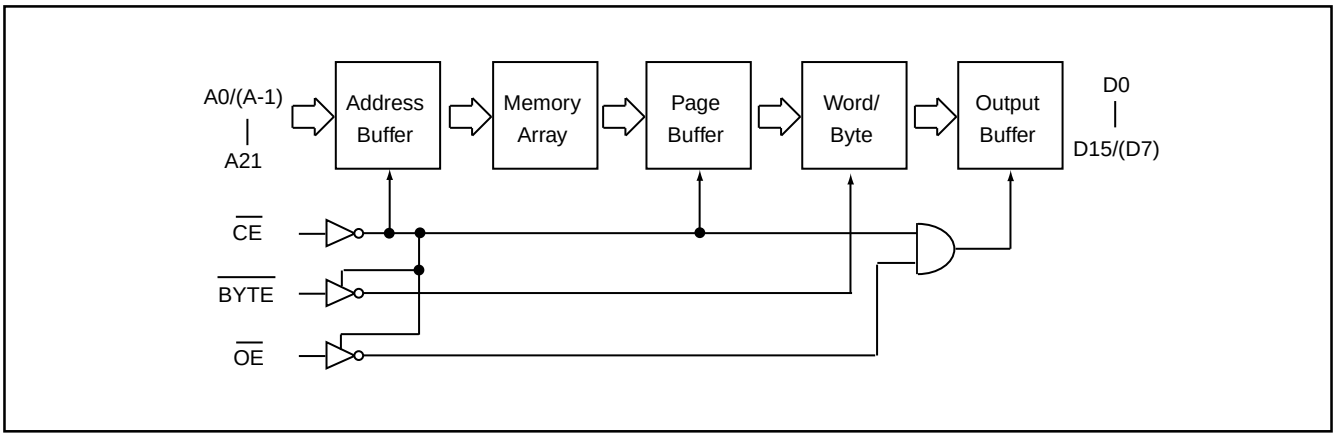
## PIN DESCRIPTION

| Symbol | Pin Function |
|---|---|
| A0~A21 | Address Inputs |
| D0~D14 | Data Outputs |
| D15/A-1 | D15 (Word Mode) / LSB Address (Byte Mode) |
| $\overline{CE}$ | Chip Enable Input |
| $\overline{OE}$ | Output Enable Input |
| $\overline{Byte}$ | Word / Byte Mode Selection |
| VCC | Power Supply Pin |
| VSS | Ground Pin |
| NC | No Connection |

## MODE SELECTION

| $\overline{CE}$ | $\overline{OE}$ | $\overline{Byte}$ | D15/A-1 | D0~D7 | D8~D15 | Mode | Power |
|---|---|---|---|---|---|---|---|
| H | X | X | X | High Z | High Z | - | Stand-by |
| L | H | X | X | High Z | High Z | - | Active |
| L | L | H | Output | D0~D7 | D8~D15 | Word | Active |
| L | L | L | Input | D0~D7 | High Z | Byte | Active |

## BLOCK DIAGRAM



## ABSOLUTE MAXIMUM RATINGS

| Item | Symbol | Ratings |
|---|---|---|
| Voltage on any Pin Relative to VSS | VIN | -0.8V to VCC+2.0V (Note) |
| Ambient Operating Temperature | Topr | 0℃ to 70℃ |
| Storage Temperature | Tstg | -65℃ to 125℃ |

Note: Minimum DC voltage on input or I/O pins is -0.5V. During voltage transitions, inputs may undershoot VSS to -0.8V for periods of up to 20ns. Maximum DC voltage on input or I/O pins is VCC+0.5V. During voltage transitions, input may overshoot VCC to VCC+2.0V for periods of up to 20ns.

## DC CHARACTERISTICS (Ta = 0℃ ~ 70℃, VCC = 5V±10%)

| Item | Symbol | MIN. | MAX. | Conditions |
|---|---|---|---|---|
| Output High Voltage | VOH | 2.4V | - | IOH = -1.0mA |
| Output Low Voltage | VOL | - | 0.4V | IOL = 2.1mA |
| Input High Voltage | VIH | 2.2V | VCC+0.3V | |
| Input Low Voltage | VIL | -0.3V | 0.8V | |
| Input Leakage Current | ILI | - | 5uA | 0V, VCC |
| Output Leakage Current | ILO | - | 5uA | 0V, VCC |
| Operating Current | ICC1 | - | 70mA | f=5MHz, all output open |
| Standby Current (TTL) | ISTB1 | - | 1mA | $\overline{CE}$ = VIH |
| Standby Current (cmos) | ISTB2 | - | 100uA | $\overline{CE}$>VCC-0.2V |
| Input Capacitance | CIN | - | 10pF | Ta = 25℃, f = 1MHZ |
| Output Capacitance | COUT | - | 10pF | Ta = 25℃, f = 1MHZ |

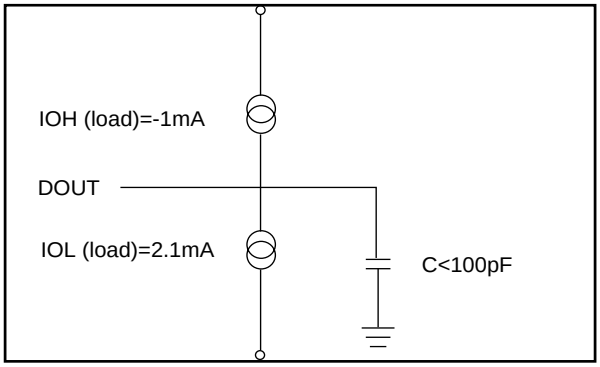
## AC CHARACTERISTICS (Ta = 0℃ ~ 70℃, VCC = 5V±10%)

| Item | Symbol | 23C6410-10 | | 23C6410-12 | | 23C6410-15 | |
|---|---|---|---|---|---|---|---|
| | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. |
| Read Cycle Time | tRC | 100ns | - | 120ns | - | 150ns | - |
| Address Access Time | tAA | - | 100ns | - | 120ns | - | 150ns |
| Chip Enable Access Time | tACE | - | 100ns | - | 120ns | - | 150ns |
| Output Enable Time | tOE | - | 50ns | - | 60ns | - | 70ns |
| Output Hold After Address | tOH | 0ns | - | 0ns | - | 0ns | - |
| Output High Z Delay | tHZ | - | 20ns | - | 20ns | - | 20ns |

Note:Output high-impedance delay (tHZ) is measured from $\overline{OE}$ or $\overline{CE}$ going high, and this parameter guaranteed by design over the full voltage and temperature operating range - not tested.

## AC Test Conditions

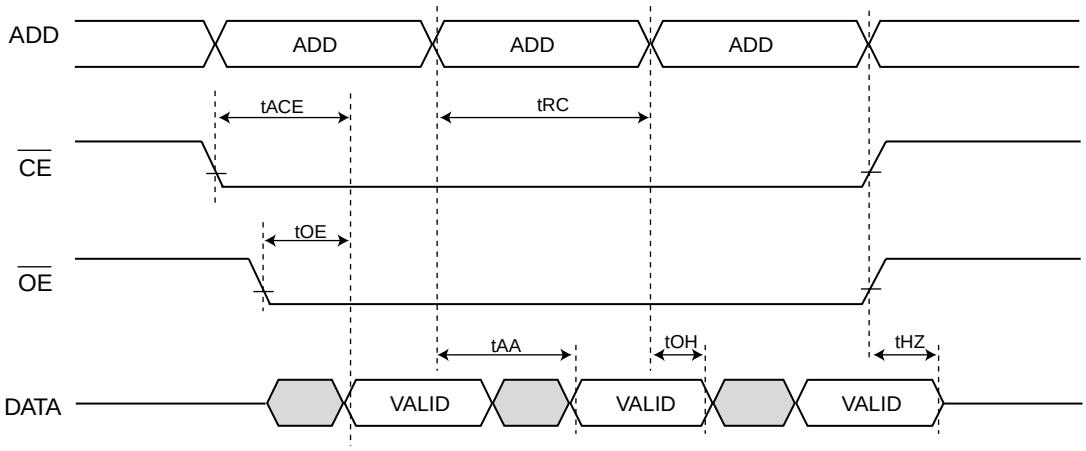
| | |
|---|---|
| Input Pulse Levels | 0.4V~ 2.4V |
| Input Rise and Fall Times | 10ns |
| Input Timing Level | 1.4V |
| Output Timing Level | 0.8V and 2.0V |
| Output Load | See Figure |




Note:No output loading is present in tester load board.
Active loading is used and under software programming control.
Output loading capacitance includes load board's and all stray capacitance.

## TIMING DIAGRAM

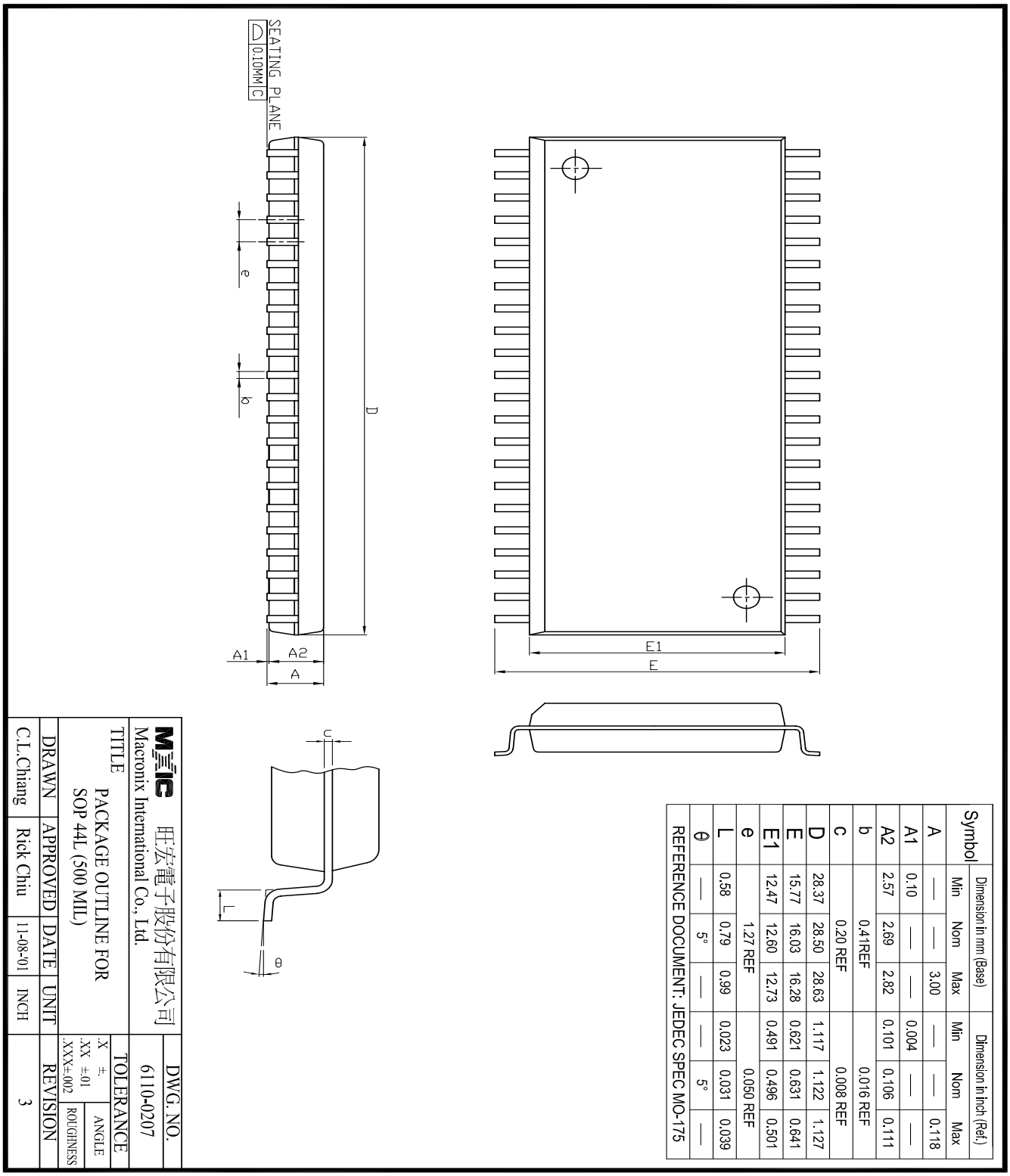
### RANDOM READ




Note:$\overline{CE}$, $\overline{OE}$ are enable

## PACKAGE INFORMATION

### 44-PIN PLASTIC SOP

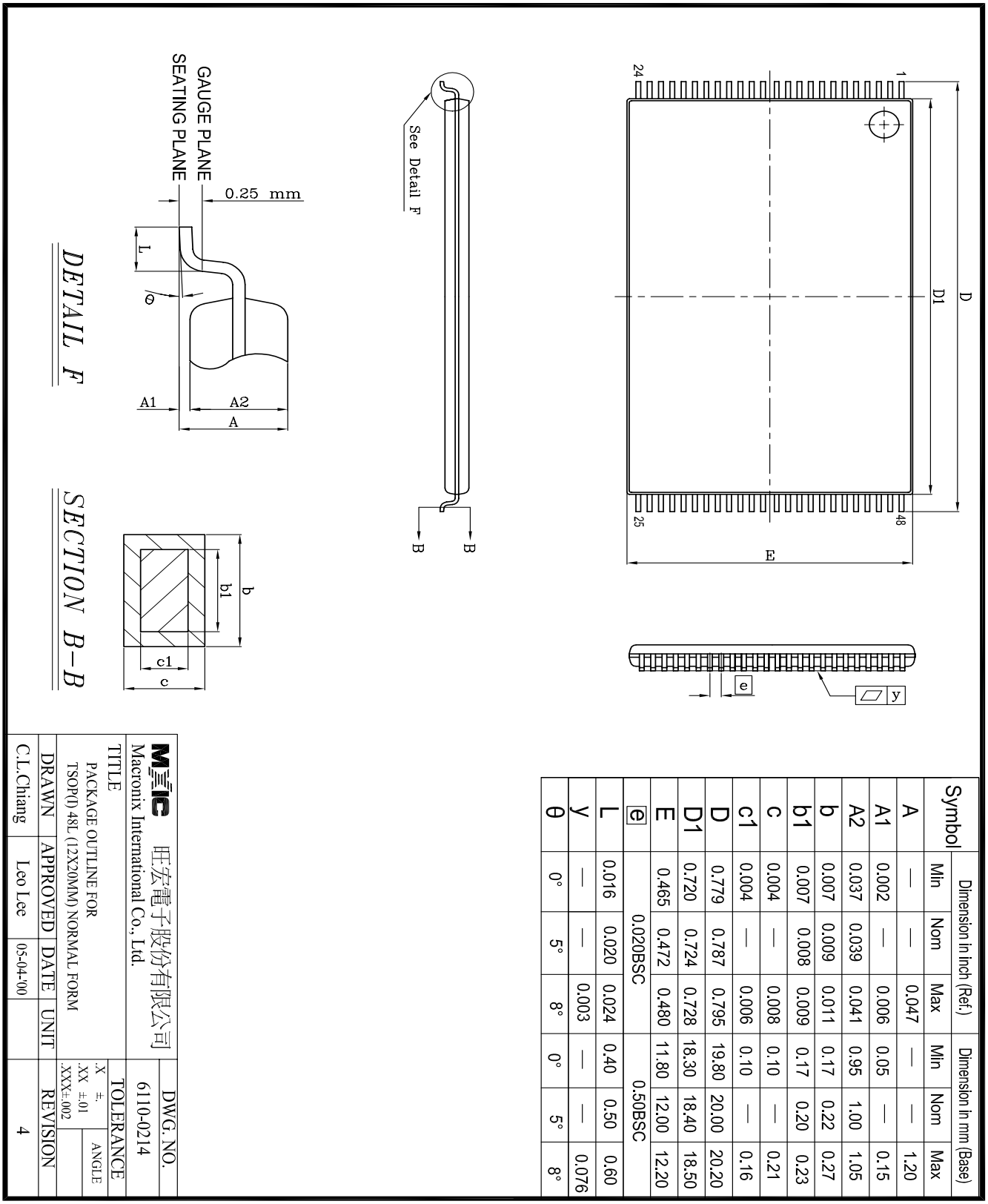



| Symbol | Dimension in mm (Base) | | | Dimension in inch (Ref.) | | |
|---|---|---|---|---|---|---|
| | Min | Nom | Max | Min | Nom | Max |
| A | — | — | 3.00 | — | — | 0.118 |
| A1 | 0.10 | — | — | 0.004 | — | — |
| A2 | 2.57 | 2.69 | 2.82 | 0.101 | 0.106 | 0.111 |
| b | | 0.41REF | | | 0.016 REF | |
| c | | 0.20 REF | | | 0.008 REF | |
| D | 28.37 | 28.50 | 28.63 | 1.117 | 1.122 | 1.127 |
| E | 15.77 | 16.03 | 16.28 | 0.621 | 0.631 | 0.641 |
| E1 | 12.47 | 12.60 | 12.73 | 0.491 | 0.496 | 0.501 |
| e | | 1.27 REF | | | 0.050 REF | |
| L | 0.58 | 0.79 | 0.99 | 0.023 | 0.031 | 0.039 |
| θ | — | 5° | — | — | 5° | — |

REFERENCE DOCUMENT: JEDEC SPEC MO-175

| | | | | |
|---|---|---|---|---|
| MXIC 旺宏電子股份有限公司 Macronix International Co., Ltd. | | | | DWG. NO. 6110-0207 |
| TITLE PACKAGE OUTLINE FOR SOP 44L (500 MIL) | | | | TOLERANCE .X ± .XX ±.01 .XXX±.002 ANGLE ROUGHNESS |
| DRAWN | APPROVED | DATE | UNIT | |
| C.L.Chiang | Rick Chiu | 11-08-'01 | INCH | REVISION 3 |

## 48-PIN PLASTIC TSOP




| Symbol | Dimension in inch (Ref.) | | | Dimension in mm (Base) | | |
|---|---|---|---|---|---|---|
| | Min | Nom | Max | Min | Nom | Max |
| A | — | — | 0.047 | — | — | 1.20 |
| A1 | 0.002 | — | 0.006 | 0.05 | — | 0.15 |
| A2 | 0.037 | 0.039 | 0.041 | 0.95 | 1.00 | 1.05 |
| b | 0.007 | 0.009 | 0.011 | 0.17 | 0.22 | 0.27 |
| b1 | 0.007 | 0.008 | 0.009 | 0.17 | 0.20 | 0.23 |
| c | 0.004 | — | 0.008 | 0.10 | — | 0.21 |
| c1 | 0.004 | — | 0.006 | 0.10 | — | 0.16 |
| D | 0.779 | 0.787 | 0.795 | 19.80 | 20.00 | 20.20 |
| D1 | 0.720 | 0.724 | 0.728 | 18.30 | 18.40 | 18.50 |
| E | 0.465 | 0.472 | 0.480 | 11.80 | 12.00 | 12.20 |
| e | | 0.020BSC | | | 0.50BSC | |
| L | 0.016 | 0.020 | 0.024 | 0.40 | 0.50 | 0.60 |
| y | — | — | 0.003 | — | — | 0.076 |
| θ | 0° | 5° | 8° | 0° | 5° | 8° |

| | | | |
|---|---|---|---|
| MXIC 旺宏電子股份有限公司 Macronix International Co., Ltd. | | | DWG. NO. 6110-0214 |
| TITLE PACKAGE OUTLINE FOR TSOP(I) 48L (12X20MM) NORMAL FORM | | | TOLERANCE .X ±. .XX ±.01 .XXX±.002 ANGLE |
| DRAWN | APPROVED | DATE | UNIT |
| C.L.Chiang | Leo Lee | 05-04-'00 | |
| | | | REVISION 4 |

## REVISION HISTORY

| Revision | Description | Page | Date |
|---|---|---|---|
| 2.1 | AC Characteristics: tOH 10ns --> 0ns | P3 | FEB/01/1999 |
| 2.2 | Add Order Information--Note:MX23C6410PC-10 only applys to supply voltage 5V±5% | P1 | OCT/02/2000 |
| 2.3 | Modify Package Information | P5,6,7 | OCT/09/2000 |
| 2.4 | Modify Operating Current:100mA-->70mA | P1,3 | JAN/15/2001 |
| 2.5 | Modify Package Information | P5~7 | JUL/17/2001 |
| | Added 44-pin TSOP package | P1,8 | |
| 2.6 | Move 42-pin PDIP Package to another new data sheet | P1,5 | JUL/20/2001 |
| 2.7 | Removed 44-pin TSOP Package | P1,7 | JAN/15/2002 |

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