THERMAL MODELING AND DESIGN OF 3D INTEGRATED CIRCUITS

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ABSTRACT

3D interconnect technology has attracted significant interest in the recent past as a means for enabling faster and more efficient integrated circuits (ICs). 3D integration relies on through-silicon vias (TSVs) and bonding of multiple active layers. While this approach provides several electrical benefits, it also offers significant challenges in thermal management. While some work has been done in the past in this field, a comprehensive treatment is still lacking. In the current work, analytical and finite-element models of heat transfer in 3D electronic circuits are developed. The models are used to investigate the limits of thermal feasibility of 3D electronics and to determine the improvements required in traditional packaging in order to accommodate 3D ICs. An analytical model for temperature distribution in a multi-die stack with multiple heat sources is developed. The analytical model is used to extend the traditional concept of thermal resistance in an IC to thermal resistance and thermal sensitivity matrices for a 3D IC. The impact of various geometric parameters and thermophysical properties on thermal performance of a 3D IC is investigated. It is shown that package thermal resistances play a more important role in determining temperature rise compared to thermal resistances intrinsic to the 3D technology, including thermal resistance of bonding layers and TSVs. As a result, an improved bonding layer or TSV thermal resistance does not offer much thermal benefit. An increase in thermal resistance of a 3D IC is predicted as compared to an equivalent System-on-Chip (SoC). This increase is found to be mainly due to the reduced chip footprint. The amount of improvement required in package and heat sink thermal resistances for a logic-on-memory 3D implementation to be thermally feasible is quantified. The results presented in this paper are expected to aid in the development of thermal design guidelines for 3D ICs.

KEY WORDS: 3D integrated circuits, 3D interconnects, Through-silicon via (TSV), thermal modeling, heat sink, thermal resistance, transient modeling.

NOMENCLATURE

Q	heat generation rate (W)
q	heat flow (W)
R_{ij}	Thermal resistance matrix (K/W)
R	Thermal resistance (K/W)
r_i	Thermal resistance of i^{th} strata non-dimensionalized by R_{hs}
S_{ij}	Thermal sensitivity matrix (K/W)
T	temperature (K)

Greek symbols

α	R_{pk} non-dimensionalized by R_{hs}
θ	Temperature rise above ambient (K)

Subscripts

1,2	die1 and die2 respectively
diel	dielectric
hs	heat sink
j	j^{th} die
pk	package

INTRODUCTION

The continued reduction of microelectronic device size over the past few decades according to Moore's law has led to unprecedented improvement in performance of electronic products. This miniaturization has been fueled by continued improvements in process technologies. As physical limits for several process technologies begin to be approached, the further reduction of device size is starting to get more and more challenging from both technological and financial perspective. This has fueled interest in other means of building faster and cheaper electronics. Examples include sub-ambient microprocessor operation [1], 3D-integrated microelectronics [2-4], etc. Vertically integrated 3-D circuits have attracted significant attention in the recent past due to several potential benefits. 3D integration is expected to address interconnect-delay related problems and enable integration of heterogeneous technologies [2]. A number of innovative process technologies go into the realization of a working 3D circuit. These include wafer thinning, etching and filling of high aspect ratio holes in silicon, inter-strata bonding, etc. [5-6]. A key component of 3D technology is a Through-silicon via (TSV) that enables communication between the two dies as well as with the package. A variety of integration technologies for realizing 3D integration have been demonstrated. These include both face-to-face integration [5] and back-to-face integration [7].

While 3D technology has some clearly established benefits in terms of electrical performance, it also exacerbates the already severe challenge of microelectronics cooling [8]. In addition to

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the fact that a 3D integrated electronic system has multiple heat generation sources, one must also account for the introduction of several new thermal resistances due to bonding between any two die. The implementation of heterogeneous integration must also take into consideration the different operating temperature requirements of individual stratum.

It is clear that successful application of 3D integration in products will require significant thermal analysis and establishment of thermal design rules governing feasibility of various integration options. Some papers in the past have tried to individually address some of the thermal issues related to 3D integration. Kleiner, *et al.* presented a simple, one-dimensional thermal analysis of a three-chip stack [9]. 3D FEM simulation was also used in this work to investigate the effect of interconnects on temperature distribution in a two-die stack. A thermal analysis of various 3D integration schemes has been presented [10]. Some work has been reported on optimizing the problem of placement of vias for heat dissipation in 3D ICs [11-12]. Numerical thermal simulations have been carried out to convert power dissipation distribution into a temperature distribution in a 3D IC [13]. Based on the past work, the development of a fundamental analytical model for heat transport in 3D integrated circuits is highly desirable. Such an analytical model will provide a framework in which to analyze the general problem of heat dissipation in 3D ICs, and will offer simple thermal design guidelines. On the theoretical front, it is important to re-interpret the concept of thermal resistances for a multi-source case and develop models that effectively analyze such cases. On the other hand, chip designers clearly need to be supplied with thermal design guidelines that address the limits of what can be 3D integrated without being thermally infeasible. For example, chip and package designers are interested in finding out the location of the maximum temperature in a given stacking arrangement. Further, there is interest in developing tools for thermal optimization of the stacking arrangement and smart design of the chip-package interface in order to alleviate the thermal dissipation problem. The influence of features inherent to 3D technology like through silicon vias (TSVs), inter-die bonding layers, etc. on the temperature distribution also needs to be investigated. The current work attempts to develop an analytical model to answer some of these questions. The next section describes an analytical 1-D model for heat transfer in a 3D IC. Associated numerical modeling is described in the following section. Finally, some representative results from the analytical and numerical modeling are presented.

ANALYTICAL MODEL FOR HEAT TRANSFER IN 3D-INTEGRATED ELECTRONICS

Heat transfer analysis in 3D microelectronics is complicated by the presence of multiple heat sources and the introduction of new thermal resistances posed by inter-die materials including interface resistances whose values are not readily available. In this section, we develop a simple, one-dimensional heat transfer model for a general multi-layer 3D integrated circuit to answer some of the fundamental heat transfer questions critical to the successful implementation of 3D technology. We assume uniform heat generation in the device planes and neglect heat spreading by assuming heat flow only normal to the device planes. In general, a 3D microelectronics system comprises of N strata mechanically connected to each other through an appropriate bonding technology. Each strata and interface is characterized by a thermal resistance R_{strata} and $R_{interface}$ respectively. The thermal resistances R_j between neighboring junctions can be calculated by summing up strata and interface resistances lying between them. By doing so, a thermal resistance network for this system can be arrived at. The general thermal resistance network, shown in Figure 1 comprises of N heat sources and (N+2) thermal resistances, including R_{hs} and R_{pk}, the resistances of the heat sink and package respectively. In figure 1, R_j is the thermal resistance between nodes j and j-1. T_j and Q_j represent the temperature and heat generation at node j respectively. Finally, q_j represents the heat flow from node j to node j-1. Heat is generated in the resistance network at each node and flows to the ambient through either the heat sink or package. The primary interest here is to determine the junction temperatures T_j. For low-power applications that operate without a heat sink, the thermal resistance of the heat sink may

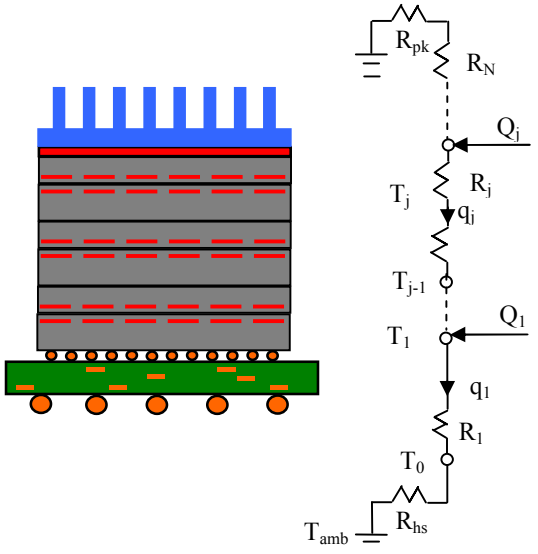

Fig 1. A general multistrata 3D IC structure and its equivalent thermal resistance network.

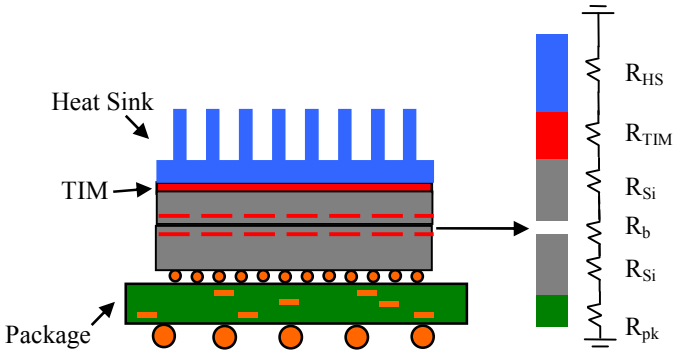

Fig 2. Schematic of a two-die 3D IC showing the specific thermal resistances of interest. R_b is the thermal resistance of the inter-strata bond layer and includes interface resistance.

be conveniently removed from this general analysis. This representation of the 3D multi-die stack differs from the two-resistor model used to describe the traditional single-die-in-package in the introduction of several new resistances and multiple heat sources. Physically speaking, heat generated in one stratum must travel through several other strata before dissipating into the package or heat sink. As a result, temperature rise in one stratum is influenced by heat generation not only in that stratum, but in all other strata as well. Thus, the traditional junction-to-ambient thermal resistance is inadequate as a measure of thermal performance. Under steady-state, temperature distribution in the various strata is governed by equations of energy conservation. For j=1, 2…N-1,

$$q_j = q_{j+1} + Q_j \tag{1}$$

For j=N, we have

$$q_N = q_{pk} + Q_N \tag{2}$$

Temperature and heat flow are related to each other as follows:

$$T_j - T_{j-1} = q_j \cdot R_j \tag{3}$$

Finally, the following equations govern the temperature of strata next to the heat sink and package respectively:

$$\begin{aligned} T_N - T_{amb} &= -q_{pk} \cdot R_{pk} \\ T_0 - T_{amb} &= q_1 \cdot R_{hs} \end{aligned} \tag{4}$$

Equations (1) through (4) represent (2N+2) equations that can be easily solved to determine the (2N+2) variables – T_0, T_1, T_2…, T_N, q_1, q_2…,q_N and q_{pk}. The solution is found to be

$$\begin{aligned} \frac{\theta_i}{R_{hs}} = &\sum_{j^*=i}^{N} Q_{j^*}\left(1-F_{j^*}\right)\left(1+\sum_{m=1}^{i} r_m\right) + \\ &\sum_{j^*=1}^{i-1} Q_{j^*}\left[\left(1-F_{j^*}\right)\left(1+\sum_{m=1}^{j^*} r_m\right) - F_{j^*}\sum_{m=j^*+1}^{i} r_m\right] \end{aligned} \tag{5}$$

where

$$F_{j^*} = \left(\frac{1+\sum_{m=1}^{j^*} r_m}{1+\alpha+\sum_{m=1}^{N} r_m}\right) \tag{6}$$

r_m represents the resistance of the m^{th} strata non-dimensionalized by R_{hs}. α is the package thermal resistance, similarly non-dimensionalized. θ_i represents the temperature rise above ambient in the i^{th} stratum.

Equations (5) and (6) represent the temperature distribution in the various strata, and help answer some of the key thermal questions likely to be encountered in designing 3D ICs. These include the maximum temperature attained, location of the hottest stratum, influence of the heat sink and package thermal resistances, the thermally optimum arrangement of the various strata and the sensitivity of the maximum temperature to various parameters of the problem.

Please note that in general, the hottest die is not necessarily the one farthest from the heat sink. Depending on the relative magnitude of heat generation in various dies, and the relative magnitude of package and heat sink thermal resistance, the hotspot may lie in any of the dies in the N-die stack.

The general solution represented by equations (5) and (6) takes on simpler forms for a number of special cases. Two special cases are of particular interest. One of them is a two-die stack, shown in Figure 2, which is the simplest and likely to be the first implementation of 3D technology. In this case, N=2, and the temperature of the two dies is given by

$$\begin{aligned} T_1 &= \frac{(Q_2(R_2+R_{hs})+Q_1(R_2+R_{hs}+R_b))(R_1+R_{pk})}{R_{hs}+R_1+R_b+R_2+R_{pk}} \\ T_2 &= \frac{(Q_2(R_b+R_1+R_{pk})+Q_1(R_1+R_{pk}))(R_2+R_{hs})}{R_{hs}+R_1+R_b+R_2+R_{pk}} \end{aligned} \tag{7}$$

where subscripts 1 and 2 refer to the two die and b refers to the inter-die bond layer, including any interface resistance between bond pads. Note that die1 is placed next to the package and die2 next to the heat sink. Note from equation (7) that die1 is not necessarily the hotter of the two. In fact, it is easy to show that die2 is the hotter die only if

$$\frac{Q_1}{Q_2} > \frac{(R_{hs}+R_2)}{(R_{pk}+R_1)} \tag{8}$$

A second interesting special case of the general solution is the one where there is no heat loss through the package. This may be relevant for high power applications where a heat sink removes most of the heat, and the package end is conservatively assumed to be insulated. In this case, the temperature solution for a two-die stack is given by

$$\begin{aligned} T_2 &= (Q_1+Q_2)R_{hs} \\ T_1 &= (Q_1+Q_2)R_{hs} + Q_1R_b \end{aligned} \tag{9}$$

Note that this case is similar to the one where no heat sink is available and all heat loss may be assumed to occur through the package. Equation (9) applies, with the package resistance replacing the heat sink resistance.

It must be noted that as shown in equations (5) and (6), the relative magnitudes of the various thermal resistances in the network play a key role in determining the temperature profile. Consequently, a certain type of 3D integration may be thermally feasible for one packaging technology, and not so for another one. In most cases, the largest resistance to heat flow occurs outside the multidie stack, since the heat sink and package resistances are much larger than die-level thermal resistances. Thus, heat sink and package resistances are the critical parameter that largely determine the thermal performance of the multi-die stack.

As an example, consider a two-die stack consisting of 300 μm thick dies with a 10 mm by 10 mm cross-section. Heat sink and package thermal resistances are assumed to be 2 K/W and 20 K/W respectively. These values are usually available from detailed thermal modeling of the heat sink and package. Thermal conductivity of silicon is taken to be 148 W/mK. In

comparison to the heat sink and package resistances, the silicon resistance is around 0.02 K/W. The inter-strata bond layer is assumed to be 10 μm thick, with an effective thermal conductivity of 0.1 W/mK. A subsequent section discusses the determination of this parameter. Assuming each die dissipates 10W, the temperature rise in the two die are determined using the model presented here to be 43.8 and 36.7 K respectively. If the bottom die (the die close to the package) dissipates 18 W and the top die dissipates 2W, the temperature rise of the bottom die increases to 50.7 K, while the top die temperature rise actually reduces to 35.3 K. If a finer pad pitch or reduced interface resistance results in an improvement in the inter-strata bond layer thermal conductivity to 1 W/mK instead of 0.1 W/mK as considered above, the die temperature rise values are 37.4 K and 36.6 K respectively, when each die dissipates 10 W power. Note that better thermal conductance in the bond layer brings the two die temperatures closer, as expected.

THERMAL RESISTANCE MATRICES FOR 3D TECHNOLOGY

Equations (5) and (6) throw light on the modifications required for using the concept of junction-to-air thermal resistance to characterize thermal performance of 3D circuits. The traditional single junction-to-air thermal resistance computed from the total temperature rise and power dissipation in the die is simply not sufficient for describing the thermal performance of a multidie stack. With the presence of multiple heat sources and multiple internal resistances, the concept of a single-valued junction-to-air thermal resistance must be expanded into a resistance matrix. We propose the use of R_{ij}, defined as the temperature rise in the i^{th} strata due to heat dissipation in the j^{th} strata *alone*, as a thermal resistance matrix characterizing the 3D stack. From the general solution, it is easy to determine that

$$R_{ij} = \frac{\theta_i}{Q_j} = \left[\sum_{k=1}^{i-1} q_{ki} \left(\begin{array}{l} (1-F_k)\left(1+\sum_{m=1}^{k} r_m\right) \\ -F_k \sum_{m=k+1}^{i} r_m + \\ \sum_{k=i}^{N} q_{ki}(1-F_k)\left(1+\sum_{m=1}^{i} r_m\right) \end{array} \right) \right] \quad (10)$$

where $q_{ki}=Q_k/Q_i$.

Further, change in temperature of the i^{th} strata due to an incremental change in heat generation in the j^{th} strata is a quantity that chip and package designers are likely to be very interested in. The thermal sensitivity matrix S_{ij} is given by

$$S_{ij} = \frac{\partial \theta_i}{\partial Q_j} = \begin{array}{ll} R_{hs}(1-F_j)\left(1+\sum_{m=1}^{i} r_m\right) & i \le j \\ R_{hs}(1-F_j)\left(1+\sum_{m=1}^{j} r_m\right) - Fj \sum_{m=j+1}^{i} r_m & i > j \end{array} \quad (11)$$

Note the subtle difference between R_{ij} and S_{ij}. While S_{ij} is independent of heat generation terms, and is thus closer in nature to the traditional junction-to-air thermal resistance for a single die, R_{ij} is dependent on the heat generation itself due to coupling. Chip and package designers must be aware of the importance of both R_{ij} and S_{ij}, and the complex coupling of temperature with multiples heat sources in order to come up with smart thermal design of 3D integrated circuits.

DETERMINATION OF INTER-STRATA THERMAL CONDUCTANCE

While the values of thermal resistance for heat sinks and packages may be available from previous numerical simulations, not much work is available for obtaining values for the inter-strata thermal resistance. A numerical model is developed for the determination of this parameter. The thickness, material and area density of micropads and the nature of the bonding between strata influence the inter-strata thermal resistance. Metal bond pads were assumed to be distributed uniformly on the bonding planes of both strata, and a unit cell, shown in Figure 3, is used for simulations. The bonding pad of the top die is comprises of two metal films, while the bottom die bonding pad has only one metal film. This is a commonly used bonding technology where the two metals form an intermetallic compound at high temperature to form the bond [14]. The space around the bonding pads may be an underfill material or may simply be air. Please note that the outer dimensions of the model geometry are determined by the micropad area density. A unit heat flux is applied on one face of the model while a constant temperature boundary condition is applied on the other face. All other faces are adiabatic by symmetry. The effective thermal conductivity of

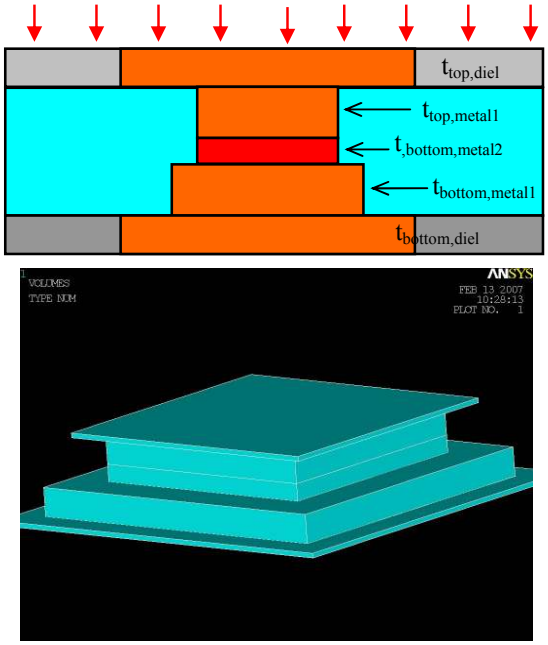

Fig 3. Geometry of the micropad bond structure simulated in ANSYS for determining the effective thermal resistance.

the bond layer is determined from the resulting temperature difference between the two faces. Figure 4 shows this parameter as a function of the area density of bond pads as well as the thermal conductivity of the filler material. For commonly used values of these parameters, the effective thermal conductivity of the bond layer falls in the same range as typical epoxies and dielectric materials. This happens despite the presence of highly conducting metal pads due to their low area density. While the thermal conductivity can be increased by increasing the bond pad density, this parameter is likely to be limited by electrical connection considerations.

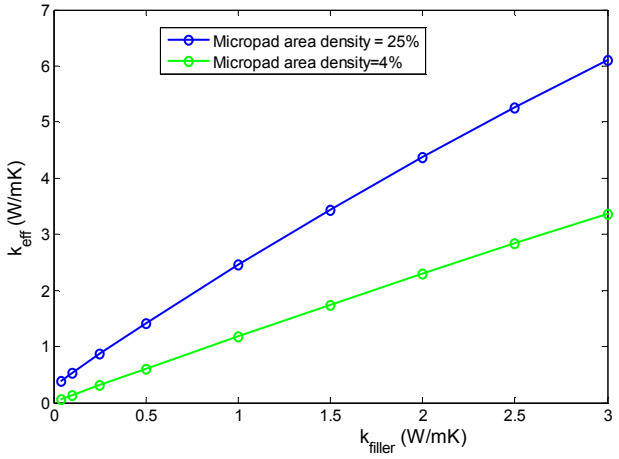

Fig 4. Variation of the effective thermal conductivity of the interdie bond layer as a function of the thermal conductivity of filler material and the micropad area density.

Nevertheless, due to the small thickness of the interstrata bond layer, the value of the thermal resistance is quite small compared to package and heat sink resistances. As a result, efforts to improve the bond layer thermal conductance by, for example, incorporating dummy metal bond pads will not provide much benefit in terms of reduced junction temperature, since this value is already quite high. While this simulation does not take into account interface resistance, it is easy to add the value of the interface resistance to the appropriate resistance in the thermal resistance network of figure 1, provided it is known in advance. The significance of the interface resistance depends on the type of integration used. For example, the interface resistance is expected to be much lower for Cu-Cu bonding compared to Cu-Sn-Cu bonding.

RESULTS AND DISCUSSION

This section discusses several interesting results based on the analytical model for two-die 3D ICs presented previously. The analytical model is capable of providing several practical thermal design guidelines for 3D electronics. Some of the issues that can be addressed include determining the optimal arrangement of various strata, the influence of internal thermal resistances on the maximum temperature, the improvements in heat sink and package required for 3D integration, etc. For simplicity, the die dissipating more power than the other is referred to as the logic die, and the other die is referred to as the memory die.

Figure 5 shows the dependence of temperature of the logic die on thermal resistance of the inter-die bond layer. As expected, the die temperature exhibits only weak dependence due to the small value of the inter-die bond thermal resistance compared to other resistances in the circuit. This effect is prominent regardless of whether logic or memory die is placed closer to the package. Figure 5 demonstrates that efforts to improve thermal resistance of the interstrata bond layer do not result in much thermal benefit. The influence of the silicon die thermal resistance on the maximum temperatures is similar. Finite-element simulations investigating the effect of metal-filled through silicon vias (TSVs) have shown that TSVs do not influence the die temperature much, even with an ultrafine pitch. This result is along expected lines, based on the results from the analytical model discussed previously. Note,

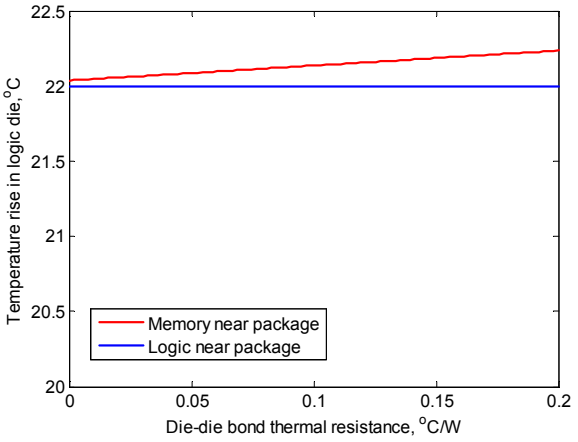

Fig 5. Logic die temperature as a function of thermal resistance of interdie bond layer. Memory die is assumed to dissipate 10% of the logic die power. A very weak dependence is observed regardless of which die is stacked next to the package.

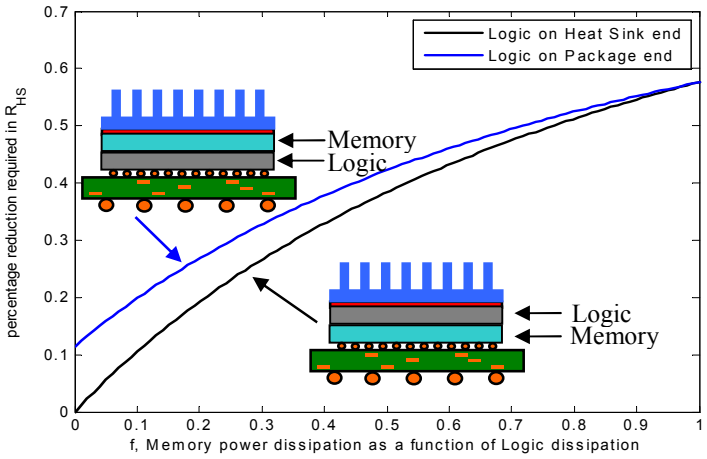

Fig 6. A plot showing the improvement required in heat sink thermal resistance as a function of power dissipation in the memory die. The baseline case is a single logic die. Note the dependence on the stacking sequence.

however, that TSVs might still be useful for local heat transport away from hotspots. A smart thermal design and placement of TSVs will require prior knowledge of expected hotspot locations. This underlines the importance of integrated thermal-electrical design of 3D electronics.

Figure 6 shows the improvement required in the heat sink thermal resistance in order to incorporate an extra die dissipating a given amount of power while maintaining the same maximum junction temperature. For a memory die dissipating around 10% of the power dissipated by the logic die, an improvement of around 10% in the thermal performance of the heat sink will be necessary to maintain the same maximum temperature. The required improvement is only weakly dependent on the inter-strata bond layer especially if one of the dies dissipates much lesser power than the other. Figure 6 provides thermal design guidelines for 3D chip and package design and places limits on the thermal feasibility of 3D integration.

Clearly, there is an inherent trade-off between electrical and thermal design of 3D integrated circuits. While it is thermally optimal to place the die dissipating more power (logic die in case of a logic-on-memory integration) closer to the heat sink rather than the package, this approach is likely to be more challenging in terms of integration since the logic die requires more I/O connections to the package, and thus more through-silicon vias will be needed to be routed through the memory die in order to reach the logic die, which is not electrically optimal. Thus, it is required to develop an integrated approach towards 3D design that considers both electrical and thermal requirements.

It is also interesting to compare 3D integration technology with System-on-Chip (SoC) technology, wherein multiple heterogeneous components (for example, memory and logic) are placed on the same silicon die. The stacking of logic and memory on top of each other instead leads to a different thermal problem that needs to be fully understood before 3D technology can offer the same functionality as SoC without running into significant thermal issues. Table 1 compares the thermal resistance based on maximum junction temperature and total power dissipation for an SoC die in package and a number of possible 3D implementations of the same SoC die in the same package. These numbers are based on finite-element numerical simulations for the 3D stack or SoC in the same package. The heat sink and package were fully simulated. Note that 3D stacking is expected to reduce the die footprint compared to a SoC. While the exact amount of reduction depends on architecture optimization, one could assume for thermal analysis that the total area of the two dies in a 3D implementation remains the same as the SoC. In that case, as shown in columns 1 and 2 of Table 1, there is an increase in maximum temperature when moving to 3D. However, this increase in temperature is not due to a feature inherent to the 3D technology, but rather due to the reduced footprint. To validate this point, the maximum temperature rise was computed for a 3D two-die stack with the same footprint area as the SoC. This value, shown in column 3, is close to the maximum temperature rise in the SoC implementation, shown in column 1. In conclusion, the 3D integration technology is likely to require thermally superior packaging compared to an equivalent SoC, but this is due to the reduced footprint area of the 3D (which leads to several other design and manufacturing related benefits), and not due to a feature inherent to the 3D technology. The drive for reduced die footprints is ongoing even in traditional non-3D technologies, and thermal engineers will need to continue to innovate to accommodate ever-shrinking dies. The introduction of 3D technology may accelerate this shrinkage, and thus require rapid introduction of new and innovative packaging and cooling solutions.

Case	Junction-to-air thermal resistance
7.8 mm by 7.8 mm SoC, dissipating 1.1 W	12.8 K/W
5.5 mm by 5.5 mm 3D stack, dissipating 1.0 and 0.1 W (total area is the same as SoC)	15.6 K/W
7.8 mm by 7.8 mm 3D stack, dissipating 1.0 and 0.1 W (total area is double of the SoC; same footprint area)	13.5 K/W
3.9 mm by 3.9 mm 3D stack, dissipating 1.0 and 0.1 W (total area is half of the SoC)	19.5 K/W

Table 1. Thermal resistances of a System-on-Chip with a comparable two-die 3D IC design. Values show the increase in thermal resistance due to the reduced chip area in a 3D IC. SoC and 3D IC of the same chip footprint area have comparable values.

CONCLUSIONS

Three-dimensional integrated circuits are expected to prominently feature in future electronics products. A significant effort is being put into solving several process and design technology related challenges. At the same time, efforts are also needed for meeting thermal challenges of 3D integration. The current work offers a framework in which to analyze the thermal performance of 3D integrated circuits through an analytical model for predicting temperature rise in a multi-die, multisource thermal resistor network. This work shows the need to extend the traditional understanding of thermal performance of microelectronics in terms of thermal resistance values to thermal resistance matrices due to the presence of multiple sources. Expressions for these matrices are derived. A trade-off between thermal and electrical design of 3D ICs is identified. The thermal resistances within a 3D structure are expected to be much smaller than those outside, including the heat sink and package. As a result, thermal optimization of 3D ICs needs to be driven by reduction in thermal resistance of the heat sink and package, and not of the 3D IC itself. The thermal challenge surrounding the 3D technology is exacerbated by the fact that 3D technology will cause reduction in the footprint area, which would only necessitate a quicker introduction of innovative cooling technologies and an integration of electrical and thermal design process for 3D integrated microelectronics.

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