Universidad Nacional Autónoma de México
Facultad de Ingeniería

Práctica 7
Direccionamiento por entrada-estado y trayectoria

Diseño Digital VLSI

Clave: 1535

Profesor: Dr. Roberto Giovanni Ramírez Chavarría

Grupo: 4

Integrantes:

- Mendoza Guillén Sergio Adrián
- Navarro Velazquez Jorge Luis
- Ramirez Villa Brandon Alberto
- Vargas Badillo Ricardo Antonio

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Objetivos

Comprender los funcionamientos de los tipos de direccionamiento por entrada-estado y por trayectoria, y encontrar las diferencias que tiene cada método con respecto al otro, observando sus ventajas y desventajas.

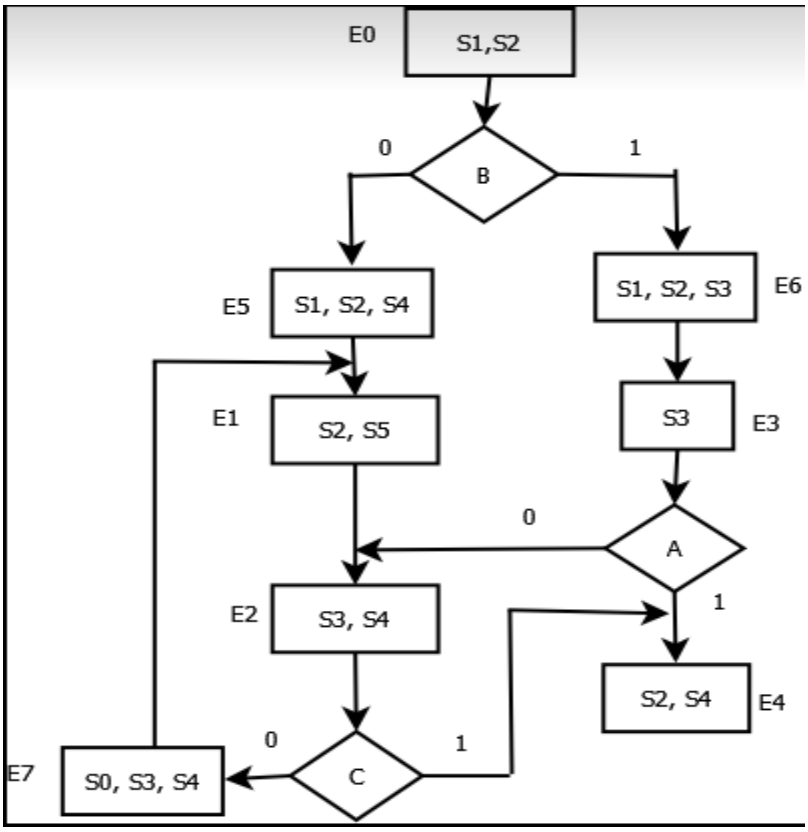
Lista de material:

- Tarjeta FPGA

Problema:

Resolver la siguiente Carta ASM por ambos métodos de direccionamiento

A) Direccionamiento Entrada-Estado

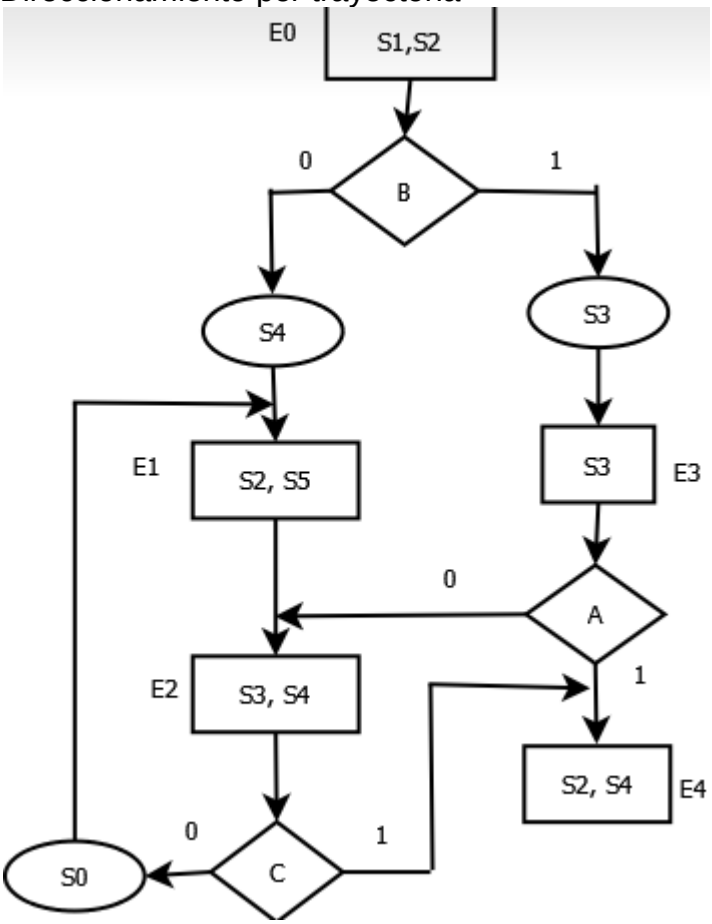


8 Estados {E0, E1, E2, E3, E4, E5, E6, E7}
3 Entradas {A, B, C}
6 Salidas {S0, S1, S2, S3, S4, S5, S6}
E0=000
E1=001
E2= 010
E3=011
E4=100
E5=101
E6=110
E7=111
Codificar entradas
Vaux=00
A=01
B=10
C=11

Tabla 1

Dirección			Contenido de memoria														
Edo. presente			Prueba Q		LF			LV			Salidas						
											S0	S1	S2	S3	S4	S5	
0	0	0	1	0	1	0	1	1	1	0	0	1	1	0	0	0	
0	0	1	0	0	0	1	0	0	1	0	0	0	1	0	0	1	
0	1	0	1	1	1	1	1	1	0	0	0	0	0	1	1	0	
0	1	1	0	1	0	1	0	1	0	0	0	0	0	1	0	0	
1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	
1	0	1	0	0	0	0	1	0	0	1	0	1	1	0	1	0	
1	1	0	0	0	0	1	1	0	1	1	0	1	1	1	0	0	
1	1	1	0	0	0	0	1	0	0	1	1	0	0	1	1	0	

B) Direccionamiento por trayectoria



5 Estados {E0, E1, E2, E3, E4}
3 Entradas {A, B, C}
6 Salidas {S0, S1, S2, S3, S4, S5, S6}
E0=000
E1=001
E2= 010
E3=011
E4=100

Tabla2

Edo. Presente			Entrada			Liga			Salidas					
			A	B	C				S0	S1	S2	S3	S4	S5
0	0	0	0	0	0	0	0	1	0	1	1	0	1	0
0	0	0	0	0	1	0	0	1	0	1	1	0	1	0
0	0	0	0	1	0	0	1	1	0	1	1	1	0	0
0	0	0	0	1	1	0	1	1	0	1	1	1	0	0
0	0	0	1	0	0	0	0	1	0	1	1	0	1	0
0	0	0	1	0	1	0	0	1	0	1	1	0	1	0
0	0	0	1	1	0	0	1	1	0	1	1	1	0	0
0	0	0	1	1	1	0	1	1	0	1	1	1	0	0
0	0	1	0	0	0	0	1	0	0	0	1	0	0	1
0	0	1	0	0	1	0	1	0	0	0	1	0	0	1
0	0	1	0	1	0	0	1	0	0	0	1	0	0	1
0	0	1	0	1	1	0	1	0	0	0	1	0	0	1
0	0	1	1	0	0	0	1	0	0	0	1	0	0	1
0	0	1	1	0	1	0	1	0	0	0	1	0	0	1
0	0	1	1	1	0	0	1	0	0	0	1	0	0	1
0	0	1	1	1	1	0	1	0	0	0	1	0	0	1
0	1	0	0	0	0	0	0	1	1	0	0	1	1	0
0	1	0	0	0	1	1	0	0	0	0	1	0	1	0
0	1	0	0	1	0	0	0	1	1	0	0	1	1	0
0	1	0	0	1	1	1	0	0	0	0	1	0	1	0
0	1	0	1	0	0	0	0	1	1	0	0	1	1	0
0	1	0	1	0	1	1	0	0	0	0	1	0	1	0
0	1	0	1	1	0	0	0	1	1	0	0	1	1	0
0	1	0	1	1	1	1	0	0	0	0	1	0	1	0
0	1	1	0	0	0	0	1	0	0	0	0	1	0	0
0	1	1	0	0	1	0	1	0	0	0	0	1	0	0
0	1	1	0	1	0	0	1	0	0	0	0	1	0	0
0	1	1	0	1	1	0	1	0	0	0	0	1	0	0
0	1	1	1	0	0	1	0	0	0	0	0	1	0	0
0	1	1	1	0	1	1	0	0	0	0	0	1	0	0
0	1	1	1	1	0	1	0	0	0	0	0	1	0	0
0	1	1	1	1	1	1	0	0	0	0	0	1	0	0
1	0	0	0	0	0	0	0	0	0	0	1	0	1	0
1	0	0	0	0	1	0	0	0	0	0	1	0	1	0
1	0	0	0	1	0	0	0	0	0	0	1	0	1	0
1	0	0	0	1	1	0	0	0	0	0	1	0	1	0
1	0	0	1	0	0	0	0	0	0	0	1	0	1	0
1	0	0	1	0	1	0	0	0	0	0	1	0	1	0
1	0	0	1	1	0	0	0	0	0	0	1	0	1	0
1	0	0	1	1	1	0	0	0	0	0	1	0	1	0

A) Resumen del programa de Direccionamiento entrada-estado

accs_miRom Project Status (10/15/2019 - 20:51:10)			
Project File:	Dierecionestado.xise	**Parser Errors:**	No Errors
Module Name:	accs_miRom	**Implementation State:**	Programming File Generated
Target Device:	xc6slx9-3csg225	**•Errors:**	No Errors
Product Version:	ISE 14.7	**•Warnings:**	2 Warnings (2 new)
Design Goal:	Balanced	**•Routing Results:**	All Signals Completely Routed
Design Strategy:	Xilinx Default (unlocked)	**•Timing Constraints:**	All Constraints Met
Environment:	System Settings	**•Final Timing Score:**	0 (Timing Report)

Device Utilization Summary				[-]
Slice Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Number of Slice Registers	43	11,440	1%	
Number used as Flip Flops	43			
Number used as Latches	0			
Number used as Latch-thrus	0			
Number used as AND/OR logics	0			
Number of Slice LUTs	70	5,720	1%	
Number used as logic	69	5,720	1%	
Number using O6 output only	38			
Number using O5 output only	24			
Number using O5 and O6	7			
Number used as ROM	0			
Number used as Memory	0	1,440	0%	
Number used exclusively as route-thrus	1			
Number with same-slice register load	0			
Number with same-slice carry load	1			
Number with other load	0			
Number of occupied Slices	20	1,430	1%	
Number of MUXCYs used	28	2,860	1%	
Number of LUT Flip Flop pairs used	71			
Number with an unused Flip Flop	34	71	47%	
Number with an unused LUT	1	71	1%	
Number of fully used LUT-FF pairs	36	71	50%	
Number of unique control sets	3			
Number of slice register sites lost to control set restrictions	13	11,440	1%	
Number of bonded IOBs	19	160	11%	
Number of LOCed IOBs	19	19	100%	

Number of RAMB16BWERs	0	32	0%	
Number of RAMB8BWERs	0	64	0%	
Number of BUFIO2/BUFIO2_2CLKs	0	32	0%	
Number of BUFIO2FB/BUFIO2FB_2CLKs	0	32	0%	
Number of BUFG/BUFGMUXs	1	16	6%	
Number used as BUFGs	1			
Number used as BUFGMUX	0			
Number of DCM/DCM_CLKGENs	0	4	0%	
Number of ILOGIC2/ISERDES2s	0	200	0%	
Number of IODELAY2/IODRP2/IODRP2_MCBs	0	200	0%	
Number of OLOGIC2/OSERDES2s	0	200	0%	
Number of BSCANs	0	4	0%	
Number of BUFHs	0	128	0%	
Number of BUFPLLs	0	8	0%	
Number of BUFPLL_MCBs	0	4	0%	
Number of DSP48A1s	0	16	0%	
Number of ICAPs	0	1	0%	
Number of MCBs	0	2	0%	
Number of PCILOGICSEs	0	2	0%	
Number of PLL_ADVs	0	2	0%	
Number of PMVs	0	1	0%	
Number of STARTUPs	0	1	0%	
Number of SUSPEND_SYNCs	0	1	0%	
Average Fanout of Non-Clock Nets	2.21			

Performance Summary			[-]
Final Timing Score:	0 (Setup: 0, Hold: 0)	**Pinout Data:**	Pinout Report
Routing Results:	All Signals Completely Routed	**Clock Data:**	Clock Report
Timing Constraints:	All Constraints Met		

Detailed Reports					[-]
Report Name	**Status**	**Generated**	**Errors**	**Warnings**	**Infos**
Synthesis Report	Current	mar. 15. oct. 20:47:58 2019	0	2 Warnings (2 new)	3 Infos (3 new)
Translation Report	Current	mar. 15. oct. 20:49:43 2019	0	0	0
Map Report	Current	mar. 15. oct. 20:50:17 2019	0	0	6 Infos (6 new)
Place and Route Report	Current	mar. 15. oct. 20:50:32 2019	0	0	3 Infos (3 new)
Power Report					
Post-PAR Static Timing Report	Current	mar. 15. oct. 20:50:41 2019	0	0	4 Infos (4 new)
Bitgen Report	Current	mar. 15. oct. 20:50:54 2019	0	0	0

Secondary Reports		[-]
Report Name	**Status**	**Generated**
WebTalk Report	Current	mar. 15. oct. 20:50:55 2019
WebTalk Log File	Current	mar. 15. oct. 20:51:09 2019

B) Resumen del programa de direccionamiento por trayectoria

accs_miRom Project Status (10/15/2019 - 20:59:43)			
Project File:	travectoria.xise	**Parser Errors:**	No Errors
Module Name:	accs_miRom	**Implementation State:**	Programming File Generated
Target Device:	xc6slx9-3csg225	**•Errors:**	No Errors
Product Version:	ISE 14.7	**•Warnings:**	No Warnings
Design Goal:	Balanced	**•Routing Results:**	All Signals Completely Routed
Design Strategy:	Xilinx Default (unlocked)	**•Timing Constraints:**	All Constraints Met
Environment:	System Settings	**•Final Timing Score:**	0 (Timing Report)

Device Utilization Summary [-]				
Slice Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Number of Slice Registers	47	11,440	1%	
Number used as Flip Flops	47			
Number used as Latches	0			
Number used as Latch-thrus	0			
Number used as AND/OR logics	0			
Number of Slice LUTs	71	5,720	1%	
Number used as logic	70	5,720	1%	
Number using O6 output only	37			
Number using O5 output only	24			
Number using O5 and O6	9			
Number used as ROM	0			
Number used as Memory	0	1,440	0%	
Number used exclusively as route-thrus	1			
Number with same-slice register load	0			
Number with same-slice carry load	1			
Number with other load	0			
Number of occupied Slices	22	1,430	1%	
Number of MUXCYs used	28	2,860	1%	
Number of LUT Flip Flop pairs used	75			
Number with an unused Flip Flop	34	75	45%	
Number with an unused LUT	4	75	5%	
Number of fully used LUT-FF pairs	37	75	49%	
Number of unique control sets	4			
Number of slice register sites lost to control set restrictions	17	11,440	1%	
Number of bonded IOBs	19	160	11%	
Number of LOCed IOBs	19	19	100%	
Number of RAMB16BWERs	0	32	0%	
Number of RAMB8BWERs	0	64	0%	
Number of BUFIO2/BUFIO2_2CLKs	0	32	0%	
Number of BUFIO2FB/BUFIO2FB_2CLKs	0	32	0%	
Number of BUFG/BUFGMUXs	2	16	12%	

Number used as BUFGs	2			
Number used as BUFGMUX	0			
Number of DCM/DCM_CLKGENs	0	4	0%	
Number of ILOGIC2/ISERDES2s	0	200	0%	
Number of IODELAY2/IODRP2/IODRP2_MCBs	0	200	0%	
Number of OLOGIC2/OSERDES2s	0	200	0%	
Number of BSCANs	0	4	0%	
Number of BUFHs	0	128	0%	
Number of BUFPLLs	0	8	0%	
Number of BUFPLL_MCBs	0	4	0%	
Number of DSP48A1s	0	16	0%	
Number of ICAPs	0	1	0%	
Number of MCBs	0	2	0%	
Number of PCILOGICSEs	0	2	0%	
Number of PLL_ADVs	0	2	0%	
Number of PMVs	0	1	0%	
Number of STARTUPs	0	1	0%	
Number of SUSPEND_SYNCs	0	1	0%	
Average Fanout of Non-Clock Nets	2.18			

Performance Summary			[-]
Final Timing Score:	0 (Setup: 0, Hold: 0)	**Pinout Data:**	Pinout Report
Routing Results:	All Signals Completely Routed	**Clock Data:**	Clock Report
Timing Constraints:	All Constraints Met		

Detailed Reports					[-]
Report Name	**Status**	**Generated**	**Errors**	**Warnings**	**Infos**
Synthesis Report	Current	dom. 13. oct. 14:04:08 2019	0	0	0
Translation Report	Current	dom. 13. oct. 14:31:28 2019	0	0	0
Map Report	Current	dom. 13. oct. 14:31:38 2019	0	0	6 Infos (0 new)
Place and Route Report	Current	dom. 13. oct. 14:31:46 2019	0	0	3 Infos (0 new)
Power Report					
Post-PAR Static Timing Report	Current	dom. 13. oct. 14:31:54 2019	0	0	4 Infos (0 new)
Bitgen Report	Current	mar. 15. oct. 20:59:29 2019	0	0	0

Secondary Reports			[-]
Report Name	**Status**	**Generated**	
WebTalk Report	Current	mar. 15. oct. 20:59:30 2019	
WebTalk Log File	Current	mar. 15. oct. 20:59:42 2019	

Conclusión:

Como podemos observar al realizar la comparación entre ambos métodos de direccionamiento podemos concluir que el método de direccionamiento por trayectoria es más rápido que el método de direccionamiento entrada-estado, esto se debe principalmente a la creación de nuevos estados para la sustitución de las entradas condicionales (debido a que este método no permite el uso de entradas condicionales) como se puede observar en su carta ASM, esta acción involucra que se tengan que perder más ciclos de reloj (y por ende el uso de más tiempo) para obtener la misma solución. En cuestión de hardware podemos observar algo completamente opuesto a los visto anteriormente ya que el método de direccionamiento entrada-estado se puede considerar mejor que el método de direccionamiento por trayectoria debido al uso de un menor número de

dispositivos lógicos, por ejemplo los flip flops que usa el primer método (Entrada-Estado) fueron 43 y el segundo (por Trayectoria) fue de 47 lo cual puede considerarse como una diferencia poco significativa pero a mayor tamaño de programa (mayores entradas, salidas, estados) esta diferencia podría influir de gran manera. Al finalizar podemos concluir que ambos métodos tiene ventajas y desventajas, la mejor opción sería necesario adecuarla a la problemática que queremos resolver y a los recursos que tengamos disponibles.