BASANT KHALIL

🛅 <u>LinkedIn</u> │ 📕 614-717-8842 │ 🤀 <u>BasantKhalil.com</u> │ 🎽 bak94@cornell.edu │ 🗘 <u>GitHub</u>

Education

Bachelor of Science, Summa Cum Laude

Ithaca. NY

08/2020 - 06/2023

Double Major in Computer Science & Electrical and Computer Engineering, GPA: 4.1

IEEE-Eta Kappa Nu (IEEE-HKN), the International Honor Society of Electrical and Computer Engineering, & Tau Beta Pi, the National Engineering Honor Society Key Courses: Database, Data structures & Algorithms, Artificial Intelligence, Machine Learning, Operating Systems, Computer Architecture, Embedded Systems, Distributed Computing, System

High School Honor Diploma

Dublin Jerome High School

Dublin, OH

09/2018 - 06/2020

Valedictorian; Summa Cum Laude; GPA: 5.0

Professional Experience

Software Engineering Intern: Full Stack

Hewlett Packard Enterprise

Durham, NC

05/2023 - Current

Accelerated the development & implementation of a Bisbee Sustainability Dashboard, leveraging Kotlin, Azure, AWS, Confluence, Docker, Maven, JIRA & GLCP Ops Management data to monitor energy usage and emissions, resulting in a 20% reduction in customers' IT estates' carbon footprint.

Drove collaboration with the Living Progress team at HPE to refine emissions modeling, achieving a significant 25% increase in accuracy (equivalent to a reduction of 10,000 metric tons of emissions per year). Provided precise energy usage and emissions data to support HPE's net zero goals, while ensuring compliance and strengthening sustainability initiatives through reliable reporting on energy consumption.

Research Assistant: Capra Research Group

Ithaca, NY

05/2023 - Current

Single-handedly created an extraordinary extension for VSCode, revolutionizing the debugging process for Calyx files by constructing "cider-dap," a sub-crate implementing the Debug Adapter Protocol (DAP) utilizing Rust, C++, Python, REST, JavaScript and SystemVerilog, ultimately achieving a remarkable 30% boost in developer productivity.

Accelerated identification & resolution of programming errors by leveraging "cider-dap" for seamless attachment & startup functionalities, resulting in an average time savings of 18% during debugging sessions and reducing initialization time by 15%.

Pioneered the optimization & transformation of programs into synthesizable hardware designs within the Calyx compiler. Streamlined processes by simplifying high-level semantics encoding, reducing development time by ${f 30}\%$, and improving hardware accelerators' performance by ${f 15}\%$.

Teaching Assistant

Ithaca, NY

08/2021 - 05/2023

For Analysis of Algorithms (CS 4820); Discrete Structures (CS 2800); and Calculus for Engineers (Math 1910).

Collaborated closely with faculty members to enhance student learning for 500+ students by developing and delivering 50+ engaging instructional materials, including visually appealing presentations, informative handouts, and interactive online resources.

Led the successful development and implementation of an advanced autograder system, automating the evaluation of coding projects for a class of 450+ students, resulting in a 25% improvement in grading accuracy and a reduction of regrade requests by approx 40%.

Software Engineer Intern

JP Morgan Chase

Remote

05/2021 - 07/2021

Devised visually appealing & user-friendly data displays for traders by integrating with a stock price data feed, leveraging React.js, TypeScript, Python, JavaScript, and HTML/CSS, significantly expediting data analysis.

Skills

Azure | AWS | Java /Spring | C/C++ | React/Angular| Scrum| Jenkins | Python | SQL/MySQL | Git | HTML/CSS| Kotlin| iOS/Swift| JIRA/Agile|JavaScript Machine Learning | Frontend Engineer | Backend Engineer | Full Stack Software Engineer | Cloud Engineer | Electrical Engineer | Embedded

 RESTful API Architecture Development: Engineered a robust RESTful API architecture with Django and Flask frameworks, resulting in a 25% reduction in response time, improved scalability to handle 10,000+ concurrent requests, and enhanced user experience by implementing and designing a secure RESTful authentication system with OAuth 2.0, integrating third-party authentication providers. Migrated a monolithic application to microservices using RESTful APIs, ultimately increasing development agility and improving fault isolation.

SINGLE-CORE and MULTI-CORE SYSTEMS: Designed & implemented a high-speed cache and memory network using request/response network to enable seamless communication between processors, caches, and main memory; integrated a multi-core data cache with 4 cache banks into the memory network, reducing cache access latency by 20%. Optimized a ring network with 4 routers and 4 input/output interfaces, improving data transmission efficiency through 3 queues; connected processors, data caches, and memory to enable data sharing across multiple cores, leading to a 30% boost in system performance. (Verilog, Python, C/C++, Verilog HDL) (10/2021)

FIPEL NED PROCE SOR: Developed & deployed 2 five-stage pipelined microarchitectures, using TinyRV2 & RISC-V ISA, utilizing val/rdy microprotocol, employing stalling and bypassing to prevent hazards, and implementing CSR, Reg-Reg, Reg-Imm, Memory, Jump, and Branch instructions. (Verilog, Python, C/C++, Verilog HDL) (11/2021)

MAZE MAPPING ROBUT: Crafted an award-winning robot by creating and implementing a maze navigation algorithm. Incorporated a dim near-infrared LED (25 kHz) and assembled the robot's physical framework to visually convey its progress to the base station. Engineered its circuitry to display the location of the discovered frequency treasures on a monitor and control the robot's LEDs for color and on/off functionality. (C/C++, Arduino) (01/2022)

SQL GEOCODING ADDRESS PARSING: Developed a geocoding project using the Google Geocoding API to parse free text addresses, resulting in formatted addresses (street, city, state, zip code, country) for enhanced SQL database efficiency. Integrated authentication and access to multiple geocoding services (Google, Bing, Yahoo, MapQuest) using API keys, enabling address validation, real-time mapping, and distance calculations in SQL-based applications. Processeed and normalized 5,625 and 266 in HK significantly improving address data quality for SQL paperations.

and 266 in HK, significantly improving address data quality for SQL operations.

LOCKING CACLE: Assembled Two-way set-associative cache (256 bytes, 16-byte lines) with LRU replacement, achieving 4-cycle hit latency, optimizing latency-insensitive interfaces, init transactions, and eviction responses for data writing without main memory refill. Coded the cache

using **Verilog**, **Python**, **VHDL**, and **C/C++** adhering to best practices for code architecture. (09/2021)

ACADEMIC NAVIGATOR: Transformed academic planning with a data parsing system from the Cornell class roster. Created a user-friendly interface for students to map out their academic journey to generate a comprehensive academic roadmap, including double & triple majors. Automated GPA calculations and class exploration for 100+ classes within specific times & professors, eliminating manual search. (OCaml, OOP)

Mentorship_

Cornell University Engineering: Circuits for Electrical and Computer Engineers (ECE 2100) IEEE- Eta Kappa Nu Tutor (08/2022 - 12/2022) Cornell University: Mechanics & Heat (Phys 1112) & Linear Algebra for Engineers (Math 2940) ELI Peer Tutor (08/2021- 12/2021)

Cornell University: Dean's List (all semesters)
Cornell Engineering: Richard A. Tapia Award for significant leadership in CS (02/2023)
Dublin Jerome High School: President's Education Award for Educational Excellence; Honor/Merit Roll (06/2020)
The CollegeBoard: AP Scholar With Distinction (05/2020)