BASANT KHALIL

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Education

Bachelor of Science, Summa Cum Laude — Cornell University — *Ithaca, NY* — **08/2020 - 06/2023**

- **Double Major** in **Computer Science & Electrical and Computer Engineering**, **GPA: 4.041**

IEEE-Eta Kappa Nu (IEEE-HKN), the International Honor Society of Electrical and Computer Engineering & Tau Beta Pi, the National Engineering Honor Society

High School Honor Diploma — Dublin Jerome High School — *Dublin, OH* — **09/2018 - 06/2020**

- **Valedictorian; Summa Cum Laude; GPA: 5.0**

Professional Experience

Software Engineering Intern: Full Stack — Hewlett Packard Enterprise — *Durham, NC* — **05/2023 - Current**

- Designed & implemented scalable APIs and background workers for managing 1st and 3rd-party proprietary licenses using **.net, Azure**, &AWS.
- Led the development of several products E2E, from identifying system requirements and partner dependencies to workload balancing, software implementation, engineering, testing, and configuring metrics, alarms, monitors, and dashboards.
- Continuous Integration/Deployment Pipeline Integration, pull requests, code reviews, load/stress testing, unit/integration/e2e testing

Undergraduate Research Assistant: Capra — Cornell University — *Ithaca, NY* — **05/2023 - Current**

- **Capra** Research Group. Advised by Adrian Sampson: Streamlined the debugging process for **Calyx** files in VSCode, improving developer productivity by up to 30% by developing and implementing "cider-dap," sub-crate utilizing the **Debug Adapter Protocol (DAP)** to enhance **Calyx compiler** infrastructure using **Rust**, **C++ Python**, **JavaScript, and SystemVerilog**.
- Accelerated identification & resolution of programming errors, achieved an average time savings of 20% during debugging sessions, reduced initialization time by 25%, and enhanced user experience by leveraging "**cider-dap**" to facilitate seamless attachment & startup functionalities.
- Led the optimization & transformation of programs into synthesizable hardware designs within the **Calyx compiler** infrastructure, streamlining processes and improving performance through simplifying high-level semantics encoding, reducing development time by 40%, and enhancing **hardware accelerators**' performance by 15%.

Teaching Assistant — Cornell University — *Ithaca, NY* — **08/2021 - 05/2023**

- For **Analysis of Algorithms (CS 4820)**; **Discrete Structures (CS 2800)**; and **Calculus for Engineers (Math 1910)**.
- Facilitated dynamic discussions&actively supported learning process of 500+ students through personalized guidance during & outside office hours.
- Collaborated closely with faculty members to develop and deliver 50+ engaging instructional materials, including visually appealing presentations, informative handouts, and interactive online resources, effectively enhancing student learning and comprehension.
- Led the successful development and implementation of an advanced **autograder** system, automating the evaluation of coding projects for a class of 450+ students which improved grading accuracy by approx 25% and reduced regrade requests by around 40%.

Software Engineer Intern — JP Morgan Chase — *Remote* — **05/2021 - 07/2021**

- Developed and analyzed data sets by interfacing with a stock price data feed using **Python, Git**, **JavaScript**, **HTML**, **CSS**, and **TypeScript** facilitating effective data analysis.
- Created visually appealing and user-friendly data displays for traders, leveraging **React**.js, **TypeScript**, and web applications to enhance data understanding and analysis.

Skills

- C# | .NET | Java | JavaScript | TypeScript | C++ | C | Node | Verilog | React | Python | SQL | HTML | CSS | VHDL | NoSQL | Rust | Git | Ruby | JSON
- Azure | AWS | Cloud Computing | Eclipse | IntelliJ | JQuery | SystemVerilog | Unit Testing | OOP | Arduino IDE | Game Development | Rest | SOAP
- Machine Learning | Frontend Engineer | Backend Engineer | Full Stack Software Engineer | Cloud Engineer | Electrical Engineer | Embedded Systems

Projects

- **BLOCKING CACHE:** Two-way **set-associative cache** (256 bytes, 16-byte lines) with **LRU** replacement, achieving **4-cycle hit** latency, efficient handling of latency-insensitive interfaces, init transactions, and eviction responses for data writing without main memory refill. Developed the cache using **Verilog**, **Python**, and **C/C++** while following best practices for code architecture. Implemented code reviews to ensure code quality and maintainable & testable code and built reusable components for seamless integration in future projects. (09/2021)
- **SINGLE-CORE and MULTI-CORE SYSTEMS**: Designed & implemented **cache** and **memory network** using request/response network pairs, for communication between **processors**, **caches**, and main **memory** as well as integrated a **multi-core data cache** with **4 cache banks** into the **memory network**. Assembled **4 routers** in a **ring network** with 4 **input/output** interfaces, optimizing data transmission through **3 queues** connecting a processors, data caches, and main memory. Developed, tested & implemented technical front-end solutions within a full-stack environment, utilizing variety of development tools and technologies while writing maintainable and testable code, following industry standards. Constructed reusable components to facilitate future project development. (**Verilog**, **Python**, **C/C++**, **Verilog HDL**) (10/2021)
- **PIPELINED PROCESSOR:** Designed & implemented 2 **five-stage pipelined microarchitectures**, using **TinyRV2** & **RISC-V ISA**, utilizing **val/rdy** microprotocol, employing stalling and bypassing to prevent hazards, and implementing **CSR**, **Reg-Reg**, **Reg-Imm**, **Memory**, **Jump**, and **Branch** instructions. (**Verilog**, **Python**, **C/C++**, **Verilog HDL**) (11/2021)
- **MAZE MAPPING ROBOT:** Developed an award-winning robot by developing a maze navigation algorithm incorporating a high-frequency blinking dim near-infrared **LED** (**25 kHz**) & constructing the robot's physical framework to visually convey its progress to the base station while also engineering circuitry to display the location of discovered treasures on a monitor and control the robot's **LEDs** for color and **on/off** functionality. (**C/C++, Arduino**) (01/2022)
- **ACADEMIC NAVIGATOR:** Developed a powerful, hands-on data parsing system from the **Cornell Class roster**, transforming academic planning. Created a user-friendly interface enabling students to easily map out their educational path by inputting desired majors (even with double majors), generating comprehensive academic roadmaps. Leveraged a robust database of **100**+ classes to provide essential information including schedules, professors, and delivery modes, empowering students to make informed decisions. Automated GPA calculations and streamlined class exploration within specific times, eliminating manual search and ensuring comprehensive coverage. Leveraging direct access to the **Cornell Class roster**, users can effortlessly calculate their **GPA** by entering class names and grades, without additional information. This seamless integration enhances user experience, simplifies academic planning, and saves valuable time and effort. (**OCaml, OOP**) (04/2022)

Mentorship

- **Cornell University Engineering**: Circuits for Electrical and Computer Engineers (ECE 2100) IEEE- **Eta Kappa Nu** Tutor **(08/2022 - 12/2022)**
- **Cornell University :** Mechanics & Heat (Phys 1112) & Linear Algebra for Engineers (Math 2940) ELI Peer Tutor (**08/2021- 12/2021**)

Others

- **Cornell University: Dean's List** (all semesters)
- **Cornell Engineering**: Richard A. Tapia Award for significant leadership in CS (02/2023)
- **Dublin Jerome High School: Engineering**: President's Education Award for Educational Excellence; Honor/Merit Roll (06/2020)
- **The CollegeBoard:** AP Scholar With Distinction (05/2020)