Computer Engineering Dept.
Faculty of Engineering
Cairo University

Computer Architecture Lab #1

You will design a part of **8-bit** ALU that accepts 2 8-bit input values "A" and "B" and provides 8-bit output "F". The ALU has 4-bit selection inputs "S" (S0->3) and "Cin" input. The required part of the ALU provides a total of 12 operations specified in the following table

	S_3	S_2	S_1	S_0	
Part A	0	0	0	0	**Next Time**
	0	0	0	1	
	0	0	1	0	
	0	0	1	1	
Part B	0	1	0	0	F = A and B
	0	1	0	1	F = A or B
	0	1	1	0	F = A Nor B
	0	1	1	1	F = Not A
Part C	1	0	0	0	F=Logic shift right A
	1	0	0	1	F=Rotate right A
	1	0	1	0	F=Rotate right A with Carry
	1	0	1	1	F=Arithmetic shift right A
Part D	1	1	0	0	F=Logic shift left A
	1	1	0	1	F=Rotate left A
	1	1	1	0	F=Rotate left A with Carry
	1	1	1	1	F = 0000

Requirement:

You will design a part of **16-bit** ALU as follows:

1. Write VHDL code for parts B, C and D in 3 separate VHDL files **Each file is named** as "partB", "partC", "partD" respectively.
   a. Part B ports
      i. Input => A, B, S0, S1
      ii. Output => F
   b. Part C ports
      i. Inputs => A, Cin, S0, S1
      ii. Output => F, Cout (the shifted/rotated bit)
   c. Part D ports
      i. Inputs => A, Cin, S0, S1
      ii. Output => F, Cout (the shifted/rotated bit)
2. Compile your Code, the code should be free of errors and warnings
3. Simulate each file using the inputs stated below.
4. **Assignment:** Integrate all 3 files in a bigger file, named "ALU", in structural way and use 4-bit "S" selection input to choose between components.
5. Your simulation will be delivered using **DO files** only.

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Operation	A	B	Cin	F	Cout
AND	F5	AA		A0	
OR	F5	AA		FF	
NOR	F5	AA		00	
NOT	F5		_	0A	
F=Logic shift right A	F5		_	7A	1
F=Rotate right A	F5		_	FA	1
F=Rotate right A with Carry	F5		0	7A	1
F=Rotate right A with Carry	F5		1	FA	1
F=Arithmetic shift right A	F5		_	FA	1
F=Logic shift left A	F5		_	EA	1
F=Rotate left A	F5		_	EB	1
F=Rotate left A with Carry	F5		0	EA	1
F=Rotate left A with Carry	F5		1	EB	1
F=0000	F5		_	0000	0
F=Rotate right A	7A		_	3D	0

N.B. you will be graded for code neatness and understanding, Good luck

Self-assessment

1. How to describe wires in VHDL?
2. What hardware does the when else statement maps to?
3. Is VHDL case sensitive?

Questions for Next Lab:

1. If you need to use several sizes of the same component (i.e. 2-bit adder, 4-adder), is there a way to use the same entity definition for all sizes without creating single entity for each size?
2. What is a process?
3. Draw a schematic for full adder.