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Tool Version : Vivado v.2015.2 (win64) Build 1266856 Fri Jun 26 16:35:25 MDT 2015
Date : Tue Jun 09 21:59:59 2020
Host : LAPTOP-6P8OO3DF running 64-bit major release (build 9200)
Command : report_utilization -file Softmax_Layer_utilization_synth.rpt -pb Softmax_Layer_utilization_synth.pb
Design : Softmax_Layer
Device : xc7a200t
Design State : Synthesized
Utilization Design Information
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1. Slice Logic

```
+-----+
| Site Type | Used | Fixed | Available | Util% |
+-----+
| Slice LUTs* | 134257 | 0 | 134600 | 99.75 |
| LUT as Logic | 134257 | 0 | 134600 | 99.75 |
| LUT as Memory | 0 | 0 | 46200 | 0.00 |
| Slice Registers | 288 | 0 | 269200 | 0.11 |
| Register as Flip Flop | 0 | 0 | 269200 | 0.00 |
| Register as Latch | 288 | 0 | 269200 | 0.11 |
| F7 Muxes | 20 | 0 | 67300 | 0.03 |
| F8 Muxes | 0 | 0 | 33650 | 0.00 |
```

1.1 Summary of Registers by Type

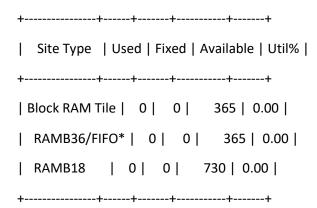
+-----+

| Total | Clock Enable | Synchronous | Asynchronous |

+----+

^{*} Warning! The Final LUT count, after physical optimizations and full implementation, is typically lower. Run opt_design after synthesis, if not already completed, for a more realistic count.

2. Memory



^{*} Note: Each Block RAM Tile only has one FIFO logic available and therefore can accommodate only one FIFO36E1 or one FIFO18E1. However, if a FIFO18E1 occupies a Block RAM Tile, that tile can still accommodate a RAMB18E1

3. DSP

+-----+

| Site Type | Used | Fixed | Available | Util% |

+-----+

| DSPs | 690 | 0 | 740 | 93.24 |

4. IO and GT Specific

+----+ | Site Type | Used | Fixed | Available | Util% | | Bonded IPADs | 0 | 0 | 26 | 0.00 | | Bonded OPADs | 0 | 0 | 16 | 0.00 | | PHY_CONTROL | 0 | 0 | 10 | 0.00 | | PHASER_OUT/PHASER_OUT_PHY | 0 | 0 | 40 | 0.00 | | OLOGIC | 0 | 0 | 400 | 0.00 | +----+

```
+-----+
| Site Type | Used | Fixed | Available | Util% |
+-----+
| BUFGCTRL | 9 | 0 | 32 | 28.13 |
| BUFIO | 0 | 0 | 40 | 0.00 |
| MMCME2_ADV | 0 | 0 | 10 | 0.00 |
| PLLE2_ADV | 0 | 0 | 10 | 0.00 |
| BUFMRCE | 0 | 0 | 20 | 0.00 |
| BUFHCE | 0 | 0 | 120 | 0.00 |
| BUFR | 0 | 0 | 40 | 0.00 |
```

6. Specific Feature

```
+-----+
| Site Type | Used | Fixed | Available | Util% |
+-----+
| BSCANE2 | 0 | 0 | 4 | 0.00 |
| CAPTUREE2 | 0 | 0 | 1 | 0.00 |
| DNA_PORT | 0 | 0 | 1 | 0.00 |
| EFUSE_USR | 0 | 0 | 1 | 0.00 |
| FRAME_ECCE2 | 0 | 0 | 1 | 0.00 |
| ICAPE2 | 0 | 0 | 2 | 0.00 |
| PCIE_2_1 | 0 | 0 | 1 | 0.00 |
```

7. Primitives

+-----+

| Ref Name | Used | Functional Category |

+----+

| LUT6 | 45594 | LUT |

| LUT5 | 41087 | LUT |

| LUT2 | 26473 | LUT |

| LUT3 | 20853 | LUT |

| LUT4 | 20678 | LUT |

| CARRY4 | 10862 | CarryLogic |

| LUT1 | 2380 | LUT |

| DSP48E1 | 690 | Block Arithmetic |

| OBUF | 352 | IO |

| IBUF | 320 | IO |

| LDCE | 288 | Flop & Latch |

| MUXF7 | 20 | MuxFx |

| BUFG | 9 | Clock |

+-----+

8. Black Boxes
