ELECTRONIC PRINCIPLES AND DEVICES

Department of Electronics and Communication Engineering

ELECTRONIC PRINCIPLES AND DEVICES

TRANSISTORS

BJT (Bipolar Junction Transistor)

Department of Electronics and Communication.

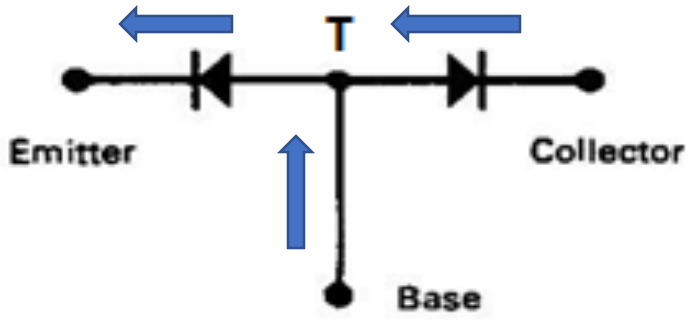
➢A **bipolar junction transistor (BJT)** is a ***three terminal device*** consisting of either a p-type semiconductor or n-type semiconductor sandwiched between opposite types .It has **two p–n junctions** connected back-to-back.

➢In a BJT, the operation depends on the active participation of both the **majority carriers**, and the **minority carriers**; hence the name **"bipolar"**.

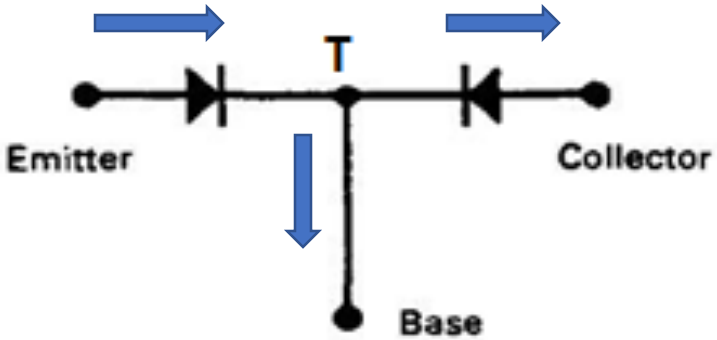
➢The combination of two terms ***transfer + resistor*** results in **TRANSISTOR** as the current is transferred from a low to a high-resistance circuit.

BJT Transistor: Construction

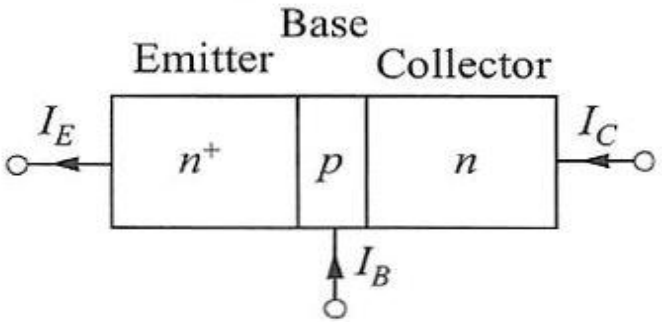
➢The three terminals of a Bipolar junction transistor are Emitter, Base & Collector.

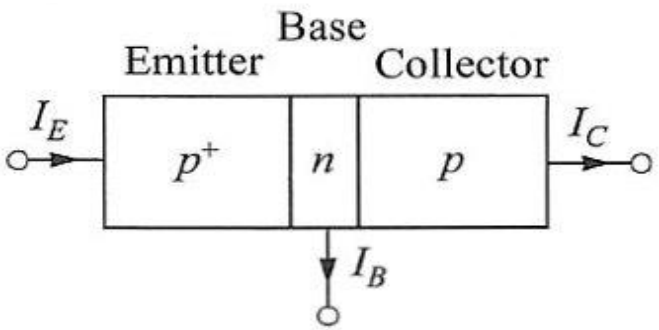


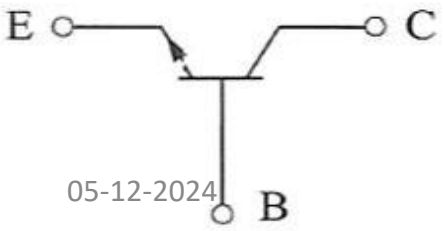
n-p-n

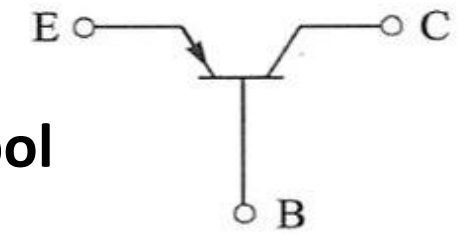


p-n-p

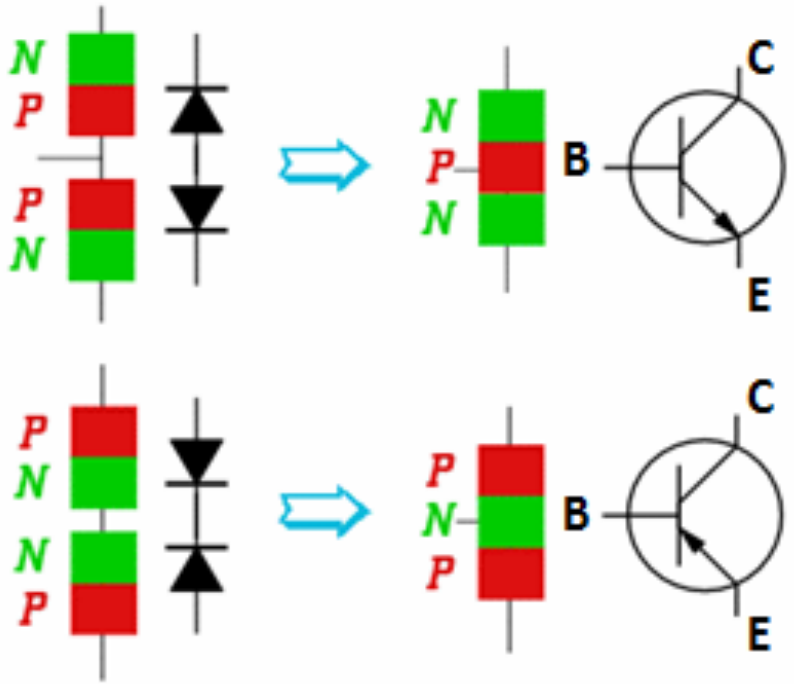








Transistor Symbol



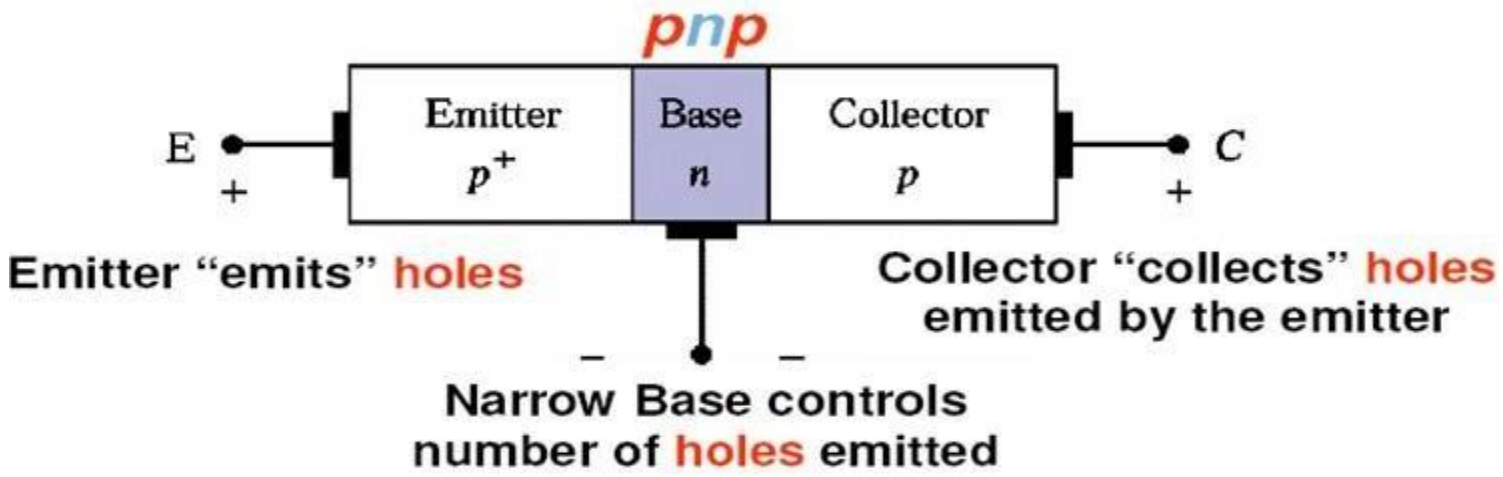
➢The **Emitter (E)** is the portion of the transistor that **supplies** charge carriers (either electrons or holes) and it is a **heavily doped** region. The area is moderate in size.

➢The **Base (B)** is the **middle** portion of the transistor that forms **two PN junction** between the emitter and the collector and it is a **lightly doped** region. It is the smallest in width of all the three regions.

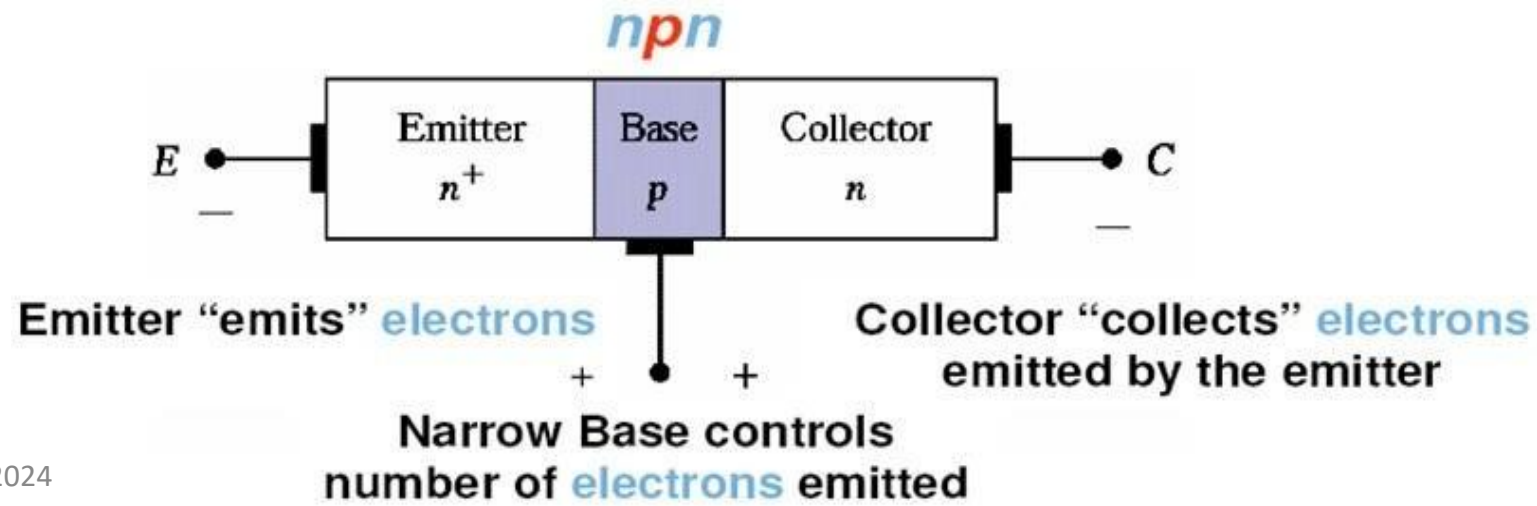
➢The **Collector (C)** is the portion of the transistor that **collects** charge carriers (either electrons or holes) and it is a **moderately doped** region. It is the widest of all the three regions as maximum heat is dissipated in this region.

Types of BJTs

1. pnp transistor:



2. npn transistor:

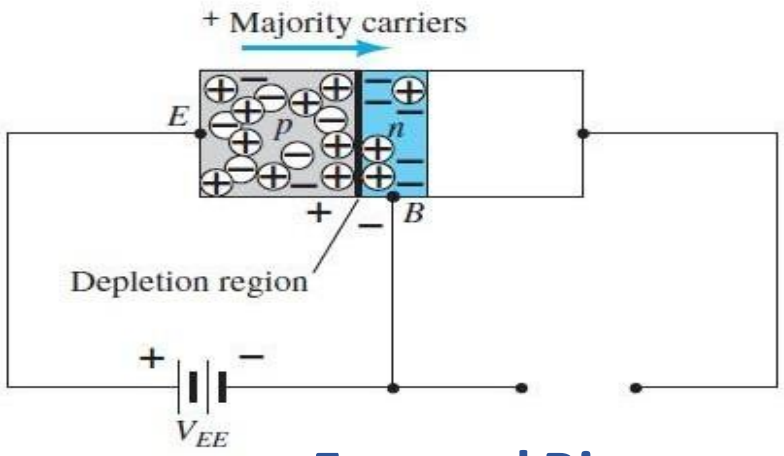


BJT Operation

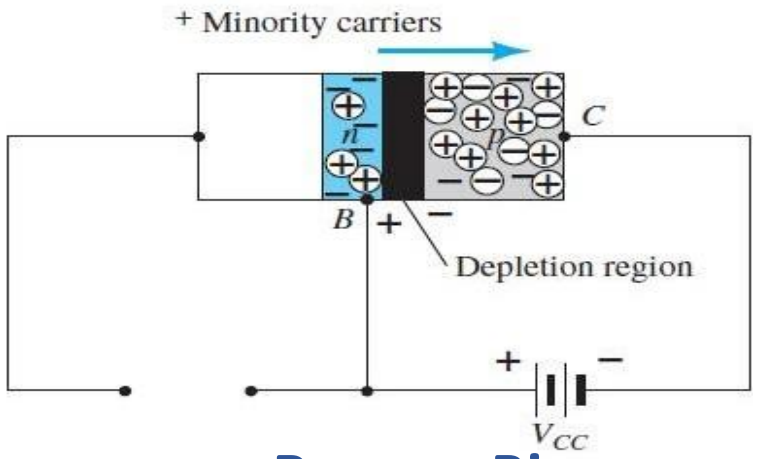
The transistor operated in **Common Base** configuration, with the external sources, **VEE** and **Vcc**, connected as shown:

- The emitter – base junction is **forward biased**
- The collector – base junction is **reverse biased**

- **As the EB junction is forward biased the current flow is because of majority charge carriers.**
- **Similarly as the CB junction is reverse biased the current flow is because of minority charge carriers (Hence wider depletion region)**



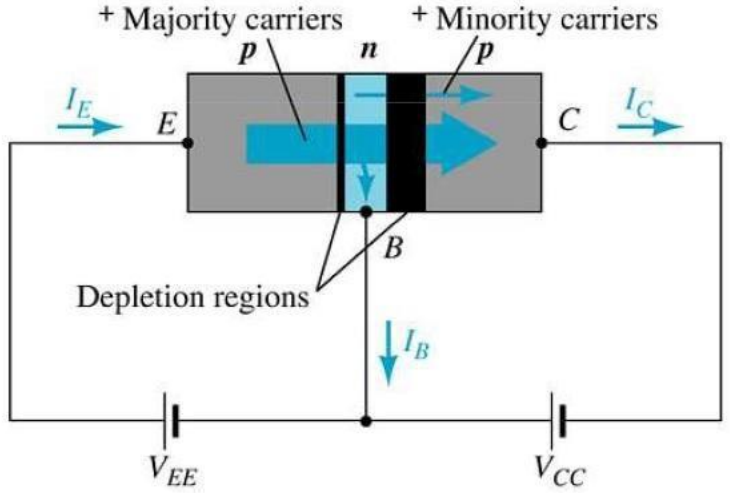
Forward Bias



Reverse Bias

BJT Operation

- A large number of majority carriers will diffuse across the forward biased p–n junction into the n -type material.
- Since the n -type material is very thin and lightly doped, a very small number of these (holes) will recombine with the electrons in base region and flow through the base terminal as base current (is typically in the order of microamperes).
- Thus, a larger number of these majority carriers from the emitter region will diffuse across the reverse-biased junction into the p -type material connected to the collector terminal.



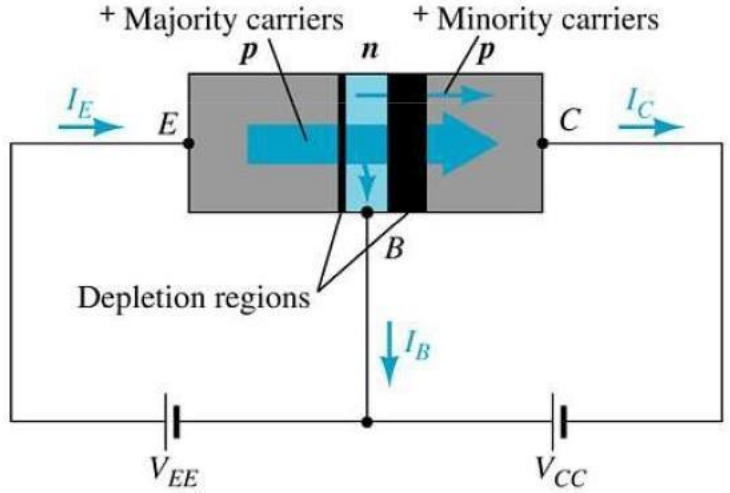
Currents in a BJT

- Applying KCL to the transistor, we get

$$I_E = I_C + I_B$$

- The collector current, comprises two components—the majority and the minority carriers.
- The minority-current is called as leakage current (I_{CO} - I_C with emitter terminal Open).
- Therefore the total collector current is given as

$$I_C = I_{C_{\text{majority}}} + I_{CO_{\text{minority}}}$$



Currents in a BJT

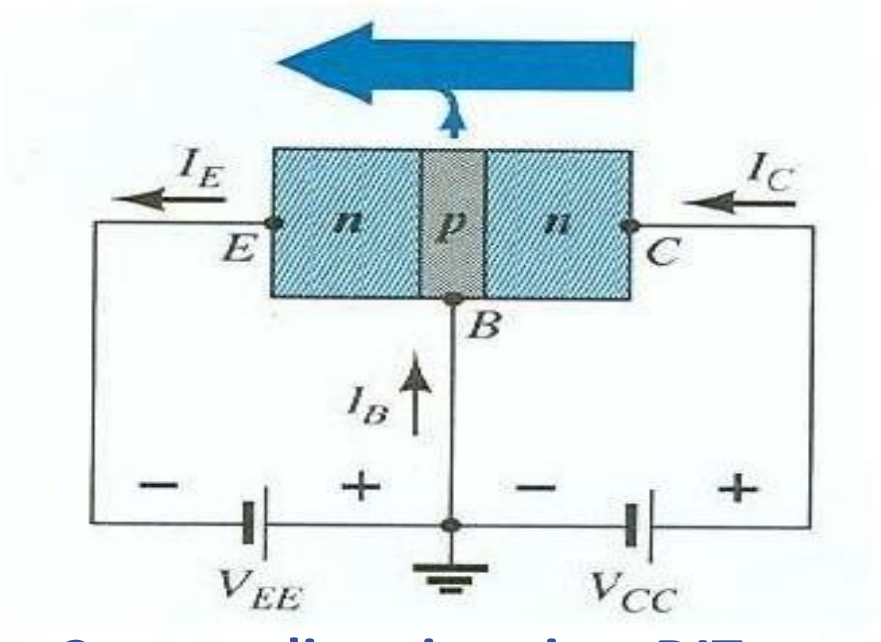
Currents in a transistor

- Emitter current is the sum of the collector and base currents:

$$I_E = I_C + I_B$$

- The collector current is comprised of two currents:

$$I_C = I_{C\,(Majority)} + I_{CO\,(Minority)}$$



Current directions in a BJT

BJT Biasing and Modes of operation

A Transistor has two p-n junctions.

1) Emitter-base (EB) Junction
2) Collector-base (CB) Junction

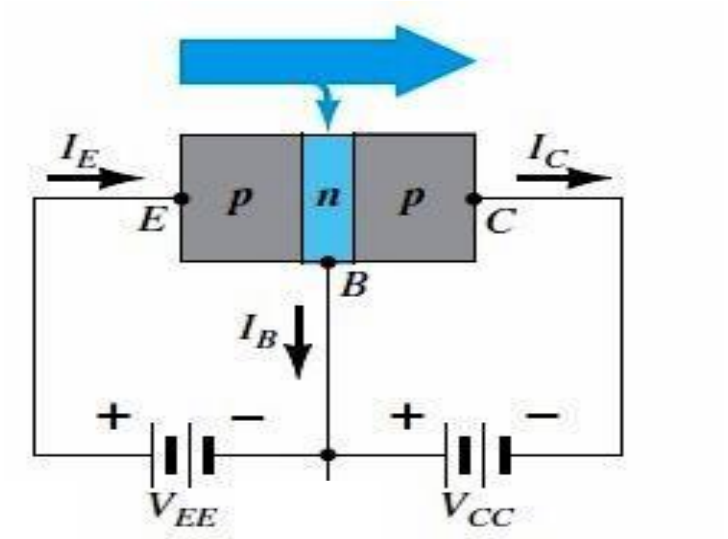
- Each junction can either be **forward or reverse biased** independently.
- Depending on the bias we have the following regions of operation of BJT

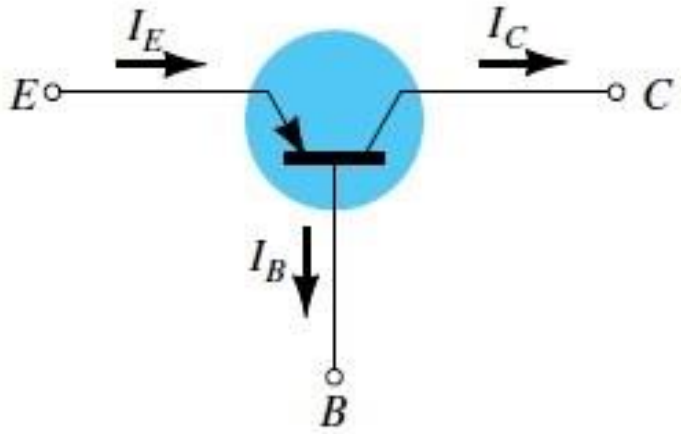
Regions of Operation	Emitter base Junction	Collector-base Junction	Application
Active region(*commonly used*)	Forward biased	Reverse biased	Transistor works as an Amplifier
Saturation region	Forward biased	Forward biased	Transistor works as a switch (ON)– Digital Application
Cut-off region	Reverse biased	Reverse biased	Transistor works as a switch (OFF)– Digital Application
Inverse active region(rarely used)	Reverse biased	Forward biased	Transistor works as an Attenuator

Common Base Configuration

➢The arrow in the diagram, indicates the direction of the emitter current and matching the letters *pnp* of the transistor type and with the appropriate letters of the phrases "*pointing in permanently*"

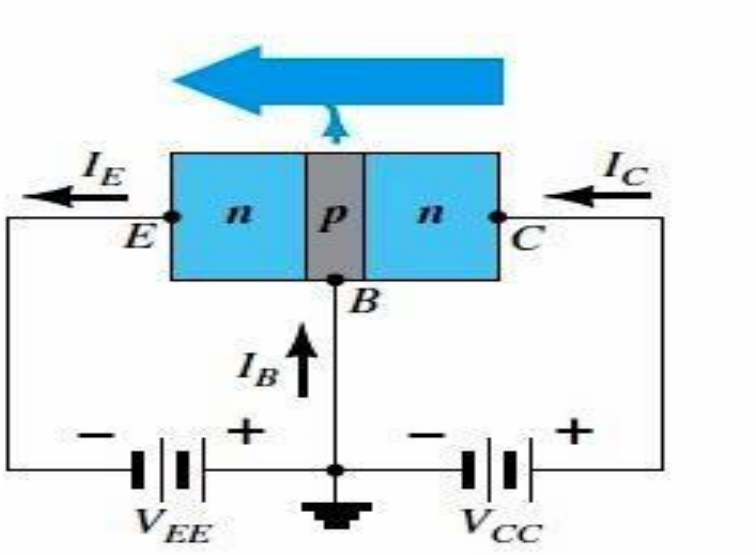
➢The ***PNP*** BJT requires two voltage sources **V_{EE}** and **V_{CC}** to bias the two junctions respectively.

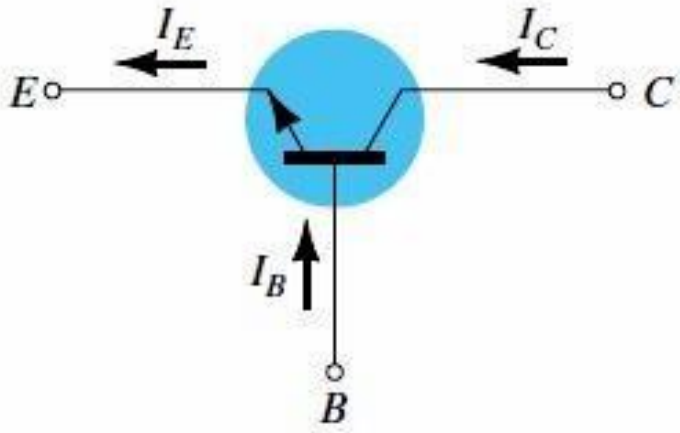




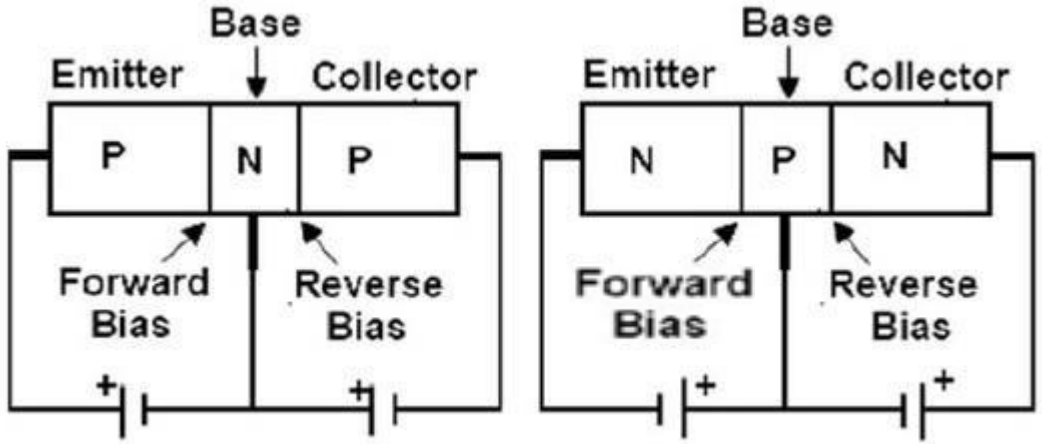
Common Base Configuration

- The arrow in the diagram indicates the direction of the emitter current.
- Easy way to remember matching the letters *npn* of the transistor type and with the appropriate letters of the phrases "*not pointing in*"
- The ***NPN*** transistor requires two voltage sources **V_{EE}** and **V_{CC}** to bias the two junctions respectively.





V_{BE} **V_{CB}**



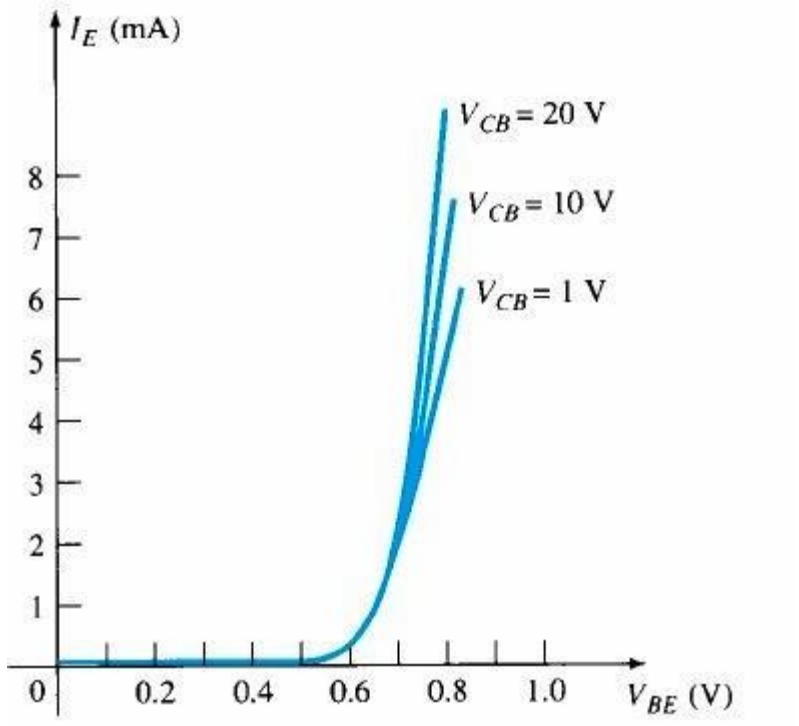
The biasing of ***PNP*** and ***NPN*** transistors to operate in active region

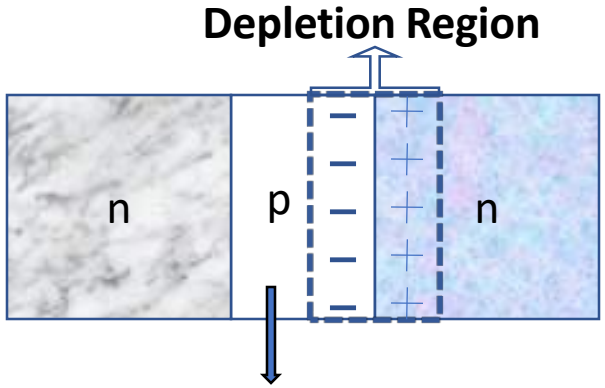
➢Since the analogy of transistor is two diodes connected back-to-back. One diode is ***forward biased*** and the other is ***reverse biased*** for the device to operate in **active region**.

➢Hence, biasing the ***emitter base junction (EB Jn)*** in forward bias condition and ***collector base junction (CB Jn)*** in reverse bias condition, gives the input characteristic of the device.

CB - Input Characteristics

For the transistor in CB configuration, when the output voltage V_{CB} is increased, it causes an ***increase*** in the emitter current and hence the graph **shifts inwards or towards the left**.





Narrower Base width
(Less chances of recombination)

Base Width Modulation

The input characteristic of BJT (Si) for varying output voltage V_{CB}

Base Width Modulation or Early Effect :

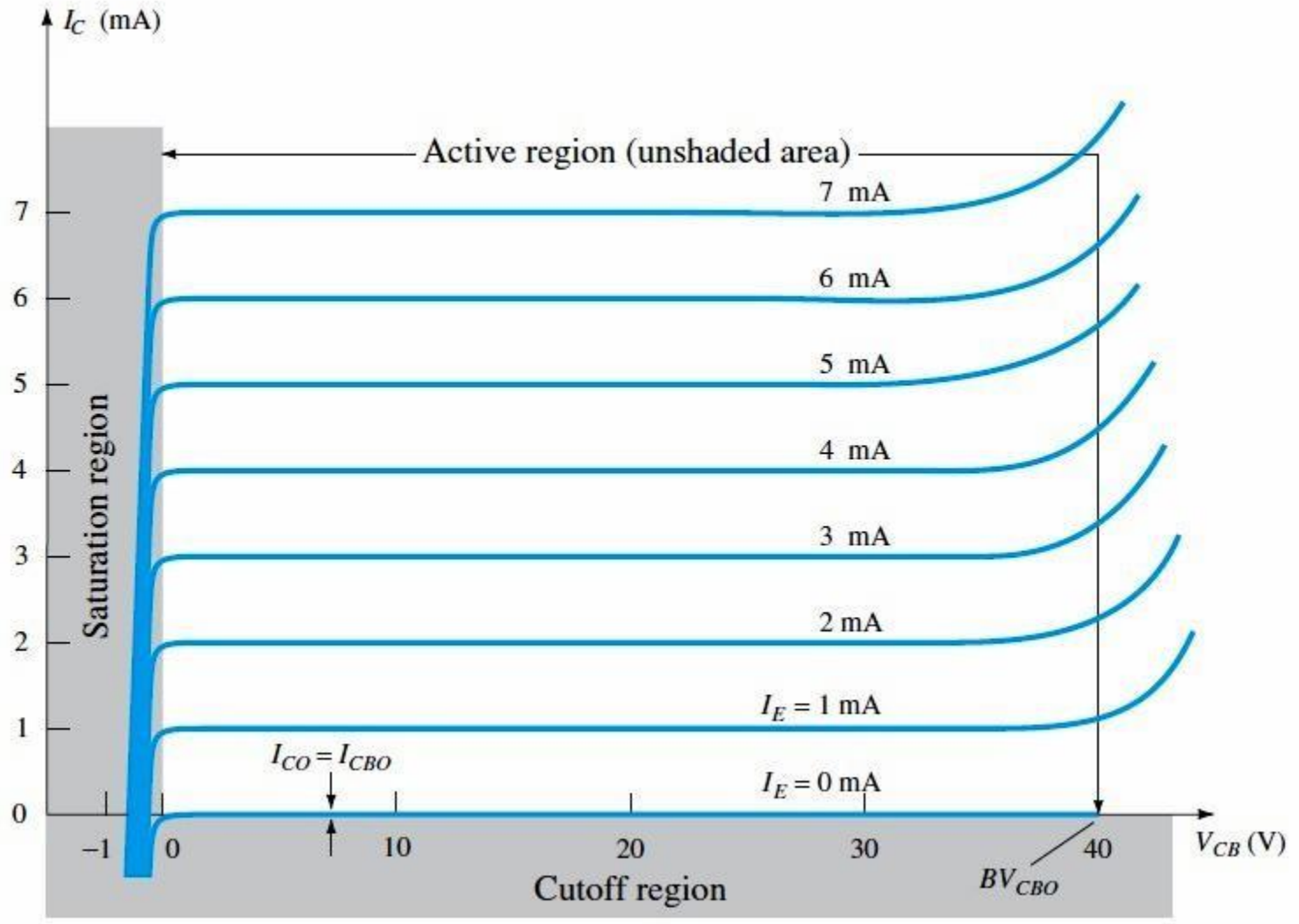
- A greater reverse bias across the collector- base junction increases the collector-base depletion width. There is a variation in the width of the base in a bipolar transistor due to a variation in the applied base-to-collector voltage.

- Base-narrowing has two consequences that affect the current:
  - There is a lesser chance for recombination within the "smaller" base region.
  - The charge gradient is increased across the base, and consequently, the current of minority carriers injected across the collector-base junction increases.

- The Early effect is observed as an increase in the collector or "output" current with increasing collector-emitter voltage.

Electronic Principles and Devices

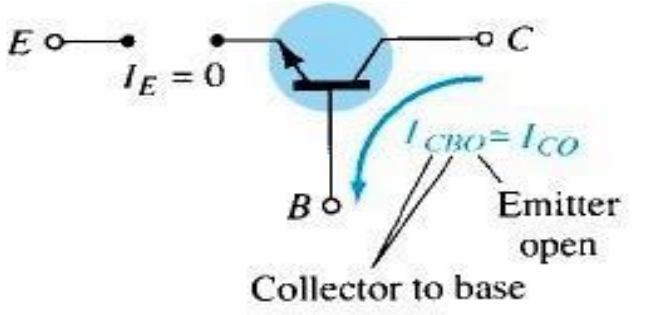
CB - Output Characteristics



The output characteristic of BJT (Si) for varying input current I_E

➢**Active region**: The operating range of the amplifier. It is noticed that I_E is approximately equal to I_C ($I_E \approx I_C$). **BJT** is a current controlled device in the active region and is independent of the output voltage V_{CB}

➢**Cut-off region**: The region where the collector current I_C is approximately equal to 0 ($I_C < I_{CBO}$). The device is basically **OFF** i.e., there's no input voltage, but only reverse – bias output voltage and negligible reverse saturation current



Reverse saturation current

➢**Saturation region**: The region to the left of $V_{CB} = 0V$. Note the exponential increase in collector current I_C as V_{CB} approaches 0V. In this region, I_C depends on V_{CB} but is independent of I_E

CB Configuration - Approximations

- **Emitter and collector current**: $I_E \approx I_C$.
- **Base – emitter voltage (V_{BE})**: $V_{BE} = 0.7V$ (Si).

Alpha (α): Ratio of I_C to I_E.

$$\alpha_{dc} = \frac{I_C}{I_E}$$

$$I_C = \alpha I_E + I_{CBO}$$

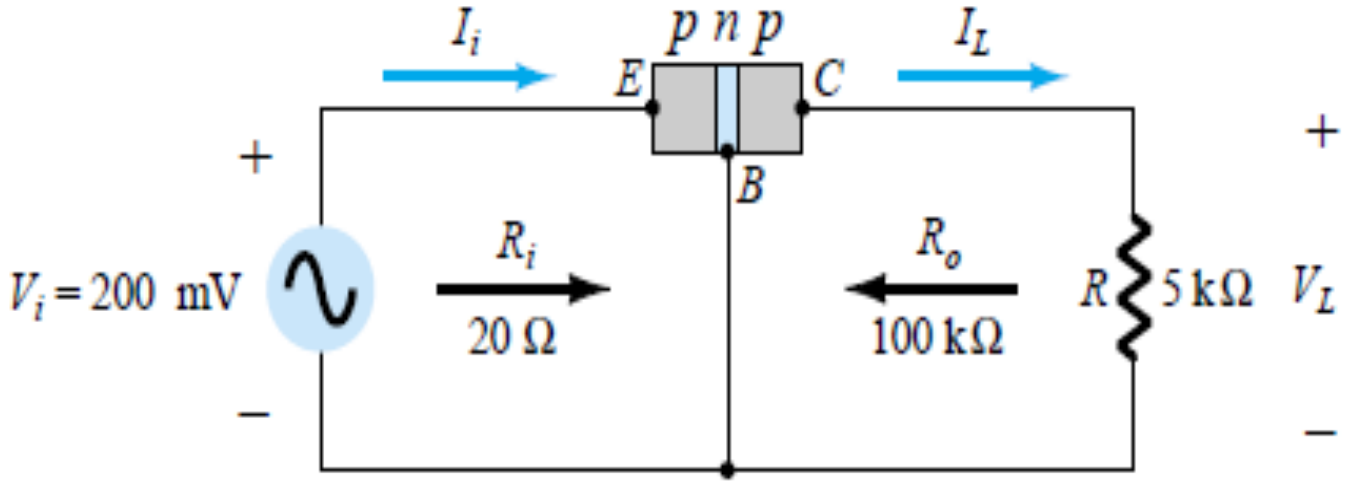
Ideally: α = 1
In reality: α is between 0.9 and 0.998

For AC mode:

$$\alpha_{ac} = \left.\frac{\Delta I_C}{\Delta I_E}\right|_{V_{CB}=\text{constant}}$$

α - Current amplification factor or current gain in CB config.

Common Base Amplifying action



$$I_i = \frac{V_i}{R_i} = \frac{200\text{ mV}}{20\ \Omega} = \mathbf{10\ mA}$$

If we assume for the moment that $\alpha_{ac} = 1$ ($I_c = I_e$),

$$I_L = I_i = 10\text{ mA}$$

and

$$V_L = I_L R$$
$$= (10\text{ mA})(5\text{ k}\Omega)$$
$$= \mathbf{50\ V}$$

The voltage amplification is

$$A_v = \frac{V_L}{V_i} = \frac{50\text{ V}}{200\text{ mV}} = \mathbf{250}$$

Numericals

1. A common base transistor amplifier has an input resistance of 20 Ω and output resistance of 100 kΩ. The collector load is 1 kΩ. If a signal of 500 mV is applied between emitter and base, find the voltage amplification. Assume α_{ac} to be nearly one.

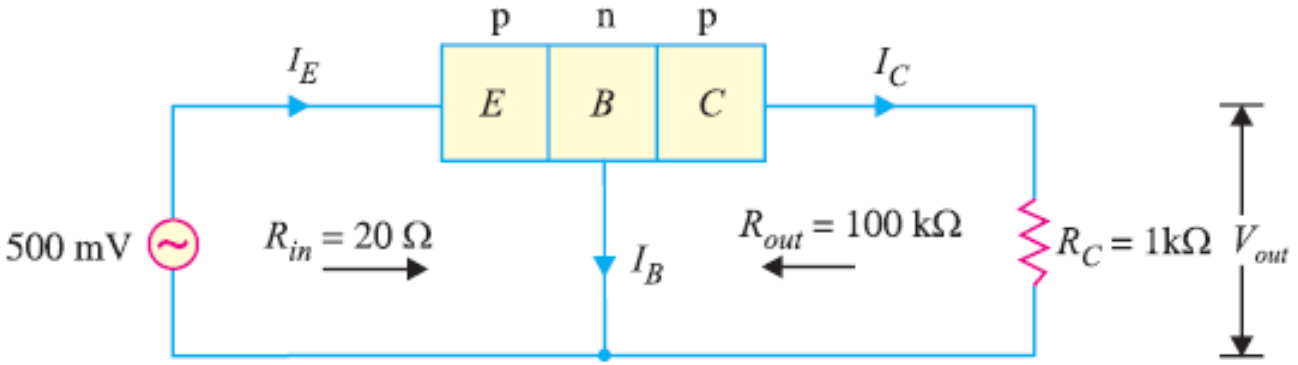


Fig. 1

Input current, $I_E = \frac{\text{Signal}}{R_{in}} = \frac{500\text{ mV}}{20\ \Omega} = 25$ mA. Since α_{ac} is nearly 1, output current, $I_C = I_E = 25$ mA.

$$\text{Output voltage, } V_{out} = I_C R_C = 25\text{ mA} \times 1\text{ k}\Omega = 25\text{ V}$$

$$\therefore \quad \text{Voltage amplification, } A_v = \frac{V_{out}}{\text{signal}} = \frac{25\,V}{500\,mV} = 50$$

2. In a common base connection, I_E = 1mA, I_C = 0.95mA. Calculate the value of I_B .

Using the relation, $I_E = I_B + I_C$

$1 = I_B + 0.95$

$I_B = 1 - 0.95 = \mathbf{0.05\ mA}$

3. In a common base connection, current amplification factor is 0.9. If the emitter current is 1mA, determine the value of base current.

Here, $\alpha = 0.9, \quad I_E = 1\ \text{mA}$

Now $\alpha = \dfrac{I_C}{I_E}$

or $I_C = \alpha I_E = 0.9 \times 1 = 0.9\ \text{mA}$

Also $I_E = I_B + I_C$

$\therefore$ Base current, $I_B = I_E - I_C = 1 - 0.9 = \mathbf{0.1\ mA}$

Numericals

4. In a common base connection, I_C = 0.95 mA and I_B = 0.05 mA. Find the value of α.

$$\text{We know } I_E = I_B + I_C = 0.05 + 0.95 = 1 \text{ mA}$$

$$\therefore \quad \text{Current amplification factor, } \alpha = \frac{I_C}{I_E} = \frac{0.95}{1} = \mathbf{0.95}$$

5. In a common base connection, the emitter current is 1mA. If the emitter circuit is open, the collector current is 50 µA. Find the total collector current. Given that α = 0.92.

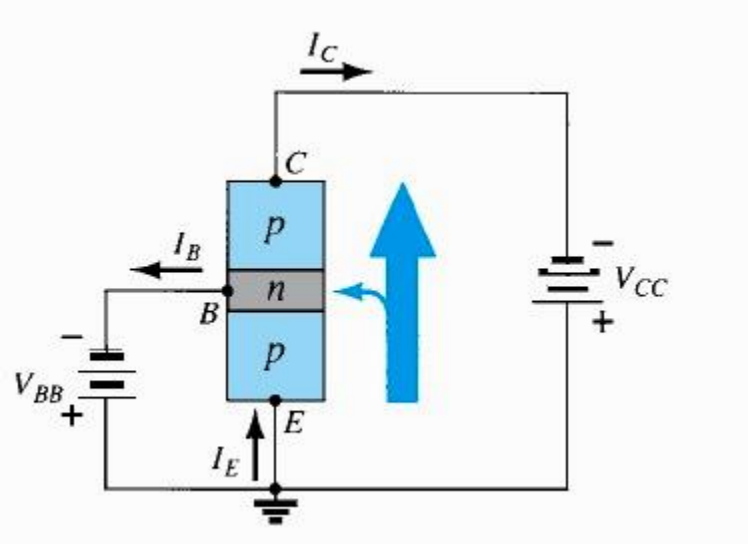
$$\text{Here, } I_E = 1 \text{ mA}, \alpha = 0.92, \quad I_{CBO} = 50 \text{ µA}$$

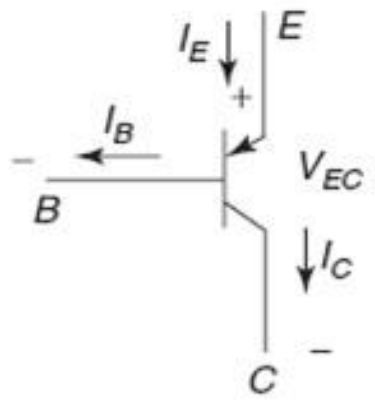
$$\therefore \quad \text{Total collector current, } I_C = \alpha I_E + I_{CBO} = 0.92 \times 1 + 50 \times 10^{-3}$$

$$= 0.92 + 0.05 = \mathbf{0.97 \text{ mA}}$$

➢The **arrow** in the diagram, indicates the direction of the emitter current and we can observe that the ***direction*** of the current in this type of transistor is **opposite** to that of a NPN transistor.

➢The ***PNP*** BJT requires two voltage sources **V_{BB}** and **V_{CC}** to bias the two junctions respectively.

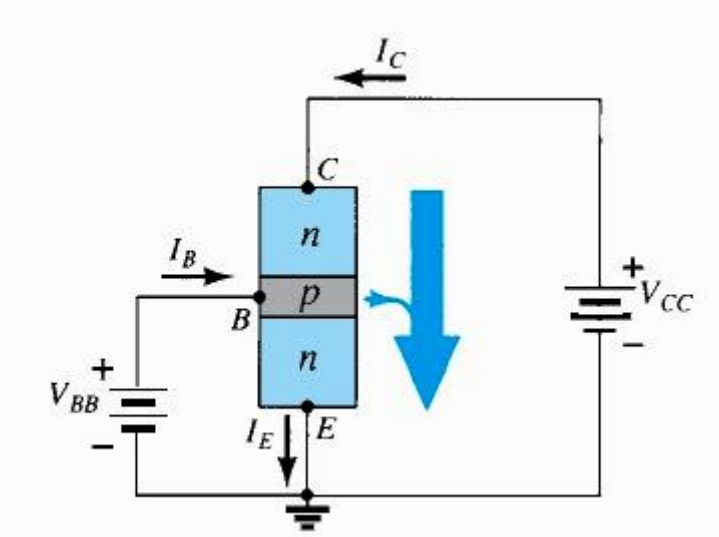


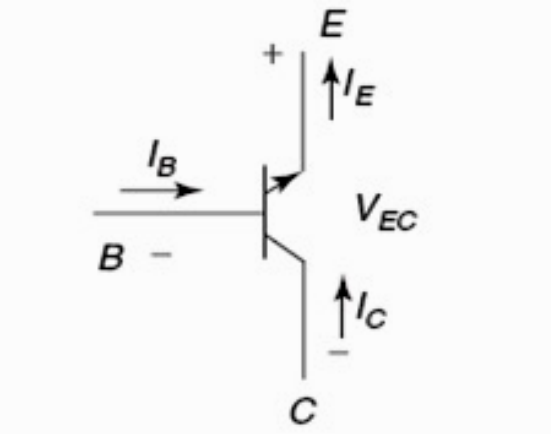


A ***PNP*** transistor used in Common Emitter (CE) configuration

➢The **arrow** in the diagram, indicates the direction of the emitter current.

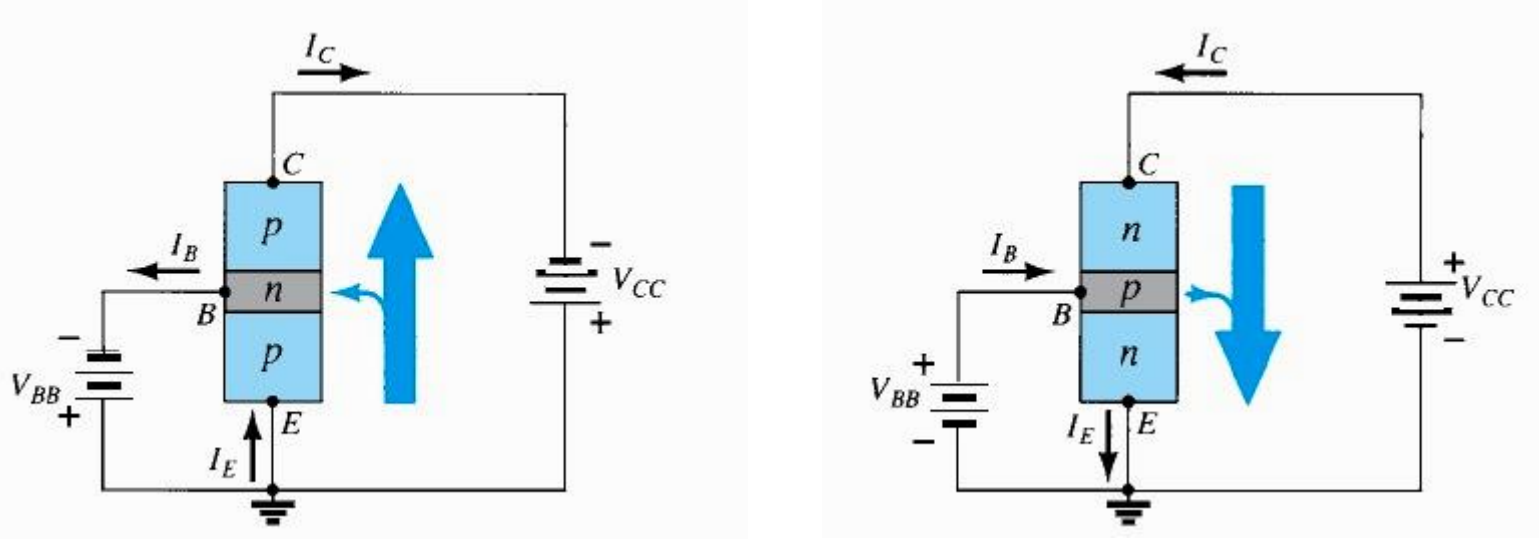
➢The ***NPN*** BJT requires two voltage sources $\mathbf{V_{BB}}$ and $\mathbf{V_{CC}}$ to bias the two junctions respectively.





An ***NPN*** transistor used in Common Emitter (CE) configuration

Common Emitter Configuration



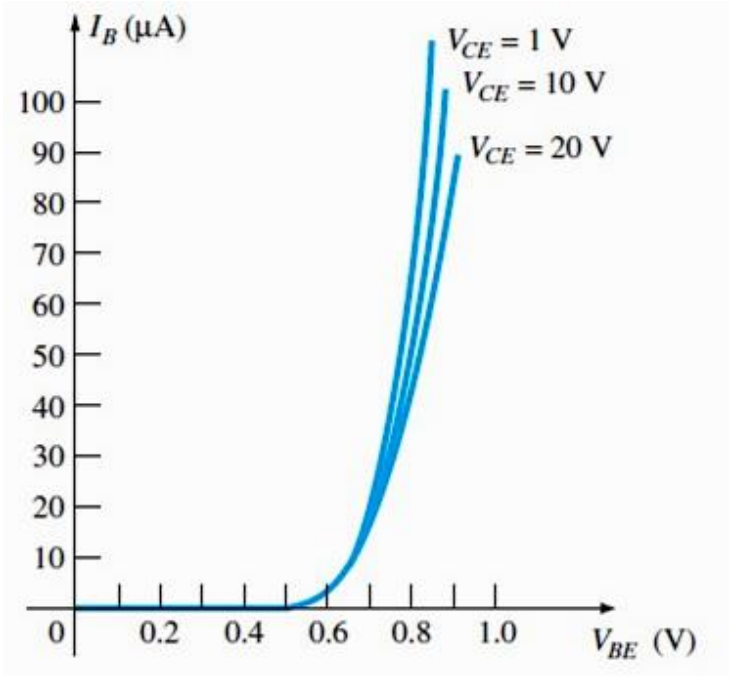
The biasing of ***PNP*** and ***NPN*** transistor to operate in active region

- The analogy of a BJT is two diodes connected back-to-back. One diode is ***forward biased*** and the other is ***reverse biased*** for the device to operate in **active region**.

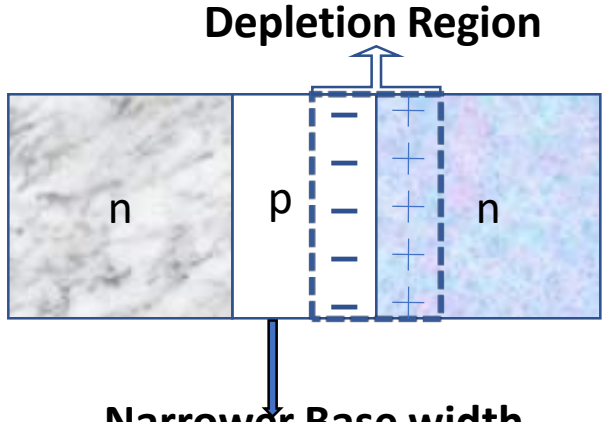
- Hence, biasing the ***emitter base junction (EB Jn)*** in forward bias condition and ***collector base junction (CB Jn)*** in reverse bias condition, gives the input characteristic of the device.

CE Configuration - Input Characteristics

- For the transistor in CE configuration, I_B is the input current (usually in uA) and V_{BE} is the input voltage. A plot of I_B v/s V_{BE} is called the input characteristics.
- The characteristics resemble the forward bias characteristics of a diode.
- When the output voltage $\mathbf{V_{CE}}$ is increased, this high voltage causes a decrease in the current I_B through the device and hence the graph **shifts towards the right**.



The input characteristic of BJT (Si) for varying output voltage $\mathbf{V_{CE}}$



Narrower Base width
(Less chances of recombination)

Base Width Modulation

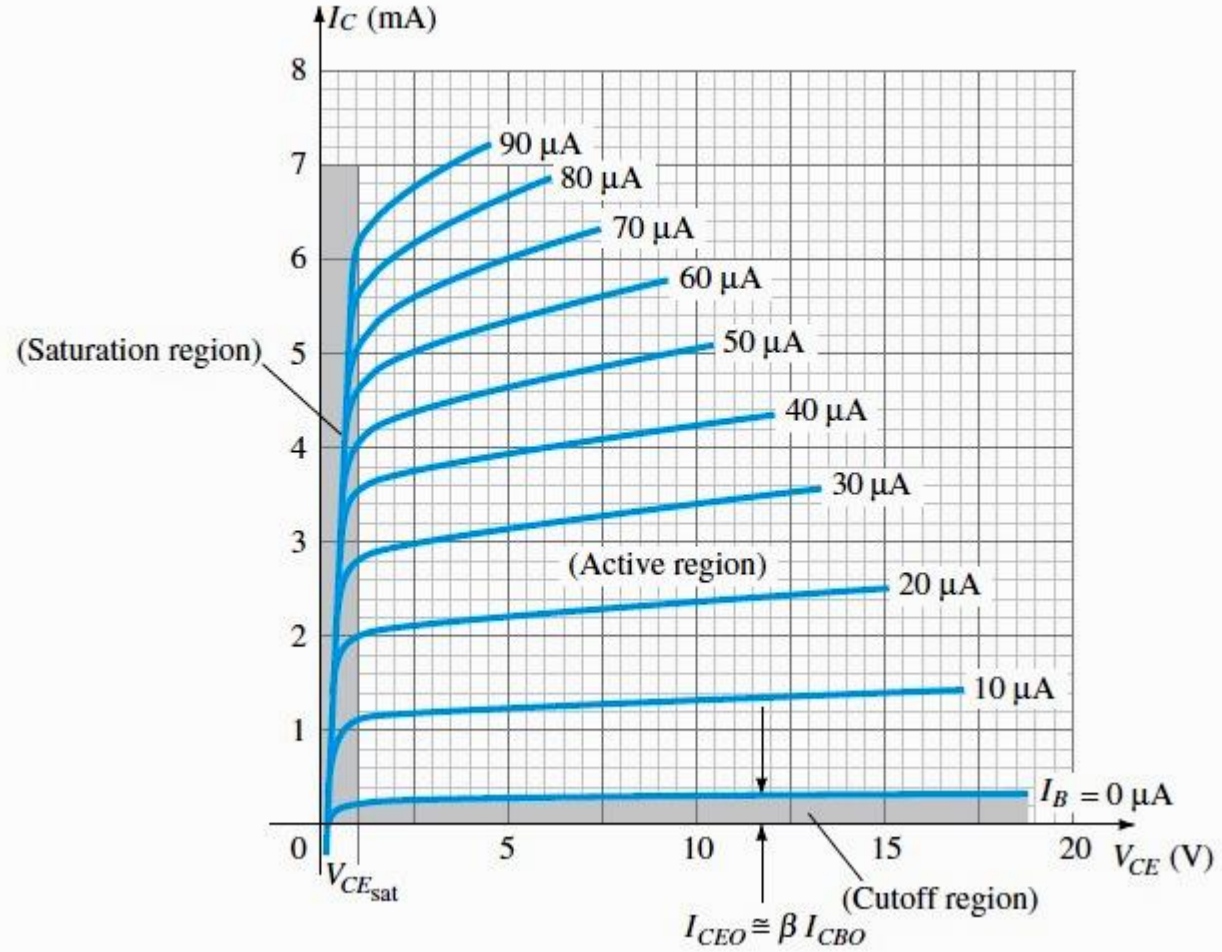
Base Width Modulation or Early Effect :

- A greater reverse bias across the collector- emitter junction increases the base-**emitter** depletion width. There is a variation in the width of the base in a bipolar transistor due to a variation in the applied collector- to-emitter voltage.

- Base-narrowing has two consequences that affect the current:
  - There is a lesser chance for recombination within the "smaller" base region & so I_B decreases further .
  - The charge gradient is increased across the base, and consequently, the current of minority carriers injected across the collector-base junction increases.

- The Early effect is observed as an increase in the collector or "output“ current with increasing collector-emitter voltage.

CE Configuration - Output Characteristics



The output characteristic of BJT (Si) for varying input current I_B

➢ **Active region**: The B-E junction is forward biased. Collector voltage is greater than the base voltage which reverse biases the C-B junction.

$$V_{CE} > V_{BE}$$

In this region, I_C depends on I_E and is almost independent of V_{CE}.

$$Ic = \beta * I_B.$$

➢ **Cut-off region**: Both junctions are ***reverse biased***. No base current. Only a small reverse leakage current between C and E. For practical purposes, current is assumed to be zero.

➢ **Saturation region:** The E-B and C-B junctions are forward biased.
Ic varies with V_{CE} and is ***independent*** of I_B and β.

Relationship between α and β

A relationship can be developed between α and β using the basic relationships introduced thus far. Using $\beta = I_C / I_B$ we have $I_B = I_C / \beta$, and from $\alpha = I_C / I_E$ we have $I_E = I_C / \alpha$. Substituting into

$$I_E = I_C + I_B$$

$$I_C / \alpha = I_C + I_C / \beta$$

and dividing both sides of the equation by I_C will result in

$$\frac{1}{\alpha} = 1 + \frac{1}{\beta}$$

or

$$\beta = \alpha\beta + \alpha = (\beta + 1)\alpha$$

$$I_C = \beta I_B$$
$$I_E = I_C + I_B$$
$$= \beta I_B + I_B$$
$$I_E = (\beta + 1) I_B$$

so that

$$\alpha = \frac{\beta}{1+\beta} \quad \text{or} \quad \beta = \frac{\alpha}{(1-\alpha)}$$

CE Active region

$$I_C = \alpha I_E + I_{CBO}$$

$$= \alpha (I_C + I_B) + I_{CBO} \qquad (\because I_E = I_C + I_B)$$

$$I_C = \frac{\alpha I_B + I_{CBO}}{1- \alpha}$$

Let $\beta = \frac{\alpha}{(1- \alpha)}$ $\qquad [\ \therefore \frac{1}{(1- \alpha)} = 1+ \beta\ ]$

$$I_C = \beta I_B + (1+ \beta) I_{CBO}$$

$$I_C = \beta I_B + I_{CEO}$$

$(\because I_{CEO} = (1+ \beta) I_{CBO})$

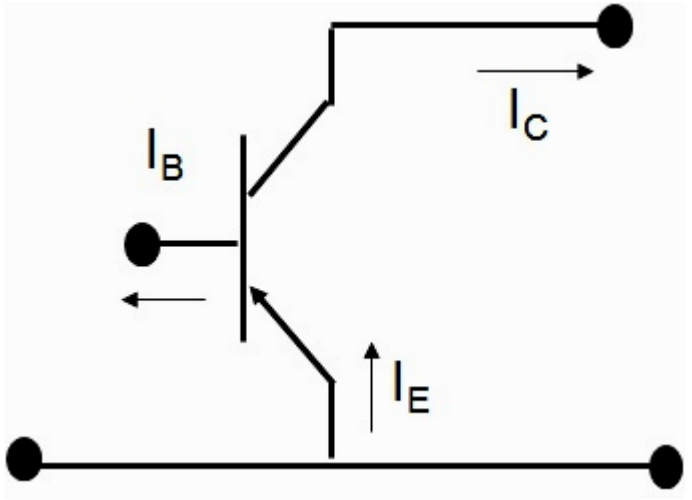
$I_{CEO} \approx \beta I_{CBO}$

or

$I_{CEO} = \left.\frac{I_{CBO}}{1- \alpha}\right|_{I_B = 0\ uA}$

$I_C = \beta I_B$ Neglecting leakage current I_{CEO}

$50 \leq \beta \leq 500$



Numericals

1. Find the value of β if (i) α = 0.9 (ii) α = 0.98 (iii) α = 0.99.

(i) $\alpha = 0.9$

$$\beta = \frac{\alpha}{1-\alpha} = \frac{0.9}{1-0.9} = 9$$

(ii) $\alpha = 0.98$

$$\beta = \frac{\alpha}{1-\alpha} = \frac{0.98}{1-0.98} = 49$$

(iii) $\alpha = 0.99$

$$\beta = \frac{\alpha}{1-\alpha} = \frac{0.99}{1-0.99} = 99$$

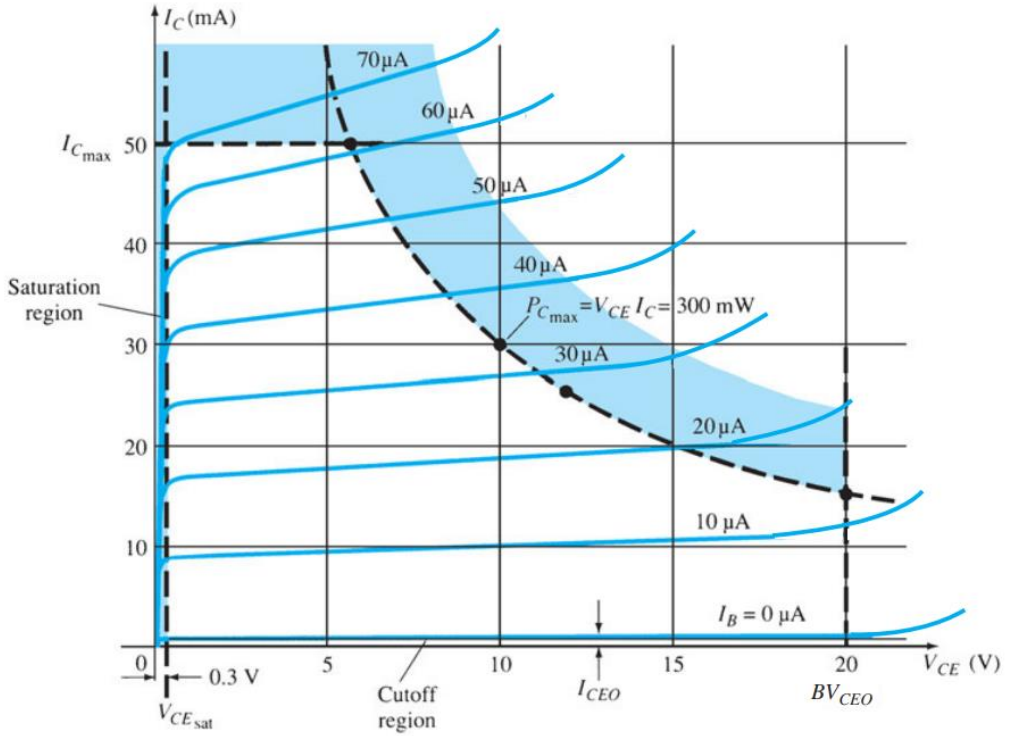
Limits of Operation

The limit of operation ensures that the transistor works within its maximum rating with minimum signal distortion. It is specified in the data sheet.

V_{CESat} : Specifies the minimum V_{CE} that can be applied without transistor going to saturation region.

The maximum power dissipation is given as

$$P_{C_{max}} = V_{CE} I_C$$



Defining the linear (undistorted) region of operation for a transistor.

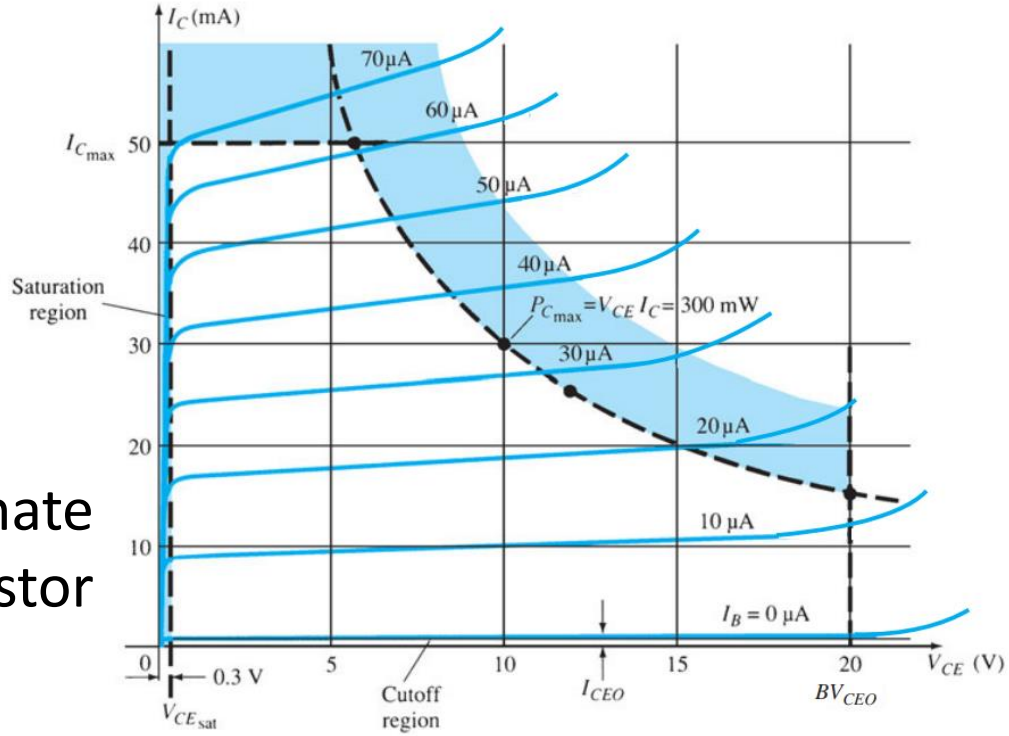
Limits of Operation

For example if,

$$P_{C_{max}} = V_{CE}I_C = 300\ \text{mW}$$

- At $I_C = I_{Cmax}$ i.e, 50 mA, V_{CE} = 6v
- At $V_{CE} = V_{CEmax}$ i.e, 20V, I_C = 15mA
- At $I_C = I_{Cmax}/2$, V_{CE} = 12v

These three points give a rough estimate of the power curve and the transistor must be operated with in this region.



Defining the linear (undistorted) region of operation for a transistor.

Limits of Operation

The cutoff region is the region below $I_C = I_{CEO}$ ($= \beta I_{CBO}$). This region must also be avoided to have minimum distortion .

If the characteristic curve/specification sheet is not available, one must ensure the following conditions are satisfied to ensure minimum distortion.

$$I_{CEO} \leqq I_C \leqq I_{C_{max}}$$
$$V_{CE_{sat}} \leqq V_{CE} \leqq V_{CE_{max}}$$
$$V_{CE} I_C \leqq P_{C_{max}}$$

For CB Characteristics, P_{Cmax} is defined as

$$P_{C_{max}} = V_{CB} I_C$$

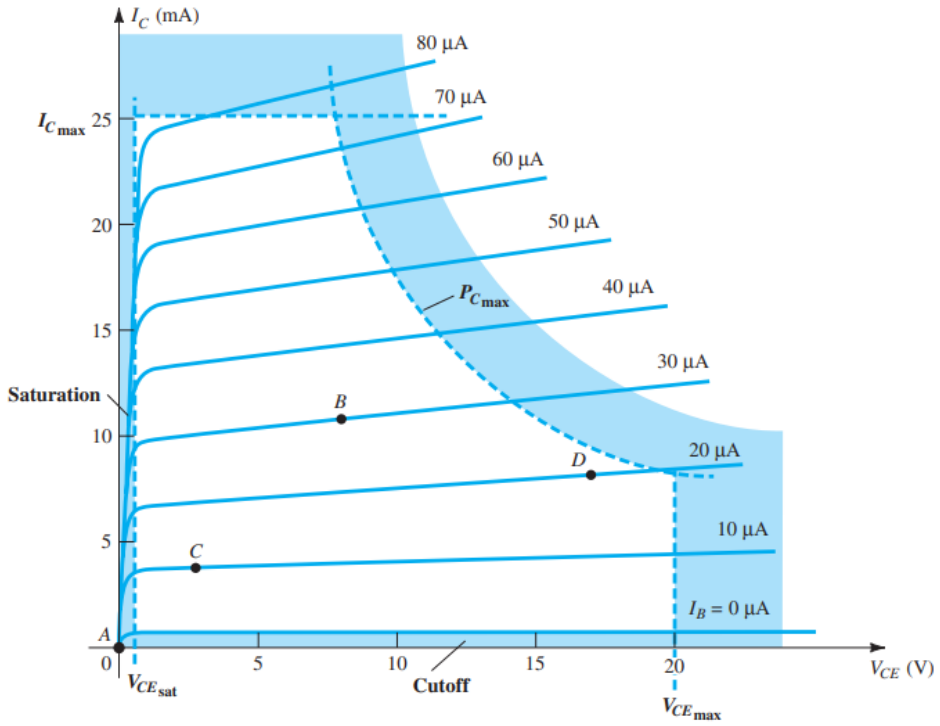
Operating Point

Biasing refers to application of DC voltages to establish a fixed level of current and voltage in a transistor.

For a transistor amplifier, the resulting DC current and voltage on the characteristic curve establish an **Operating Point**. This indicates the region of operation of the transistor.

Since the operating point is **fixed** on the Characteristic curve , it is also called as **Quiescent point** or **Q point**.

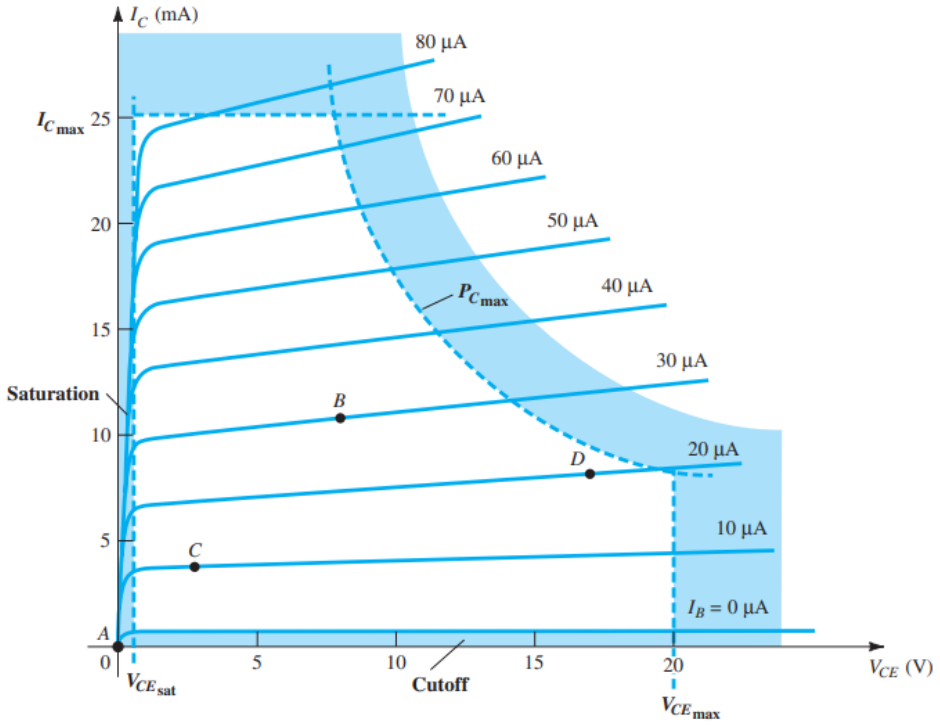
Biasing circuit can be used to set the operating point within the active region. A, B, C, D are some of the possible operating points.



Various operating points within the limits of operation of a transistor.

Operating Point

- **Q Point at A**: If there is no bias, the device is completely off, resulting in Q point at A. This point is not suitable as complete input range can not be covered for amplification.
- **Q Point at B**: can cover a large range of input signal. It is also far from both cut-off and saturation region.
- **Q Point at C**: This is near to both cutoff and saturation region thus limiting the swing of input signal.
- **Q Point at D**: as is near to the maximum voltage and power level, limits the positive swing of input signal



Various operating points within the limits of operation of a transistor.

Operating Point

- Figure 4.1 shows a general output device characteristic with four operating points indicated.

The maximum ratings are indicated on the characteristics of Fig. 4.1 by

- ✓ a horizontal line for the maximum collector current I_{Cmax} and a vertical line at the maximum collector-to-emitter voltage V_{CEmax} .
- ✓ The maximum power constraint is defined by the curve P_{Cmax}.
- ✓ At the lower end of the scales are the cutoff region , defined by I_B=0 mA, and the saturation region , defined by V_{CE} =V_{CEsat} .

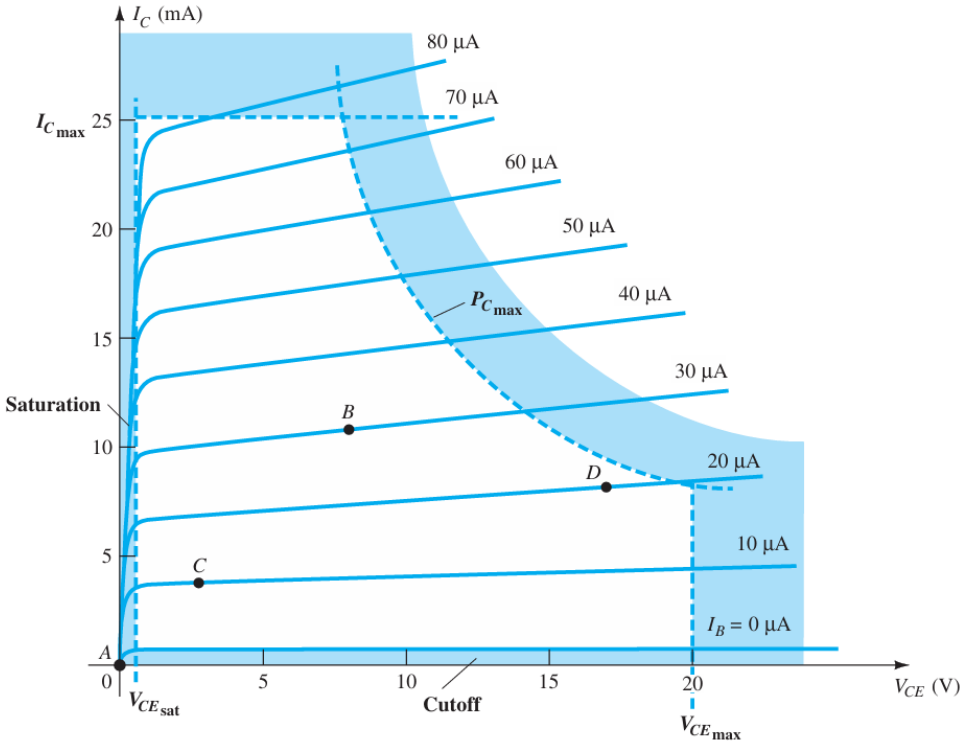


FIG. 4.1
Various operating points within the limits of operation of a transistor.

Operating Point

Temperature also has its effect on the Operating point.

Temperature causes the device parameters like transistor current gain (β_{ac}) and the transistor leakage current (I_{CEO}) to change.

As temperature increases, I_{CEO} increases, resulting in changing the Q point. Thus the network design must also consider temperature stability to reduce the changes in Q point.

The variation of operating point due to variation in temperature is indicated by stability factor (S). Higher the stability of the circuit, better is the circuit.

Transistor Biasing

Transistor Biasing:

Biasing is the process of providing DC voltage which helps in the functioning of the circuit. A transistor is biased in order to make the base- emitter junction forward biased and base-collector junction reverse biased, so that it maintains in active region, to work as an amplifier.

Need for DC biasing:

If a signal of very small voltage is given to the input of BJT, it cannot be amplified. Because, for a BJT, to amplify a signal, two conditions have to be met.

- The input voltage should exceed cut-in voltage for the transistor to be ON.
- The BJT should be in the linear / active region, to be operated as an amplifier.

DC biasing:

- The operating point is a fixed point on the characteristics and is also called quiescent point, denoted by Q-point. The term biasing means the application of dc voltages used to setup a fixed level of current and voltage. Called “dc basing” or “biasing analysis”
- This step determines both the region of operation and the small-signal parameters of each device

Different regions of operation of BJT

Operation in the cutoff, saturation, and linear regions of the BJT characteristic are provided as follows:

1. Linear-region (or Active region) operation:

Base–emitter junction forward-biased, Base–collector junction reverse-biased

2. Cutoff-region operation:

Base–emitter junction reverse-biased, Base–collector junction reverse-biased

3. Saturation-region operation:

Base–emitter junction forward-biased, Base–collector junction forward-biased

Types of BJT Biasing Configuration

Objective is to **determine the terminal voltages and currents of *BJT transistor* and obtain the conditions that ensure biasing in the Active /Linear mode**

Types of Biasing (only the first 3 is included in the syllabus)

1. Fixed Bias configuration
2. Emitter- bias configuration
3. Voltage –divider bias configuration
4. Collector-feedback
5. Emitter-follower
6. Common-base

Fixed-Bias Configuration

- The fixed-bias circuit of Fig. 4.2 is the simplest transistor dc bias configuration. Hence, it is also called as simple biasing.
- For dc, f = 0 Hz, and XC = 1>2pfC = 1>2p(0)C = ∞Ω.

Forward Bias of Base–Emitter

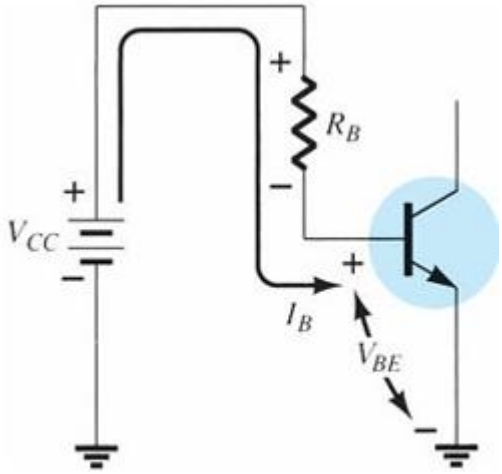
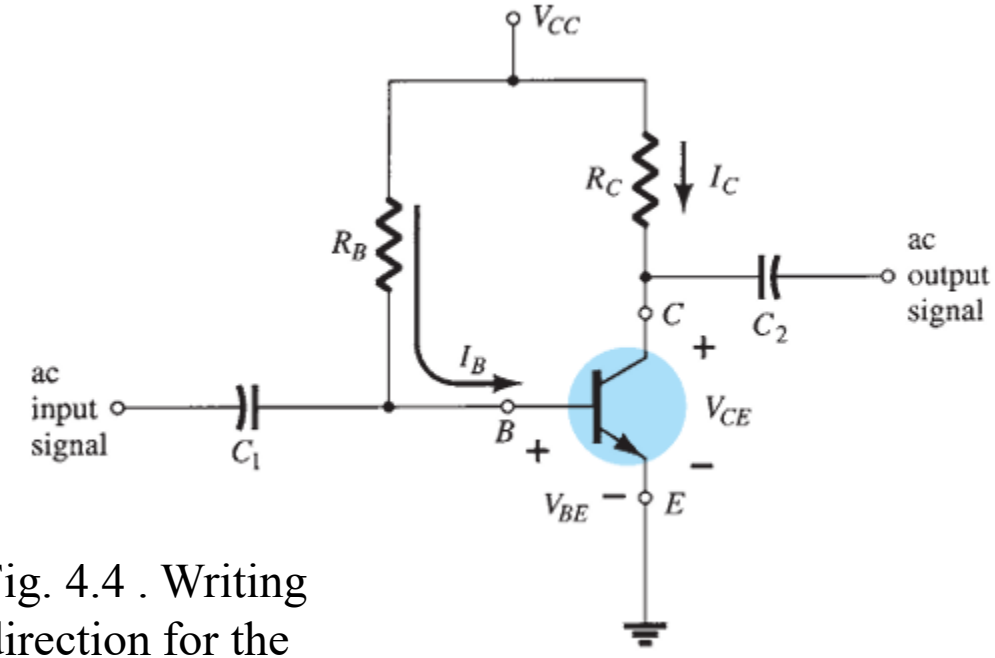


FIG. 4.4
Base–emitter loop.



Consider first the base–emitter circuit loop of Fig. 4.4 . Writing Kirchhoff's voltage equation in the clockwise direction for the loop, we obtain $+V_{CC} - I_B R_B - V_{BE} = 0$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

Fixed-Bias Configuration

The supply voltage V_{CC} and the base–emitter voltage V_{BE} are constants, the selection of a base resistor R_B sets the level of base current for the operating point.

Collector–Emitter Loop

The collector–emitter section of the network appears in Fig. 4.5 with the indicated direction of current I_C and the resulting polarity across R_C $\mathbf{I_C = \beta I_B}$

- Changing R_C to any level will not affect the level of I_B or I_C as long as the device in the active region.
- The level of R_C will determine the magnitude of V_{CE}.

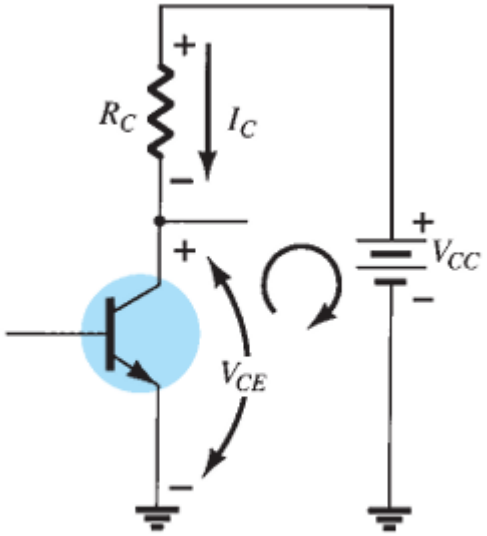


FIG. 4.5
Collector–emitter loop.

$$V_{CE} + I_C R_C - V_{CC} = 0$$

$$V_{CE} = V_{CC} - I_C R_C$$

$$V_{CE} = V_C - V_E$$

$$V_{BE} = V_B - V_E$$

Since, emitter is ground

$$V_{CE} = V_C$$

$$V_{BE} = V_B$$

Fixed-Bias Configuration

Determine the following for the fixed-bias configuration of Fig. 4.7

a. I_{B_Q} and I_{C_Q}.
b. V_{CE_Q}.
c. V_B and V_C.
d. V_{BC}.

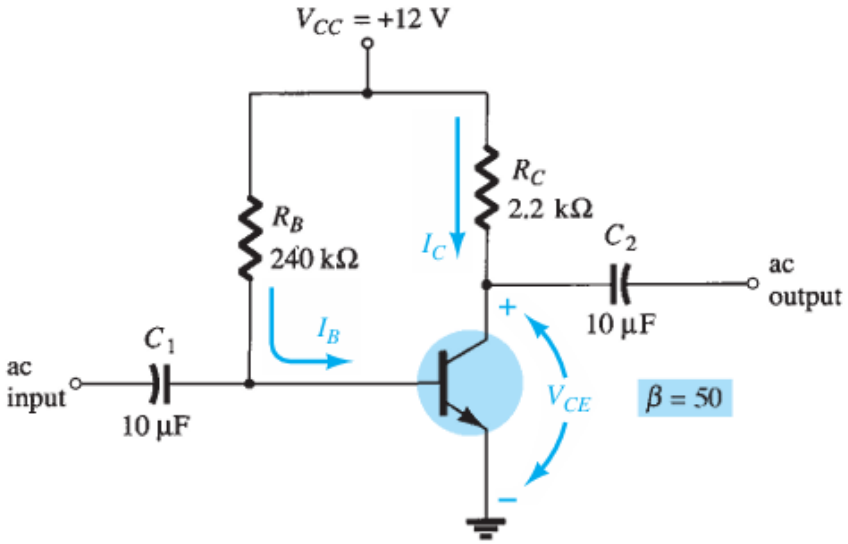


FIG. 4.7
DC fixed-bias circuit for Example 4.1.

a) $$I_{B_Q} = \frac{V_{CC} - V_{BE}}{R_B} = \frac{12\text{ V} - 0.7\text{ V}}{240\text{ k}\Omega} = \mathbf{47.08\ \mu A}$$

$$I_{C_Q} = \beta I_{BQ} = (50)(47.08\ \mu\text{A}) = \mathbf{2.35\ mA}$$

b) $$V_{CE_Q} = V_{CC} - I_C R_C$$
$$= 12\text{ V} - (2.35\text{ mA})(2.2\text{ k}\Omega)$$
$$= \mathbf{6.83\ V}$$

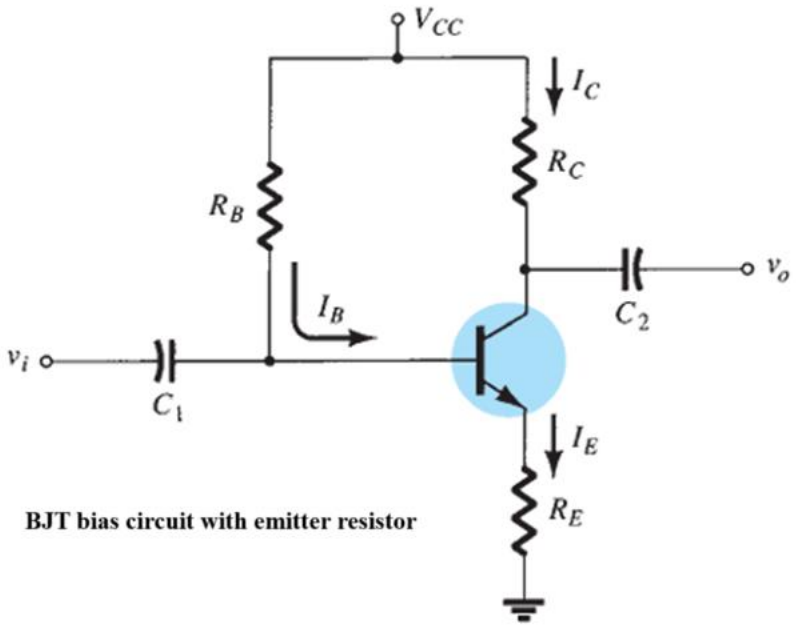
c) $$V_B = V_{BE} = \mathbf{0.7\ V}$$
$$V_C = V_{CE} = \mathbf{6.83\ V}$$

d) $$V_{BC} = V_B - V_C = 0.7\text{ V} - 6.83\text{ V}$$
$$= \mathbf{-6.13\ V}$$

The negative sign revealing that the junction is reversed-biased, as it should be for linear amplification.

Emitter-Bias Configuration

- The DC bias network of fig below contains an emitter resistor to improve the stability level over that of the fixed bias configuration.



BJT bias circuit with emitter resistor

Emitter-Bias Configuration

Base–Emitter Loop

Applying Kirchhoff's voltage law around the indicated loop in the clockwise direction results in the following equation:

$$+V_{CC} - I_B R_B - V_{BE} - I_E R_E = 0$$

Since $I_E = (\beta + 1)I_B$, substitute in the above equation

$$V_{CC} - I_B R_B - V_{BE} - (\beta + I)I_B R_E = 0$$

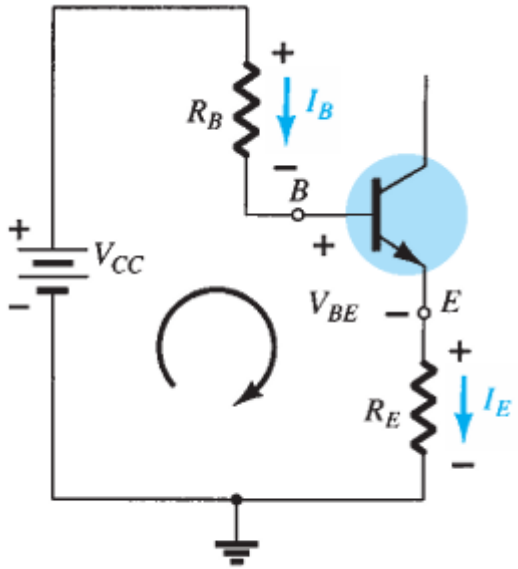
$$-I_B(R_B + (\beta + 1)R_E) + V_{CC} - V_{BE} = 0$$

Multiplying through by (-1), we have

$$I_B(R_B + (\beta + 1)R_E) - V_{CC} + V_{BE} = 0$$

$$I_B(R_B + (\beta + 1)R_E) = V_{CC} - V_{BE}$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)R_E}$$



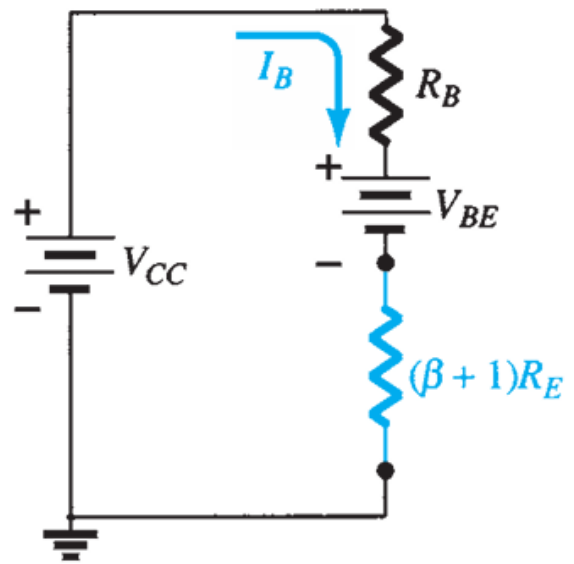
Base-emitter loop

Note: that the only difference between this equation for I_B and that obtained for the fixed bias configuration is the term $(\beta+ 1)R_E$.

Emitter-Bias Configuration

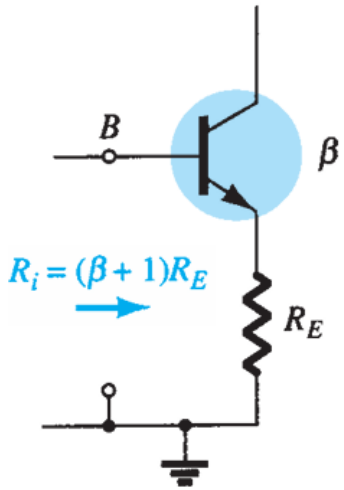
$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)R_E}$$

the network derived from this I_B equation is



- ✓ Note that aside from the base-to-emitter voltage V_{BE}, the resistor RE is reflected back to the input base circuit by a factor (β+1).
- ✓ In other words, the emitter resistor, which a part of the collector-emitter loop, "appears as" $(\beta+1)R_E$ in the base-emitter loop.
- ✓ Thus, the reflected impedance level of R_E, in the base circuit as shown in figure. Therefore, for this configuration the input impedance is given by

$$R_i = (\beta + 1)R_E$$



Emitter-Bias Configuration

Collector–Emitter Loop

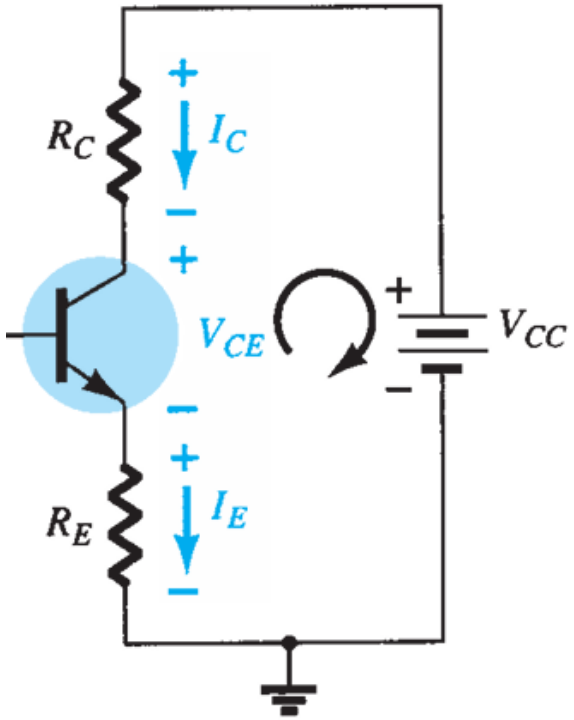
The collector–emitter loop appears as shown in figure. Applying Kirchhoff's voltage law for the indicated loop in the clockwise direction results in

$$+I_E R_E + V_{CE} + I_C R_C - V_{CC} = 0$$

Substituting $I_E \cong I_C$ and grouping terms gives

$$V_{CE} - V_{CC} + I_C(R_C + R_E) = 0$$

$$\boxed{V_{CE} = V_{CC} - I_C(R_C + R_E)}$$



Collector - Emitter loop

Voltage from emitter to ground is given by $\boxed{V_E = I_E R_E}$

Voltage between collector and emitter is $V_{CE} = V_C - V_E$

Voltage from collector to ground is given by $\boxed{V_C = V_{CE} + V_E}$

$$\boxed{V_C = V_{CC} - I_C R_C}$$

Voltage at base w.r.t to ground is given by $\boxed{V_B = V_{CC} - I_B R_B}$

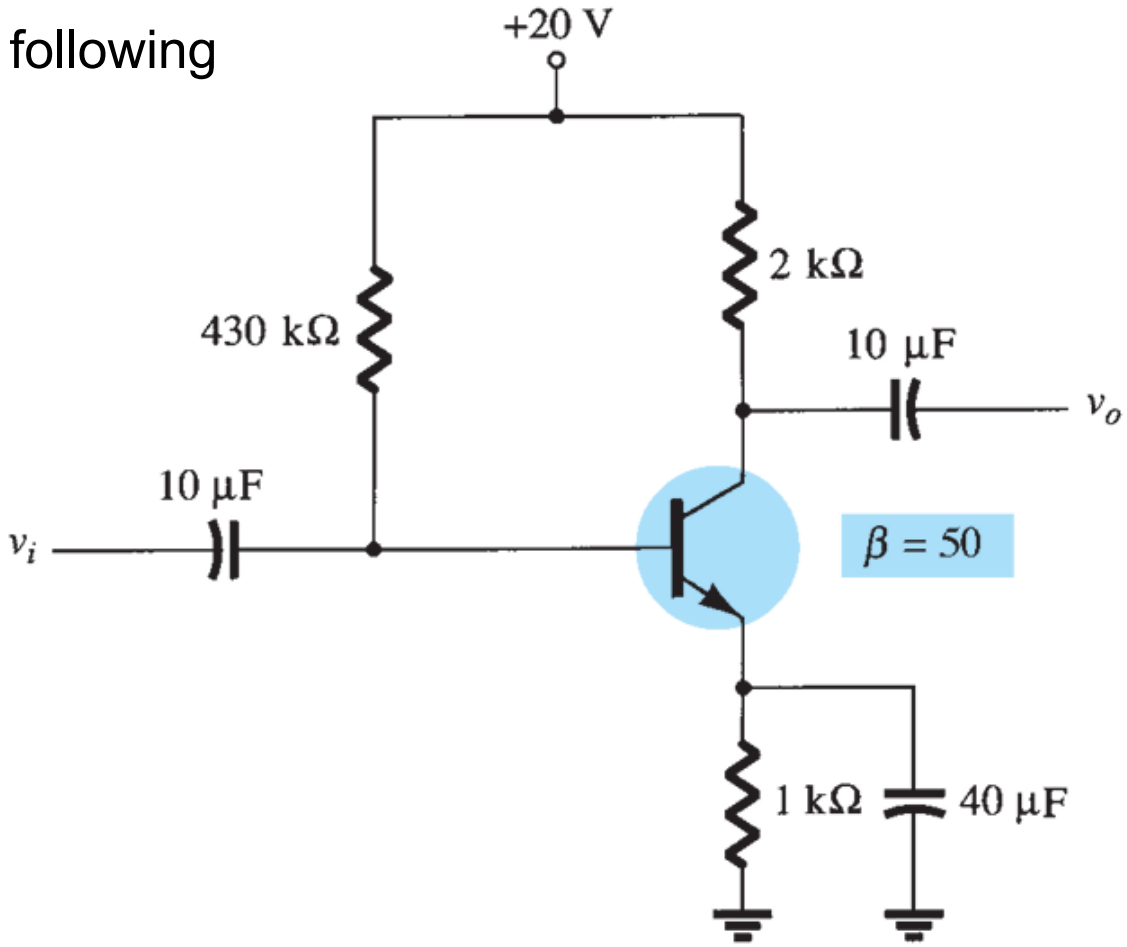
$$\boxed{V_B = V_{BE} + V_E}$$

Emitter-Bias Configuration

Problem

For the emitter-bias network of Fig. 4.23 , determine the following

a. I_B.
b. I_C.
c. V_{CE}.
d. V_C.
e. V_E.
f. V_B.
g. V_{BC}.



Emitter-Bias Configuration

Solution

a) $$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)R_E} = \frac{20\text{ V} - 0.7\text{ V}}{430\text{ k}\Omega + (51)(1\text{ k}\Omega)}$$

$$= \frac{19.3\text{ V}}{481\text{ k}\Omega} = \mathbf{40.1\ \mu A}$$

b) $$I_C = \beta I_B$$

$$= (50)(40.1\ \mu\text{A})$$

$$\cong \mathbf{2.01\ mA}$$

c) $$V_{CE} = V_{CC} - I_C(R_C + R_E)$$

$$= 20\text{ V} - (2.01\text{ mA})(2\text{ k}\Omega + 1\text{ k}\Omega) = 20\text{ V} - 6.03\text{ V}$$

$$= \mathbf{13.97\ V}$$

d) $$V_C = V_{CC} - I_C R_C$$

$$= 20\text{ V} - (2.01\text{ mA})(2\text{ k}\Omega) = 20\text{ V} - 4.02\text{ V}$$

$$= \mathbf{15.98\ V}$$

e) $$V_E = V_C - V_{CE}$$

$$= 15.98\text{ V} - 13.97\text{ V}$$

$$= \mathbf{2.01\ V}$$

f) $$V_B = V_{BE} + V_E$$

$$= 0.7\text{ V} + 2.01\text{ V}$$

$$= \mathbf{2.71\ V}$$

or $$V_E = I_E R_E \cong I_C R_E$$

$$= (2.01\text{ mA})(1\text{ k}\Omega)$$

$$= \mathbf{2.01\ V}$$

g) $$V_{BC} = V_B - V_C$$

$$= 2.71\text{ V} - 15.98\text{ V}$$

$$= \mathbf{-13.27\ V}\text{ (reverse-biased as required)}$$

Emitter-Bias Configuration

- **Improved Bias Stability in Emitter bias configuration**

The addition of the emitter resistor to the dc bias of the BJT provides improved stability, that is, the dc bias currents and voltages remain closer to where they were set by the circuit when outside conditions, such as temperature and transistor beta, change.

- The comparison table of the bias voltage and currents of the circuits of Fixed and emitter bias for the given value of beta= 50 and for a new value of beta = 100. The changes in I_C and V_{CE} for the same increase in beta is.

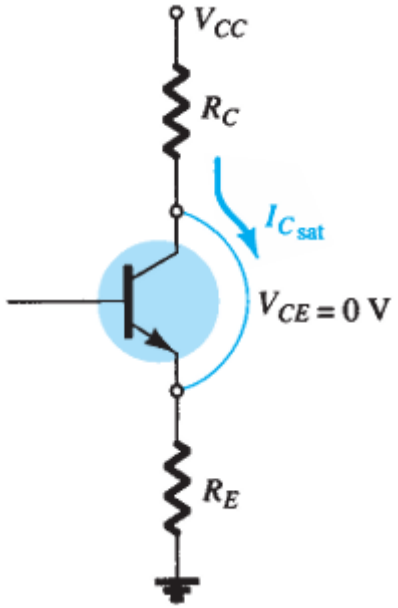
Fixed bias configuration				Emitter bias configuration			
β	I_B (μA)	I_C (mA)	V_{CE} (V)	β	I_B (μA)	I_C (mA)	V_{CE} (V)
50	47.08	2.35	6.83	50	40.1	2.01	13.97
100	47.08	4.71	1.64	100	36.3	3.63	9.11
The collector current is seen to change by 100% due to the 100% change in the value of beta. The value of I_B is the same, and V_{CE} decreased by 76%				The collector current increases by about 81% due to the 100% increase in beta. I_B decreased, maintain the value of I_C —or at least reducing the overall change in I_C due to the change in beta. The change in V_{CE} has dropped to about 35%			

- Thus, the emitter – bias configuration is therefore more stable than that of fixed bias for the same change in beta.

Emitter-Bias Configuration

Saturation Level

- The collector saturation level or maximum collector current for an emitter-bias design can be determined using the same approach applied to the fixed-bias configuration
- Apply a short circuit between the collector–emitter terminals as shown in below and calculate the resulting collector current.



$$I_{C_{sat}} = \frac{V_{CC}}{R_C + R_E}$$

Voltage- Divider Bias Configuration

- In the previous bias configurations, the bias current I_{CQ} and voltage V_{CEQ} were a function of the current gain β of the transistor.
- Since, β is temperature sensitive, especially for silicon transistors, and the actual value of beta is usually not well defined.
- it is necessary to develop a bias circuit that is less dependent on, or independent of, the transistor beta.
- Thus, Voltage divider bias configuration is preferred.

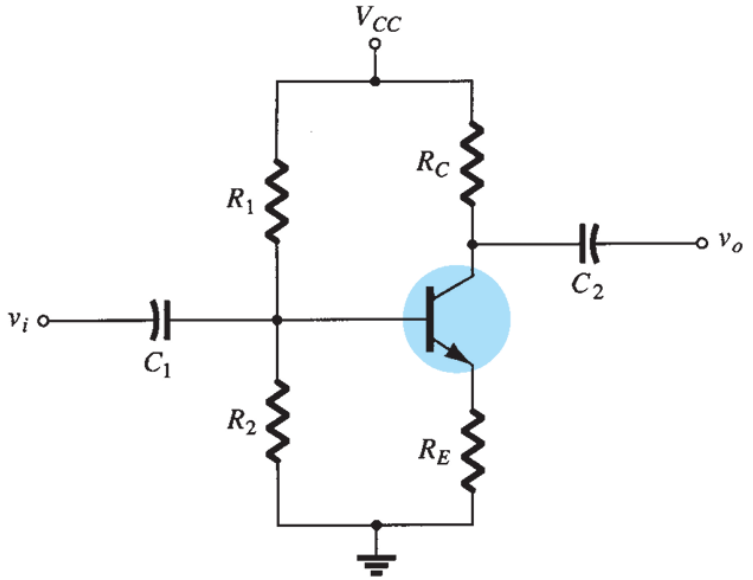


FIG. 4.28
Voltage-divider bias configuration.

Voltage- Divider Bias Configuration

- Approximate Analysis: can be applied only if specific conditions are satisfied

➢ The input section of the voltage-divider configuration can be represented by the network of Fig. 4.36

➢ The R_i is the resistance between base and ground for the transistor with the emitter resistance, with the reflected resistance between the base and emitter, similar to the Emitter bias configuration and is given by $R_i = (\beta+1)R_E$

➢ If Ri is much larger than the resistance R_2 , the current I_B will be much smaller than I_2 and I_2 will be approximately equal to I_1

Since, $I_B \cong 0$, the voltage drop across R_2 is given by $\frac{R_2}{R_1+R_2} V_{CC}$

(using the voltage divider rule, hence the name of the configuration)

➢ **If $\beta R_E \geq 10R_2$, then the approximation method can be applied to determine the biasing current and voltage.**

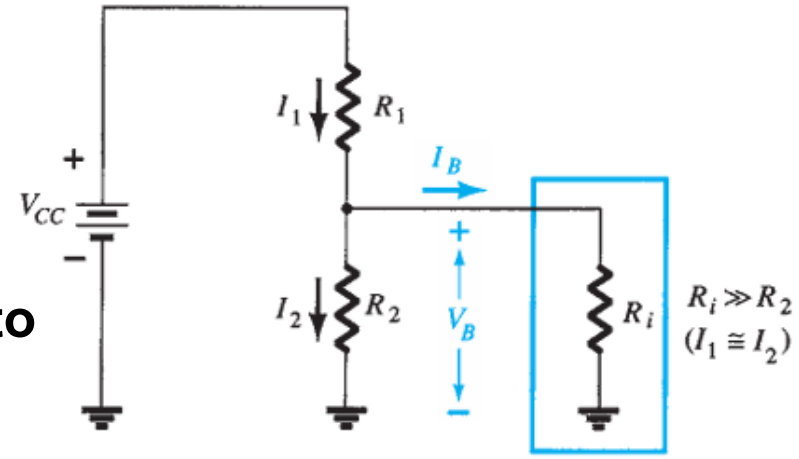


FIG. 4.36

Partial-bias circuit for calculating the approximate base voltage V_B.

Voltage- Divider Bias Configuration

- Approximate Analysis:

➢ V_E and I_E are calculated by $V_E = V_B - V_{BE}$ and $I_E = \frac{V_E}{R_E}$

➢ And $I_{C_Q} \cong I_E$

➢ The collector-to-emitter voltage is determined by $V_{CE} = V_{CC} - I_C R_C - I_E R_E$

➢ Since $I_E \cong I_C$,

$$V_{CE_Q} = V_{CC} - I_C(R_C + R_E)$$

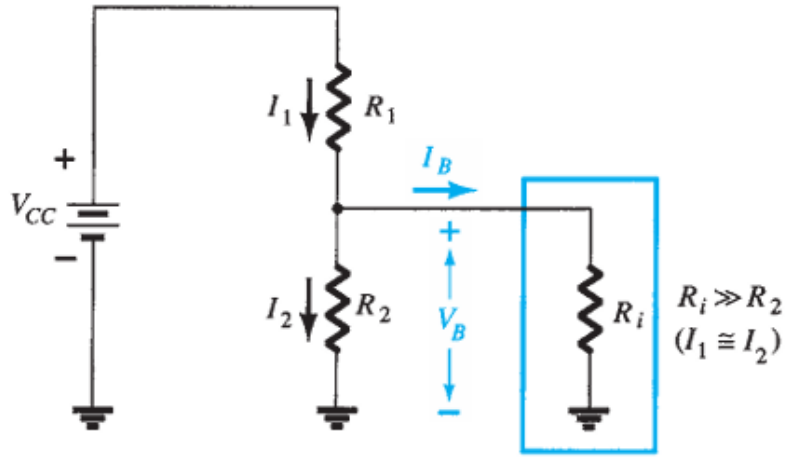


FIG. 4.36
Partial-bias circuit for calculating the approximate base voltage V_B.

➢ In all the biasing voltage and current equation β does not appear and the Q -point (as determined by I_{CQ} and V_{CEQ}) is therefore independent of the value of β.

➢ Transistor Saturation

$$I_{C_{sat}} = I_{C_{max}} = \frac{V_{CC}}{R_C + R_E}$$

Voltage- Divider Bias Configuration

Determine the dc bias voltage V_{CE} and the current I_C for the voltage divider configuration of Fig. 4.35 .

Solution: check the condition to apply approximate method

$$\beta R_E \geq 10R_2$$
$$(100)(1.5\,\text{k}\Omega) \geq 10(3.9\,\text{k}\Omega)$$
$$150\,\text{k}\Omega \geq 39\,\text{k}\Omega \ (\textit{satisfied})$$

I_{CQ} calculation

$$V_B = \frac{R_2 V_{CC}}{R_1 + R_2} = \frac{(3.9\,\text{k}\Omega)(22\,\text{V})}{39\,\text{k}\Omega + 3.9\,\text{k}\Omega} = 2\,\text{V}$$

$$V_E = V_B - V_{BE} = 2\,\text{V} - 0.7\,\text{V} = 1.3\,\text{V}$$

$$I_{CQ} \cong I_E = \frac{V_E}{R_E} = \frac{1.3\,\text{V}}{1.5\,\text{k}\Omega} = \mathbf{0.867\,mA}$$

V_{CEQ} Calculation

$$V_{CE_Q} = V_{CC} - I_C(R_C + R_E)$$
$$= 22\,\text{V} - (0.867\,\text{mA})(10\,\text{kV} + 1.5\,\text{k}\Omega)$$
$$= 22\,\text{V} - 9.97\,\text{V}$$
$$= \mathbf{12.03\,V}$$

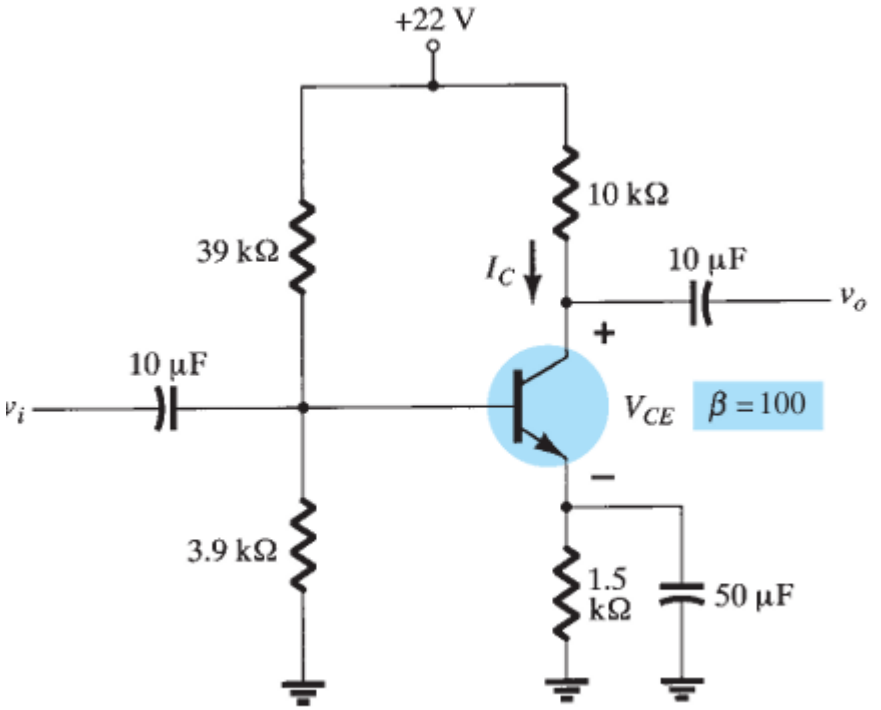
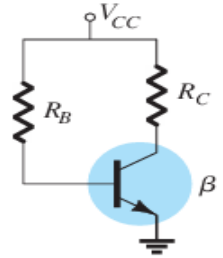
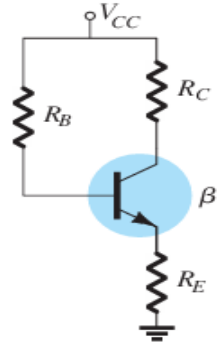
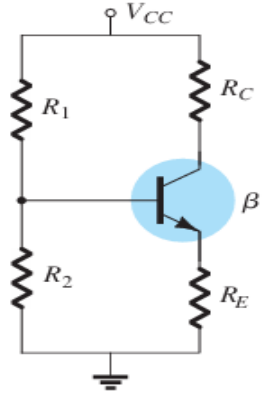


FIG. 4.35

Summary Table of biasing circuits

Type	Configuration	Pertinent Equations
Fixed-bias		$I_B = \frac{V_{CC} - V_{BE}}{R_B}$ $I_C = \beta I_B, I_E = (\beta + 1)I_B$ $V_{CE} = V_{CC} - I_C R_C$
Emitter-bias		$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)R_E}$ $I_C = \beta I_B, I_E = (\beta + 1)I_B$ $R_i = (\beta + 1)R_E$ $V_{CE} = V_{CC} - I_C (R_C + R_E)$
Voltage-divider bias		APPROXIMATE: $\beta R_E \geq 10R_2$ $V_B = \frac{R_2 V_{CC}}{R_1 + R_2}, V_E = V_B - V_{BE}$ $I_E = \frac{V_E}{R_E}, I_B = \frac{I_E}{\beta + 1}$ $V_{CE} = V_{CC} - I_C(R_C + R_E)$

DESIGN OPERATIONS

- The design process is one where a current and/or voltage may be specified and the elements required to establish the designated levels must be determined.
- This synthesis process requires a clear understanding of the characteristics of the device, the basic equations for the network, and a firm understanding of the basic laws of circuit analysis, such as Ohm's law, Kirchhoff's voltage law, and so on.
- EXAMPLE 4.21 Given the device characteristics of Fig. 4.59a , determine V_{CC}, R_B, and R_C for the fixed-bias configuration of Fig. 4.59b .

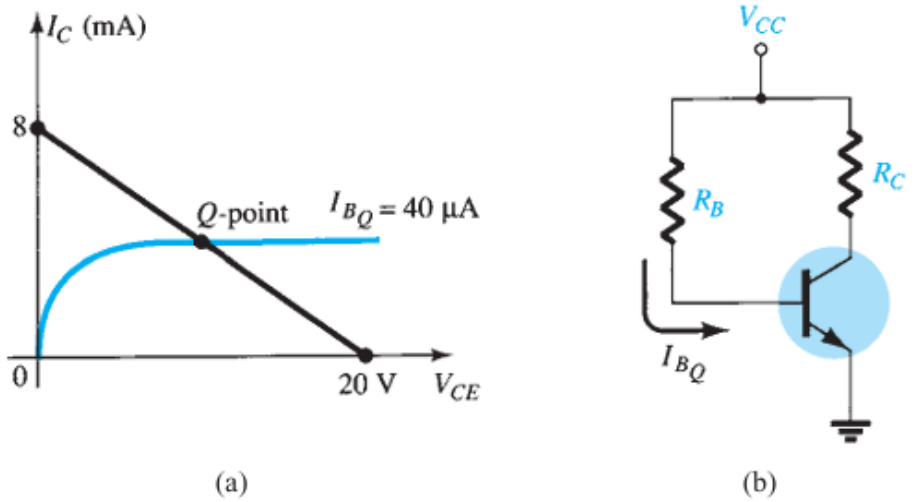
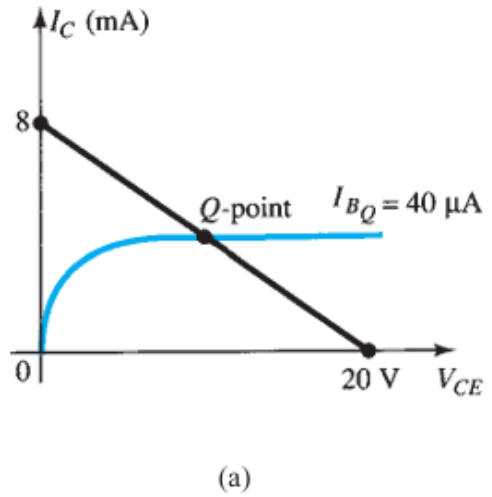


FIG. 4.59
Example 4.21.

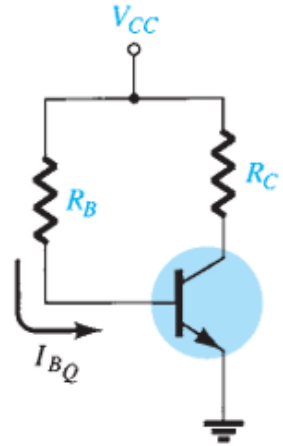
DESIGN OPERATIONS

- EXAMPLE 4.21 Given the device characteristics of Fig. 4.59a , determine V_{CC}, R_B, and R_C for the fixed-bias configuration of Fig. 4.59b .

Solution: From the load line



(a)



(b)

FIG. 4.59
Example 4.21.

R_C calculation

$$V_{CC} = \mathbf{20\ V}$$

$$I_C = \left.\frac{V_{CC}}{R_C}\right|_{V_{CE}=0\ V}$$

$$R_C = \frac{V_{CC}}{I_C} = \frac{20\ V}{8\ mA} = \mathbf{2.5\ k\Omega}$$

R_B calculation

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

$$R_B = \frac{V_{CC} - V_{BE}}{I_B}$$

$$= \frac{20\ V - 0.7\ V}{40\ \mu A} = \frac{19.3\ V}{40\ \mu A}$$

$$= \mathbf{482.5\ k\Omega}$$

Standard resistor values are

$$R_C = 2.4\ k\Omega$$

$$R_B = 470\ k\Omega$$

Using standard resistor values gives

$$I_B = 41.1\ \mu A$$

which is well within 5% of the value specified.

DESIGN OPERATIONS

- EXAMPLE 4.22 Given that $I_{CQ} = 2$ mA and $V_{CEQ} = 10$ V, determine R_1 and R_C for the network of Fig. 4.60

Solution:

R1 calculation

$$V_E = I_E R_E \cong I_C R_E$$
$$= (2\text{ mA})(1.2\text{ k}\Omega) = 2.4\text{ V}$$
$$V_B = V_{BE} + V_E = 0.7\text{ V} + 2.4\text{ V} = 3.1\text{ V}$$
$$V_B = \frac{R_2 V_{CC}}{R_1 + R_2} = 3.1\text{ V}$$
$$\frac{(18\text{ k}\Omega)(18\text{ V})}{R_1 + 18\text{ k}\Omega} = 3.1\text{ V}$$
$$324\text{ k}\Omega = 3.1R_1 + 55.8\text{ k}\Omega$$
$$3.1R_1 = 268.2\text{ k}\Omega$$
$$R_1 = \frac{268.2\text{ k}\Omega}{3.1} = \mathbf{86.52\text{ k}\Omega}$$

R_C Calculation

$$R_C = \frac{V_{R_C}}{I_C} = \frac{V_{CC} - V_C}{I_C}$$
$$V_C = V_{CE} + V_E = 10\text{ V} + 2.4\text{ V} = 12.4\text{ V}$$
$$R_C = \frac{18\text{ V} - 12.4\text{ V}}{2\text{ mA}}$$
$$= \mathbf{2.8\text{ k}\Omega}$$

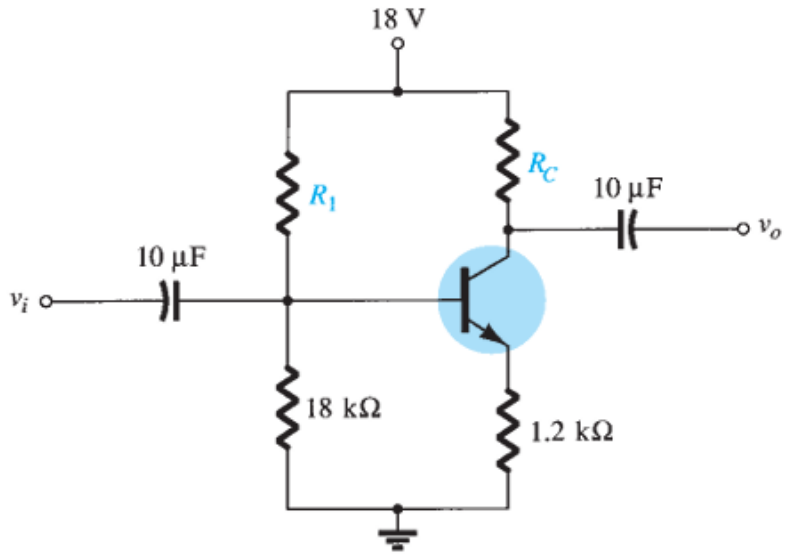


FIG. 4.60
Example 4.22.

DESIGN OPERATIONS

- EXAMPLE 4.23 The emitter-bias configuration of Fig. 4.61 has the following specifications: $I_{CQ} = 1/2 I_{sat}$, $I_{Csat} = 8$ mA, $V_C = 18$ V, and $\beta = 110$. Determine R_C, R_E, and R_B.

- **Solution:**

R_C calculation

$$I_{C_Q} = \tfrac{1}{2} I_{C_{sat}} = 4 \text{ mA}$$

$$R_C = \frac{V_{R_C}}{I_{C_Q}} = \frac{V_{CC} - V_C}{I_{C_Q}}$$

$$= \frac{28 \text{ V} - 18 \text{ V}}{4 \text{ mA}} = \mathbf{2.5\ k\Omega}$$

R_E calculation

$$I_{C_{sat}} = \frac{V_{CC}}{R_C + R_E}$$

$$R_C + R_E = \frac{V_{CC}}{I_{C_{sat}}} = \frac{28 \text{ V}}{8 \text{ mA}} = 3.5 \text{ k}\Omega$$

$$R_E = 3.5 \text{ k}\Omega - R_C$$

$$= 3.5 \text{ k}\Omega - 2.5 \text{ k}\Omega$$

$$= \mathbf{1\ k\Omega}$$

R_B calculation

$$I_{B_Q} = \frac{I_{C_Q}}{\beta} = \frac{4 \text{ mA}}{110} = 36.36\ \mu\text{A}$$

$$I_{B_Q} = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)R_E}$$

$$R_B + (\beta + 1)R_E = \frac{V_{CC} - V_{BE}}{I_{B_Q}}$$

$$R_B = \frac{V_{CC} - V_{BE}}{I_{B_Q}} - (\beta + 1)R_E$$

$$= \frac{28 \text{ V} - 0.7 \text{ V}}{36.36\ \mu\text{A}} - (111)(1 \text{ k}\Omega)$$

$$= \frac{27.3 \text{ V}}{36.36\ \mu\text{A}} - 111 \text{ k}\Omega$$

$$= \mathbf{639.8\ k\Omega}$$

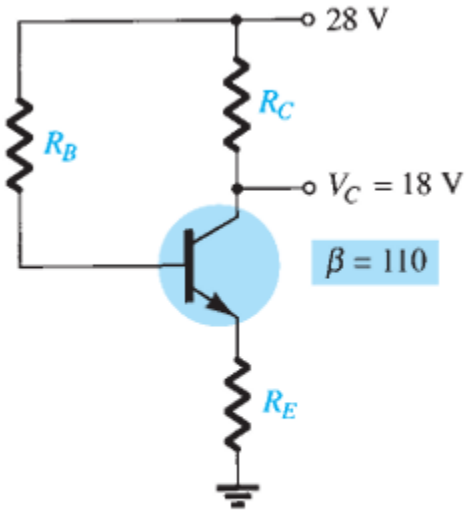


FIG. 4.61
Example 4.23.

For standard values,

$$R_C = 2.4 \text{ k}\Omega$$

$$R_E = 1 \text{ k}\Omega$$

$$R_B = 620 \text{ k}\Omega$$

DESIGN OPERATIONS

- EXAMPLE 4.24 Determine the resistor values for the network of Fig. 4.62 for the indicated operating point and supply voltage.
- **Solution:**

$$V_E = \frac{1}{10}V_{CC} = \frac{1}{10}(20\text{ V}) = 2\text{ V}$$

$$R_E = \frac{V_E}{I_E} \cong \frac{V_E}{I_C} = \frac{2\text{ V}}{2\text{ mA}} = \mathbf{1\,k\Omega}$$

$$R_C = \frac{V_{R_C}}{I_C} = \frac{V_{CC} - V_{CE} - V_E}{I_C} = \frac{20\text{ V} - 10\text{ V} - 2\text{ V}}{2\text{ mA}} = \frac{8\text{ V}}{2\text{ mA}}$$

$$= \mathbf{4\,k\Omega}$$

$$I_B = \frac{I_C}{\beta} = \frac{2\text{ mA}}{150} = 13.33\,\mu\text{A}$$

$$R_B = \frac{V_{R_B}}{I_B} = \frac{V_{CC} - V_{BE} - V_E}{I_B} = \frac{20\text{ V} - 0.7\text{ V} - 2\text{ V}}{13.33\,\mu\text{A}}$$

$$\cong \mathbf{1.3\,M\Omega}$$

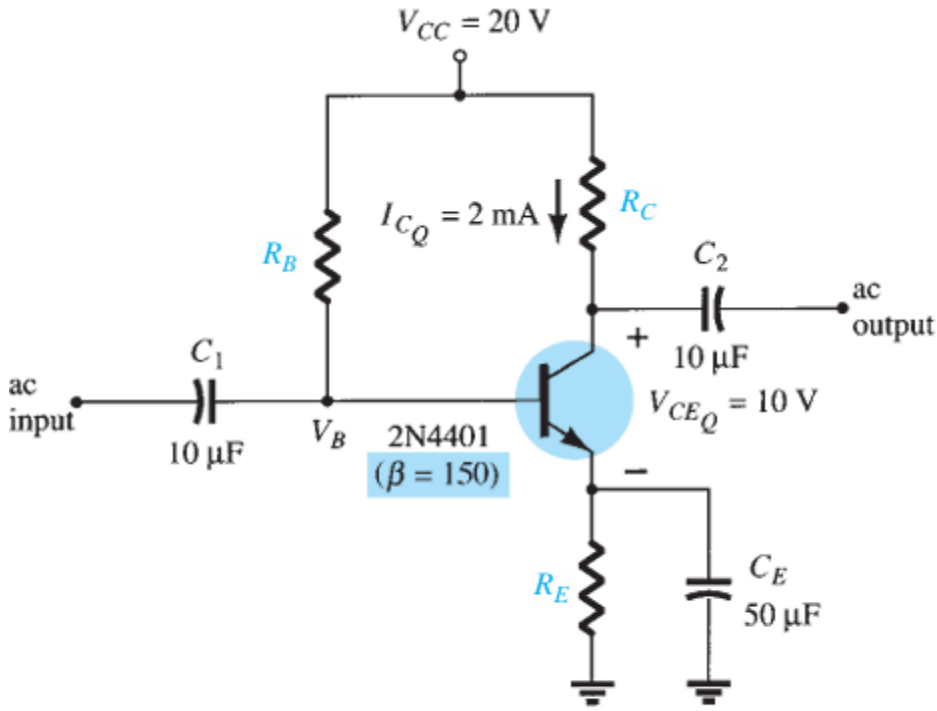


FIG. 4.62

Emitter-stabilized bias circuit for design consideration.

DESIGN OPERATIONS

- EXAMPLE 4.25 Determine the levels of RC, RE, R1, and R2 for the network of Fig. 4.63 for the operating point indicated.

- **Solution:**

$$V_E = \frac{1}{10}V_{CC} = \frac{1}{10}(20\text{ V}) = 2\text{ V}$$

$$R_E = \frac{V_E}{I_E} \cong \frac{V_E}{I_C} = \frac{2\text{ V}}{10\text{ mA}} = \mathbf{200\ \Omega}$$

$$R_C = \frac{V_{R_C}}{I_C} = \frac{V_{CC} - V_{CE} - V_E}{I_C} = \frac{20\text{ V} - 8\text{ V} - 2\text{ V}}{10\text{ mA}} = \frac{10\text{ V}}{10\text{ mA}}$$

$$= \mathbf{1\ k\Omega}$$

$$V_B = V_{BE} + V_E = 0.7\text{ V} + 2\text{ V} = 2.7\text{ V}$$

- **Using $\beta R_E \geq 10R_2$,**

R_2 calculation

$$R_2 \leq \frac{1}{10}\beta R_E$$

$$V_B = \frac{R_2}{R_1 + R_2}V_{CC}$$

$$R_2 \leq \frac{1}{10}(80)(0.2\text{ k}\Omega)$$

$$= \mathbf{1.6\ k\Omega}$$

R_1 calculation

$$V_B = 2.7\text{ V} = \frac{(1.6\text{ k}\Omega)(20\text{ V})}{R_1 + 1.6\text{ k}\Omega}$$

$$2.7R_1 + 4.32\text{ k}\Omega = 32\text{ k}\Omega$$

$$2.7R_1 = 27.68\text{ k}\Omega$$

$$R_1 = \mathbf{10.25\ k\Omega} \quad (\text{use } 10\text{ k}\Omega)$$

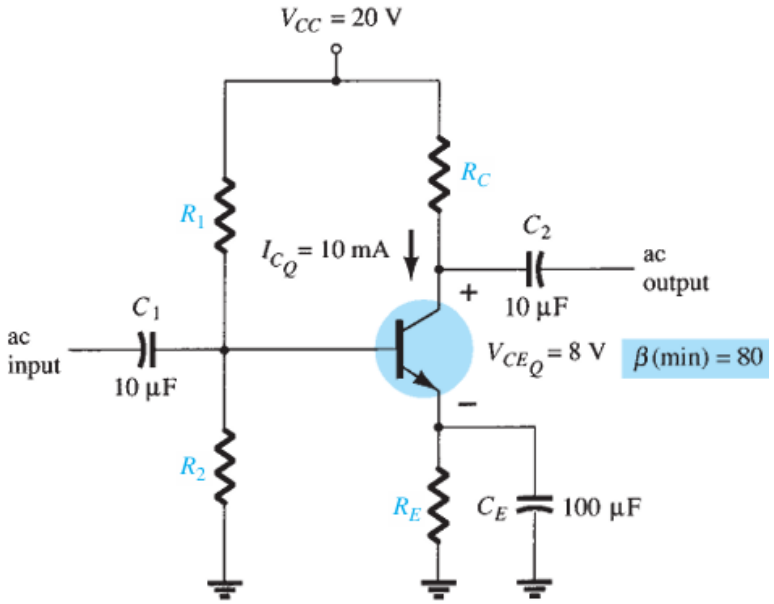


FIG. 4.63
Current-gain-stabilized circuit for design considerations.

Single stage CE Amplifier

- Fig shows a single stage CE amplifier. The different circuit elements and their functions are described as follows.

(i) Biasing circuit :

The resistances R_1, R_2 and R_E form the biasing and stabilization circuit.

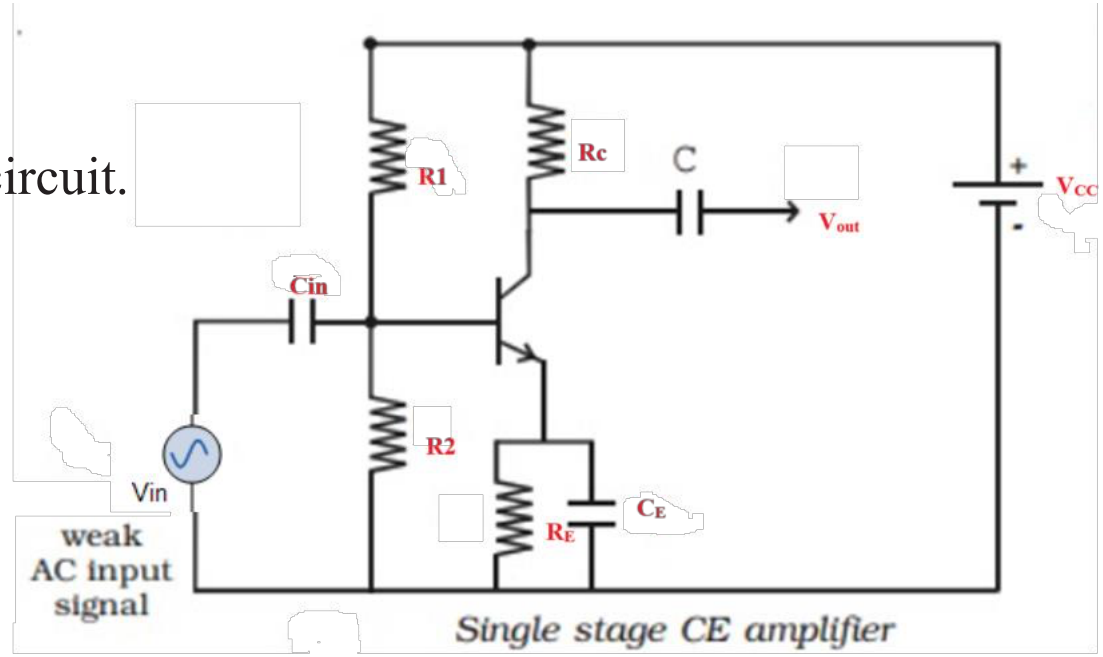
(ii)Input capacitance C_{in} :

This is used to couple the signal to the base of the transistor.

If this is not used, the signal source resistance will come across

R_2 and thus changes the bias condition of the transistor.

The capacitor C_{in} allows only a.c. signal to flow.



(iii) Emitter bypass capacitor C_E :

This is connected in parallel with R_E to provide a low reactance path to the amplified a.c. signal. If it is not used, then amplified a.c. signal flowing through R_E will cause a voltage drop across it, thereby shifting the output voltage.

Single stage CE Amplifier

(iv)**Coupling capacitor C :**

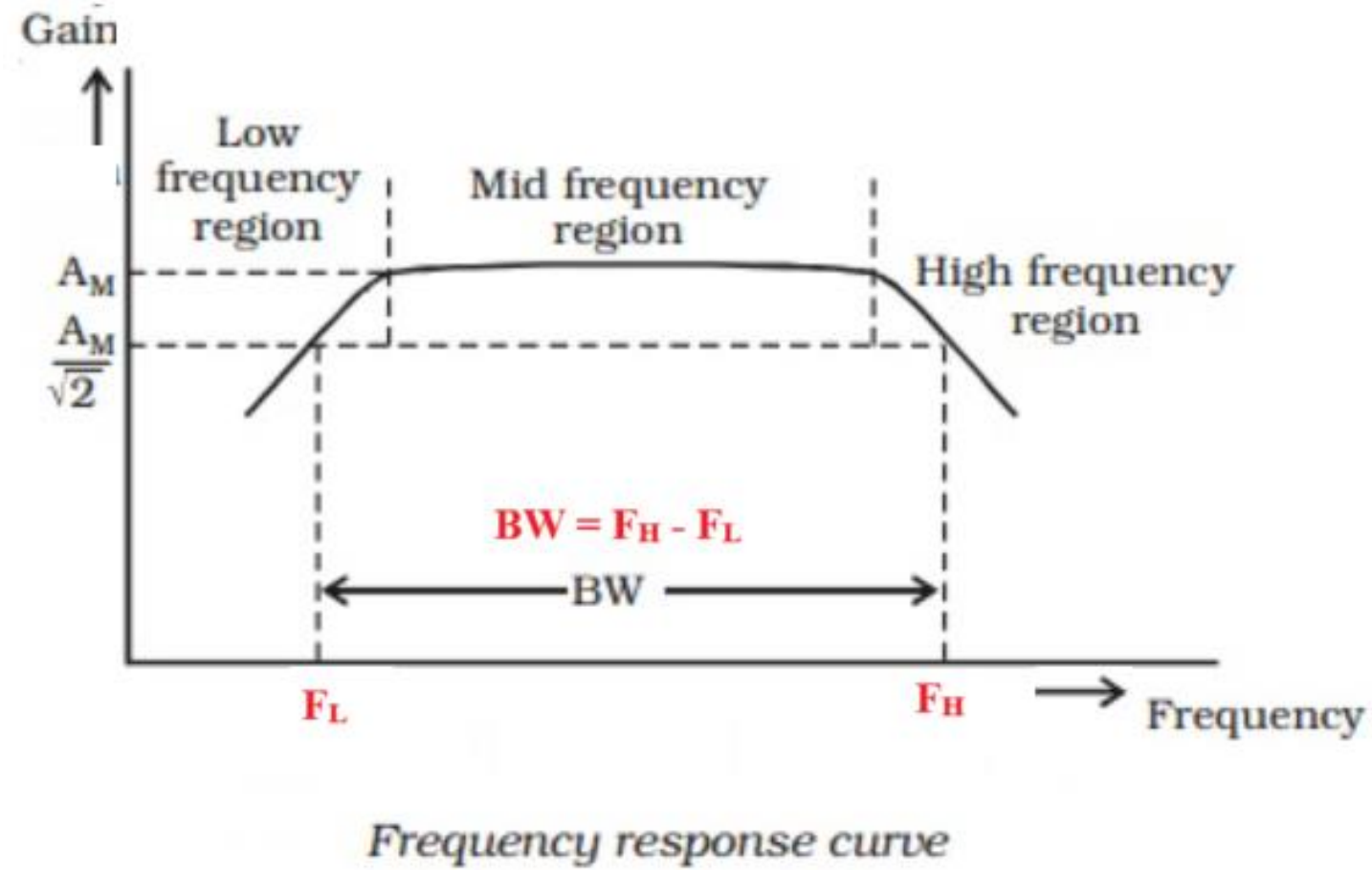
This is used to couple the amplified signal to the output device. This capacitor C allows only a.c. signal to flow.

(v) Working

- When a weak input a.c. signal is applied to the base of the transistor, a small base current flows**.**
- Due to transistor action, a much larger a.c. current flows through collector load R_C, a large voltage appears across R_C and hence at the output.
- Therefore, a weak signal applied to the base appears in amplified form at the collector of circuit.
- Voltage gain (A_v) of the amplifier is the ratio of the amplified output voltage to the input voltage.

Single stage CE Amplifier

(vi) ***Frequency response and bandwidth***



Frequency response curve

THANK YOU

Department of Electronics and Communication