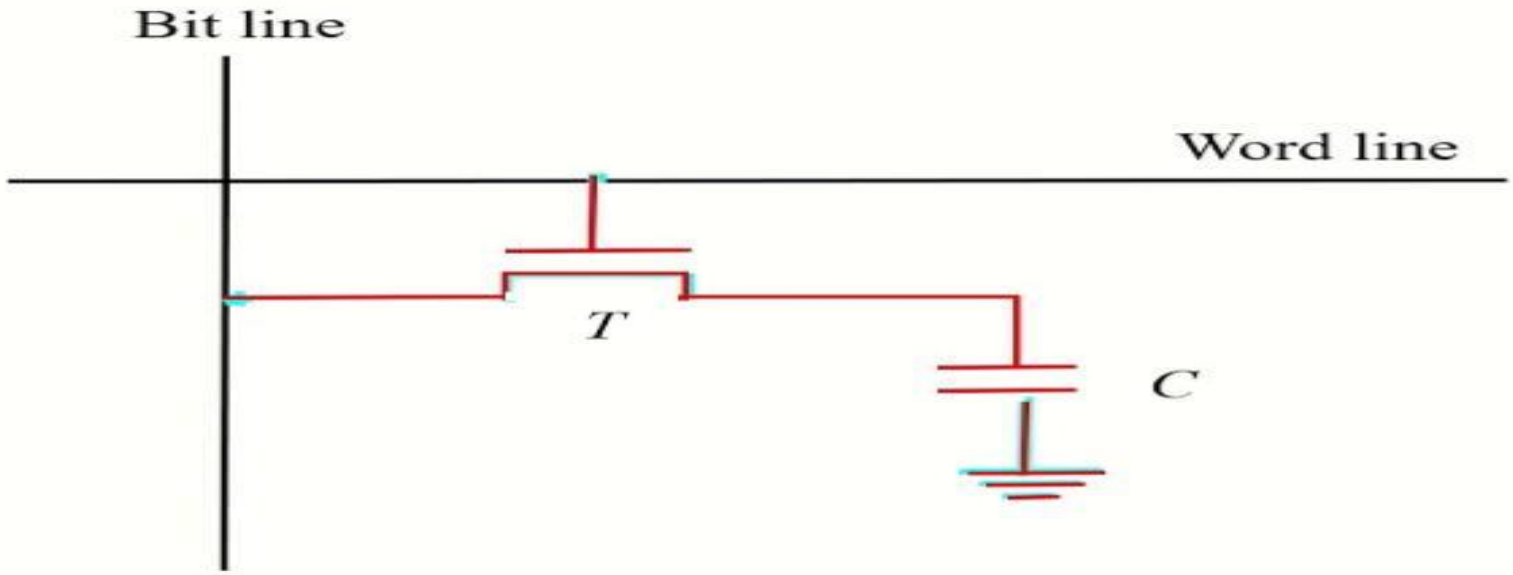
Drams

- **Dynamic RAMS (DRAMs) are cheap and area efficient, but they cannot retain their state indefinitely.**
- **Information stored in the form of charge on a capacitor can be maintained only for tens of milliseconds.**
- **Contents must be periodically refreshed.**

A single transistor dynamic memory cell



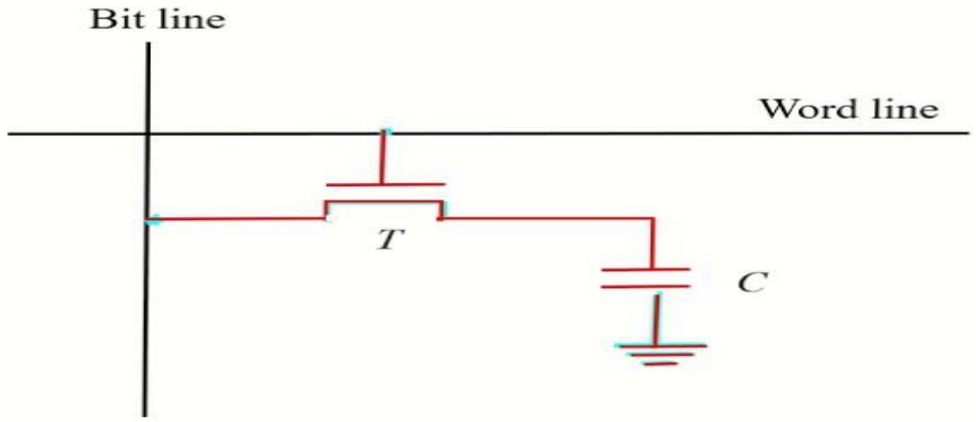
A single-transistor dynamic memory cell

A single transistor dynamic memory cell

- **Components:**
- **1. Access Transistor: A single transistor acts as a switch to control access to the storage capacitor.**
- **2. Storage Capacitor: A capacitor stores the actual data bit in the form of an electrical charge.**
- **3. Bit Line: A bit line is a wire that connects the memory cell to the sense amplifier.**
- **4. Word Line: A word line is a wire that selects the memory cell for reading or writing.**

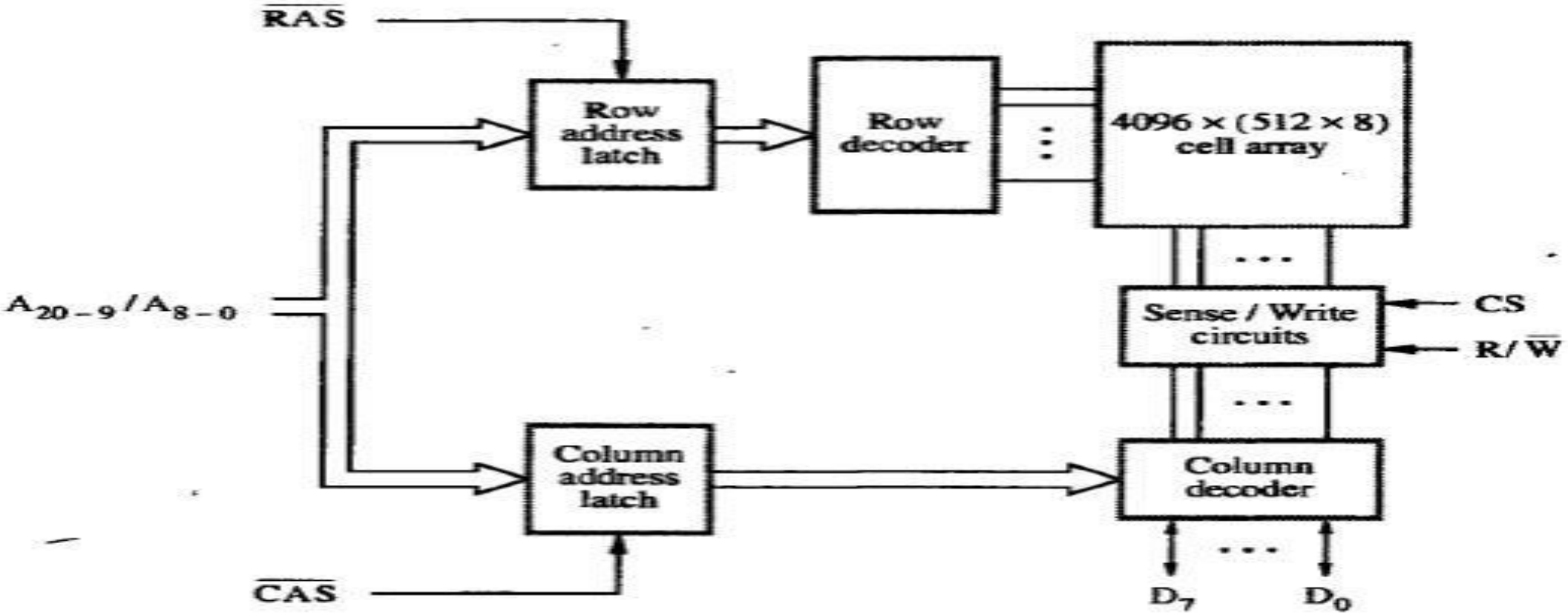
1-Transistor Memory Cell (DRAM)

- • Write Operation:
- 1. Activate the word line.
- 2. Transistor in selected cell is turned ON
- • 3.Capacitor gets charged to the voltage supplied to bit line.
- Read Operation:
- 1. Activate the word line.
- 2. Transistor in selected cell is turned ON
- 3. Cell and bit line share charges
- Capacitor > Threshold voltage, Bit line 1
- Capacitor < Threshold voltage, Bit line 0
- Refresh
- 1. Refresh Operation: Since the capacitor's charge leaks over time, the memory
- cell needs to be refreshed periodically by re-writing the stored data.



A single-transistor dynamic memory cell

Internal Organisation of a 2M x 8 Dynamic Memory Chip



Internal Organisation of a 2M x 8 Dynamic Memory Chip

- **Address lines are divided into two parts and multiplexed.**

- **Upper half of address:**

Loaded into Row Address Latch using Row Address Strobe (RAS).

- **Lower half of address:**

Loaded into Column Address Latch using Column Address Strobe(CAS).

Internal Organisation of a 2M x 8 Dynamic Memory Chip

- A **16-Mbit DRAM chip, configured as 2M X 8 memory organisation**
- **Cells are organized in the form of array, in rows and columns.**
- **The cells are organized as 4K X 4K array**
- **The 4096 cells in each row are divided into 512 groups of 8 cells**
- **That means a row can store 512 bytes of data**

  12 bits to select a row, and 9 bits to select a group (8 bits) in a row. Total of 21 bits.
- **Higher order 12 bits-row address and lower order 9 bits column address of a byte**
- **First apply the row address, RAS signal latches the row address. Then apply the**

. **column address, CAS signal latches the address.**
- **Timing of the memory unit is controlled by a specialized unit which generate RAS and CAS.**
- **This is asynchronous DRAM**

Internal Organisation of a 2M x 8 Dynamic Memory Chip

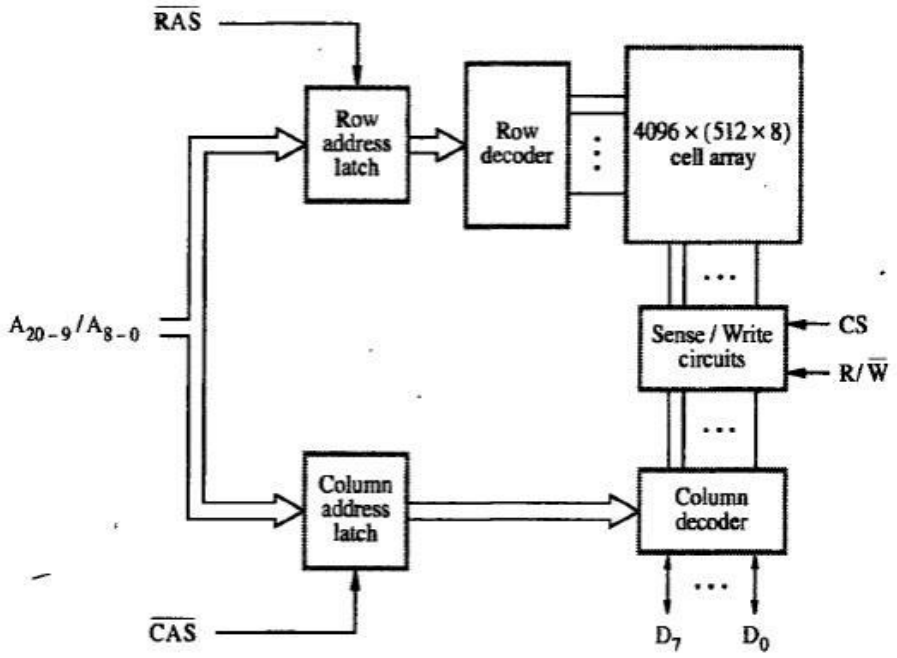
Design 16 M bit DRAM chip (2M X 8 memory organization)

$16\ 2^{20}$

$2^4\ 2^{20}$

2^{24}

$2^{12} x\ 2^{12}$ **Equivalent to 4K x 4K**



ROWS=2^{12}=4096

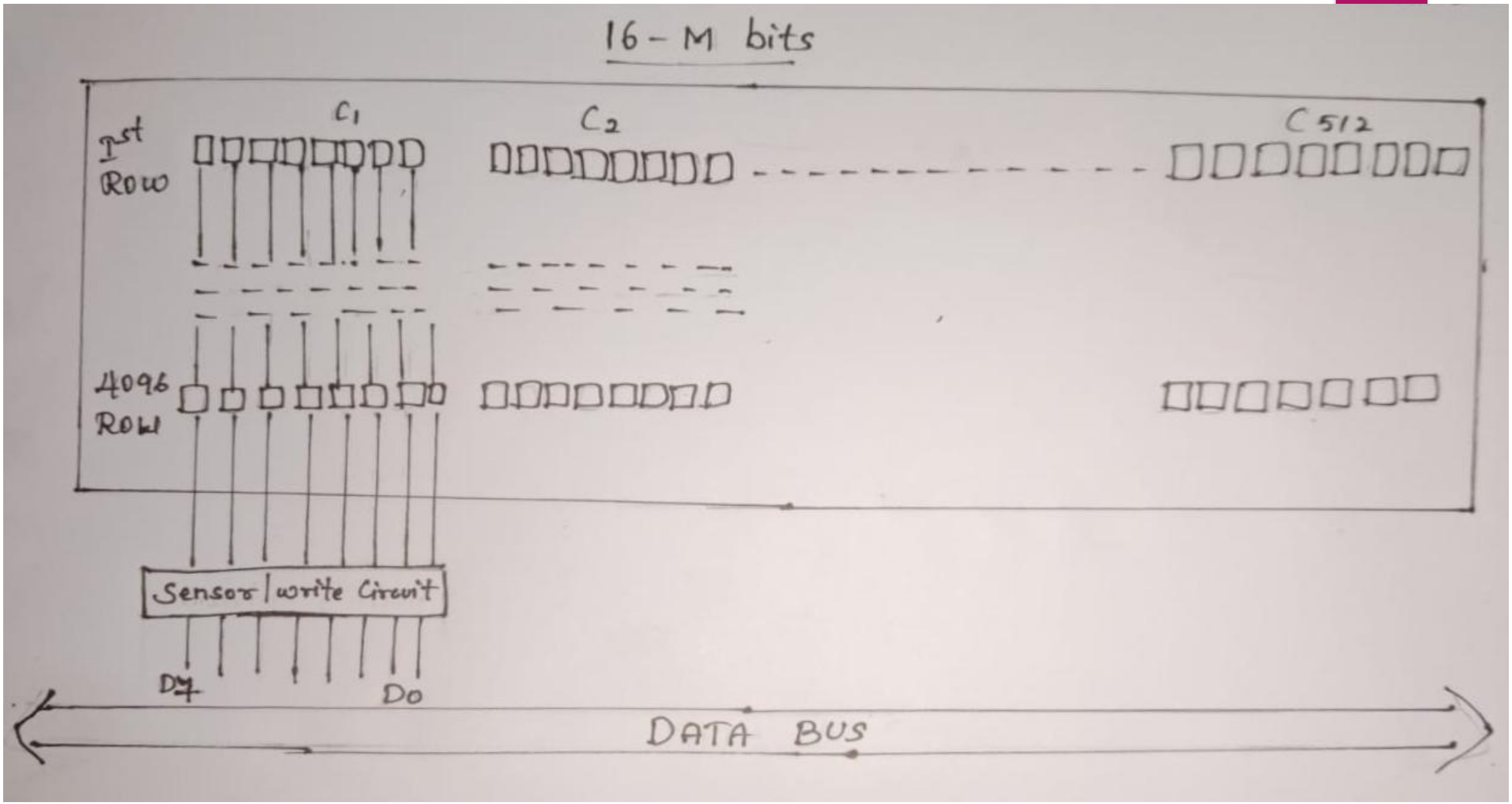
COLUMNS=4096/8=512 columns (8 bits)

No: of bits required for ROW Add. X=log2 2^{12} =12

No: of bits required for COLUMN Add. Y=log2 2^9 =9

Total address bit n=x(higher order) + y(lower order) **12+9=21 bits**

=A20-A9 + A8-A0


16 - M bits
C1
C2
C512
1st Row
4096 Row
Sensor / write Circuit
D7
D0
DATA BUS

FAST PAGE MODE

- When the DRAM in last slide is accessed, the contents of all 4096 cells in the selected row are sensed, but only 8 bits are placed on the data lines D7-0, as selected by A8-A0.
- Suppose if we want to access the consecutive bytes in the selected row. This can be done without having to reselect the row.
- Add a latch at the output of the sense circuits in each row.
- All the latches are loaded when the row is selected.
- Consecutive bytes can be transferred by applying consecutive column addresses under the control of successive CAS signals..
- This allows a block of data to be transferred at a much faster rate than random accesses.
- A small collection/group of bytes is usually referred to as a block. This transfer capability is referred to as the FAST PAGE MODE ACCESS
- Good for bulk transfer


thank
you