CBCS Scheme

USN | | | | | | | | | | |

15CS32

Third Semester B.E. Degree Examination, June/July 2018
Analog and Digital Electronics

Time: 3 hrs. Max. Marks: 80

Note: Answer any FIVE full questions, choosing one full question from each module.

Module-1

1 a. What is MOSFET? Name its types. Explain the construction of n-channel E-MOSFET. **(06 Marks)**

b. Compare JFET and MOSFET. **(05 Marks)**

c. Explain self-bias circuit for JFET. **(05 Marks)**

OR

2 a. Define: i) CMRR ii) Slew rate iii) PSRR iv) Bandwidth pertaining to OPAMP. **(06 Marks)**

b. Explain with schematics operation of relaxation oscillator with relevant waveforms. **(05 Marks)**

c. What are active filters? Explain active low pass filter. **(05 Marks)**

Module-2

3 a. Using Q-M method, simplify the expression $f(A, B, C, D) = \Sigma(0, 3, 5, 6, 7, 11, 14)$. **(06 Marks)**

b. Explain about positive and negative logic prove that positive 'OR' is equal to negative 'AND'. **(05 Marks)**

c. What are Hazards? Briefly describe about designing Hazard free circuit. **(05 Marks)**

OR

4 a. Give Sum-Of-Product (SOP) and Product-Of-Sum (POS) circuit for $f(A, B, C, D) = \sum m (6, 8, 9, 10, 11, 12, 13, 14, 15)$. **(06 Marks)**

b. Explain the verilog program structure. **(05 Marks)**

c. Design a logic circuit to provide an output when any two or three of four switches are closed. **(05 Marks)**

Module-3

5 a. Implement the following Boolean function using 4:1 multiplexer $F(A, B, C, D) = \sum m (0, 1, 2, 4, 6, 9, 12, 14)$. **(06 Marks)**

b. Construct 16:1 multiplexer using 4:1 and 2:1 multiplexer. **(05 Marks)**

c. What is a decoder? Give the circuit for 3:8 decoder. **(05 Marks)**

OR

6 a. What is a magnitude comparator? Explain a 1-bit comparator with truth table and circuit diagram. **(06 Marks)**

b. Briefly explain about parity generators and checkers. For a 3 bit message, give the expression for even parity bit. **(05 Marks)**

c. Compare and contrast PLA and PAL. **(05 Marks)**

Module-4

7 a. Explain the working of JK master slave flip-flop with a sketch, truth table and symbol. **(06 Marks)**

b. Give a brief account an flip flop as finite state machine. **(05 Marks)**

c. Briefly describe about sequential logic circuit. **(05 Marks)**

OR

8 a. Enumerate different types of shift registers. Explain Serial In Serial Out (SISO) register. **(06 Marks)**

b. Mention the applicators of shift registers. **(05 Marks)**

c. Using behavioral model write verilog HDL code for a 'D' flipflop with reset input. **(05 Marks)**

Module-5

9 a. Explain digital clock with block diagram. **(06 Marks)**

b. Design a 3 bit synchronous binary counter using JK flip flop. **(05 Marks)**

c. Mention different types of A/D converters and test its specifications. **(05 Marks)**

OR

10 a. Explain binary weighted resistor D/A converter. Mention its drawbacks. **(06 Marks)**

b. Describe about successive approximation type ADC. **(05 Marks)**

c. What is the resolution of a 12 bit D/A converter which uses a binary ladder, if the full scale output is +10V? **(05 Marks)**

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