# SIO Port
1.0

## Deprecation of SIO Port

The SIO Port component and its associated data sheet have been deprecated and replaced by the Pins component and data sheet. This was due to the creation of the Pins component to provide a more flexible solution for pins and ports. The SIO Port component remains in the Component Catalog to support legacy designs; however, it will be hidden by default for new designs, and it has been moved to a "deprecated" folder.

You should update your designs that use the SIO Port component to use the Pins component. To replace the component:

1. Based on the direction of your SIO port, select the appropriate Pins component from the catalog (Digital Input, Digital Output, or Digital Bidirectional), from under the **Ports and Pins** section. **Note** There is no longer a specific SIO port/pins component. A pin will become SIO in the following cases:
   - If the pin uses an Input and Hotswap is set to true.
   - If the pin uses an Input and the Threshold is set to anything except CMOS or LVTTL.
   - If the pin uses an Output and the Drive Current is set to a 25mA sink.
   - If the pin uses an Output and the Drive Level is Vref.
2. To have the terminals drawn as a bus, as they did on the SIO Port, go to the **Mapping** tab and check the "Display as Bus" option.
3. Configure the Pins component to match the SIO Port settings using the following conversion table:

| Port Parameter | Pins Component Equivalent Setting |
|---|---|
| AccessMode – SW | The equivalent setting would be to make the pins component Contiguous from the **Mapping** tab and to uncheck HW Connection from the **Pins/Type** tab (this will remove the terminals so that no connection is required in the schematic). |
| AccessMode - HW | The equivalent setting would be to make the pins component Non-Contiguous from the **Mapping** tab and to make sure HW Connection from the **Pins/Type** tab is checked so that terminals will be displayed on the schematic. |
| Direction | Select the pin(s) you want to change the direction of in the tree on the left side of the **Pins** tab. From the **Type** subtab you can use the check boxes to set the "direction" of the pins. |
| HiFreq | This is currently not settable in the new Pins component. It will always be set to High. It will be settable in a future release. If this needs to be set before then you will need to set the register directly. |

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| Port Parameter | Pins Component Equivalent Setting |
|---|---|
| InputBuffer | This can be set from the **Pins/Input** tab (as long as the pin type has Input or Bidirectional used). It is set based on the Threshold. If CMOS or LVTTL is chosen it will be Single Ended. All other selections will be Differential. **Note** LVTTL is not a valid option for SIOs. |
| OutputBuffer | This can be set from the **Pins/Output** tab (as long as the pin type has Output or Bidirectional used). It is set based on the Drive Level.<br>Regulated = Vref<br>Unregulated = Vddio |
| PowerOnResetState | This can be set from the **Reset** tab.<br>InDisabledOutHiZ = High-Z Analog<br>InEnabledOut1 = Pulled Up<br>InEnabledOut0 = Pulled Down<br>InEnabledOutHiZ = No longer supported |
| StandardLogic | This can be set from the **Pins/Input** tab (as long as the pin type has Input or Bidirectional used). It is now called Threshold. LVTTL is not a valid option for SIOs. |
| UseInterrupts | This is no longer used. Just set the interrupt mode for the pin directly. |
| VRefSelection/VTrip | These two options have now been combined into one.<br>If the pin direction is an input this is set on the **Pins/Input** tab by the Threshold option.<br>If the pin direction is an output this is set on the **Pins/Output** tab by the Drive Level option. |
| Width | From the **Pins** tab there is a "Num Pins" text box on the toolbar in the upper left of the tab. |
| Alias | From the **Pins** tab select a pin from the tree on the left side of the tab then either click the **Rename** button, press [**F2**], or double-click the pin in the tree. This will open a dialog where the alias can then be specified. |
| Pin Mode | This is now set from the **Pins/General** tab from the Drive Mode drop down list.<br>CMOS_Out = Strong Drive<br>Hi_Z = High Impedance Digital<br>ResPull_Up = Resistive Pull Up<br>ResPull_Down = Resistive Pull Down<br>ResPull_UpDown = Resistive Pull Up/Down<br>OpenDrain_Lo = Open Drain, Drives Low<br>OpenDrain_Hi = Open Drain Drives High |
| Slew Rate | This can be set from the **Pins/Output** tab (as long as the pin type has Output or Bidirectional used). |
| Hysteresis Enabled | This can be set from the **Pins/Input** tab (as long as the pin type has Input or Bidirectional used). It is controlled by a checkbox next to the Threshold. |
| Interrupt Mode | This can be set from the **Pins/Input** tab (as long as the pin type has Input or Bidirectional used). |

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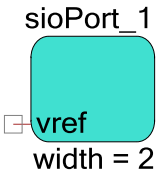
4. Delete your SIO Port and move your new Pins component to its old location.

   **Note** Once your pins are configured to be SIOs (they will get a pin outline in around the pin symbol in the tree) you will need to group them into a pair if your width was set to 2 before to get an equivalent functionality. To do this select your two adjacent SIO pins and click the Pair SIO button on the toolbar on the top of the **Pins** tab.
5. Right-click on your project in the Workspace Explorer and select **Update Components**; use the Component Update Tool to update the latest version of the cy_boot component.

# Features

- Regulated output level
- Reference generator per pair
- Supports hot swap




# General Description

An SIO port provides access to external data via an appropriately configured IO. Compared to GPIO's, SIO ports provide for regulated output levels, differential input levels, and hot swap capability. All ports allow for the creation of per-pin aliases which may be viewed in the PSoC Creator Pin Editor and used in the generated port APIs.

## When to use a SIO Port

Use a port when a design needs to generate or access an off-device signal. (Use an appropriate port for the type of the signal being accessed.)

# Input/Output Connections

This section describes the various input and output connections for the SIO port. An asterisk (*) in the list of I/O's states that the I/O may be hidden on the symbol under the conditions listed in the description of that I/O.

## i – Input *

Provides access to the digital input signal. This connection is only visible if all of the following criteria are met:

- AccessMode is PortAccessMode_HW
- Direction is PortDirection_Input or PortDirection_InOut

## o – Output *

Allows PSoC to drive a digital signal off the device. This connection is only visible if all of the following criteria are met:

- AccessMode is PortAccessMode_HW
- Direction is PortDirection_Output or PortDirection_InOut

## oe – Input *

Output enable determines whether the signal connected to the “o” terminal is actually driven off the device. This connection is only visible if all of the following criteria are met:

- AccessMode is PortAccessMode_HW
- Direction is PortDirection_Output or PortDirection_InOut

## irq – Output *

The signal driven out of this connection is high when the conditions under which the port should generate an interrupt have been met. Connect this to an Interrupt component to define the interrupt handler. This terminal is shown when the UseInterrupt parameter is set to true.

## vref – Analog InOut

One reference voltage will service two sio pins. The sio pair input buffer voltage levels are set by the VRefSelection and the VTrip selections.

### Input buffer Reference Voltage Selection

| VRefSelection | VTrip | Mode description |
|---|---|---|
| PortSIORefSel_VIO | PortSIOVTrip_Zero | 0.5*VIO |
| PortSIORefSel_VIO | PortSIOVTrip_One | 0.4*VIO |
| PortSIORefSel_VoHref | PortSIOVTrip_Zero | 0.5*Vref |
| PortSIORefSel_VoHref | PortSIOVTrip_One | Vref |

### Input and Output Configuration

| OutputBuffer | InputBuffer | Mode description |
|---|---|---|
| PortSIOOutput_Unregulated | PortSIOInput_SingleEnded | Single Ended Input buffer<br>Non-regulated Output buffer |
| PortSIOOutput_Unregulated | PortSIOInput_Differential | Differential Input buffer with<br>Non-regulated Output buffer |
| PortSIOOutput_Regulated | PortSIOInput_SingleEnded | Single Ended Input buffer<br>Regulated Output buffer |

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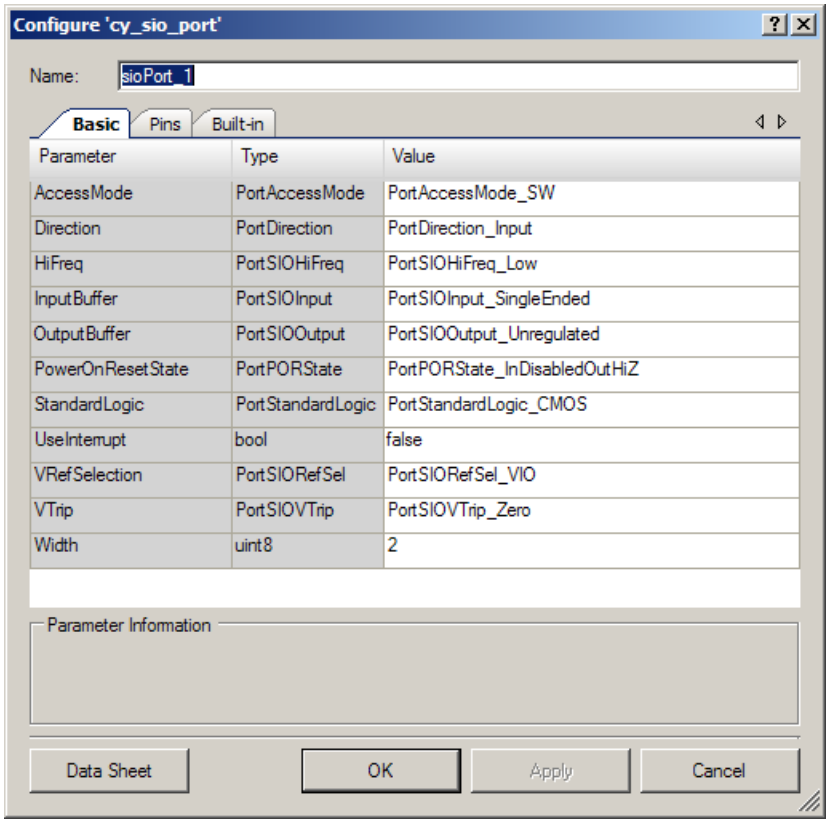
| | | |
|---|---|---|
| PortSIOOutput_Regulated | PortSIOInput_Differential | Differential Input buffer with Regulated Output buffer |

# Component Parameters

Drag an SIO port onto your design and double-click it to open the Configure dialog.

**Figure 1 Configure SIO port Dialog – Basic Tab**




## Basic Options

The following are the basic SIO port options.

### AccessMode

Determines how the port is accessible.

| AccessMode Value | Description |
|---|---|
| **PortAccessMode_SW** | The port may only be accessed via firmware (default). |

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| PortAccessMode_HW | The port may only be accessed via hardware. Hardware only ports do not have APIs callable from firmware. |

### Direction

Determines the direction of data flow.

| Direction Value | Description |
|---|---|
| **PortDirection_Input** | Allow the design to access digital signals coming in to the device (default). |
| PortDirection_Output | Allow the design to drive digital signals off the device. |
| PortDirection_InOut | Allow the design to access or drive a signal off device. |
| PortDirection_Bidirectional | Allow the design to access as well as drive a signal . |

### HiFreq

Regulated pull-up driver DC current setting (0=low current ~33uA for 10MHz with Cl=25pF, 1=high current ~59uA for 33MHz, 3.3V with Cl=10pF).

### InputBuffer

Allows the user to configure the input buffer of the SIO as single ended or differential. When single ended, the SIO acts like the GPIO with the reference as the VIO for the quadrant. When differential the reference voltage used is based on either the VIO for the quadrant or the routed vref to the SIO. The differential setting also allows for a multiplier to be applied to the reference voltage as well. Refer to the sio_vtrip and sio_refsel options for more details.

### OutputBuffer

Allows the user to configure the output of the SIO as unregulated or regulated. When unregulated the SIO acts like a GPIO where the reference used is the VIO for the quadrant. When regulated the reference used is the vref routed to the SIO port.

### PowerOnResetState

Specifies the power on reset state of the port. Legal values include:

- **InDisabledOutHiZ** (default)
- InEnabledOut1
- InEnabledOut0
- InEnabledOutHiZ.

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### StandardLogic

StandardLogic specifies the voltage level at which a device changes state.

| Direction Value | Description |
|---|---|
| **PortStandardLogic_CMOS** | The input buffer functions as a CMOS input buffer. This option is more power effiecient than LVTTL. (default). |
| PortStandardLogic_LVTTL | The input buffer functions as a LVTTL input buffer. |

### UseInterrupt

If true, the port may generate an interrupt. The “irq” terminal will become visible, and must be connected to an Interrupt component. The conditions under which an interrupt will be generated may be specified on the “Pins” tab. If false (default), the port will not generate an interrupt.

### VRefSelection

Select whether the voltage for the quadrant (VIO) (default) or the routed vref value (VoHref) are used as the reference for the input buffer when it is in differential mode.

### VTrip

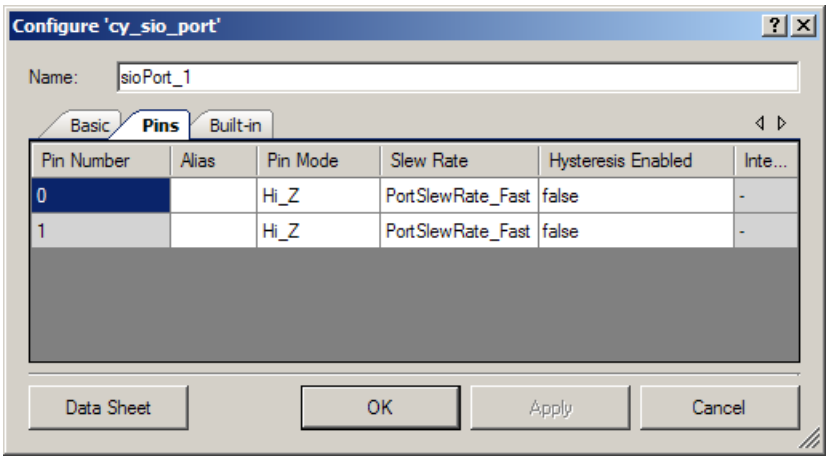
A value of 0 (PortSIOVTrip_Zero) will apply a 0.5 multiplier to the reference for the SIO when it is configured with a differential input. A value of 1 (PortSIOVTrip_One) will apply a 0.4 multiplier when the reference selected by sio_refsel is the VIO. If sio_refsel select VoHref then the multiplier is 1.

| Direction Value | Description |
|---|---|
| **PortSIOVTrip_Zero** | Applies a 0.5 multiplier to the reference for the SIO when it is configured with a differential input. (default). |
| PortSIOVTrip_One | Applies a 0.4 multiplier when the reference selected by sio_refsel is the VIO. If sio_refsel select VoHref then the multiplier is 1. |

### Width

Specifies the width in bits of the logical port (default is 2). Only 1 or 2 are valid.

**Figure 2 Configure SIO port Dialog – Pins Tab**




## Pins Options

The following options are set on a per pin basis.

### Alias

Allows an alias to be assigned to each pin in the port. The alias is presented in the Pin Editor and in the generated APIs for the port.

### Pin Mode

Allows for the configuration of the pin mode to the following:

**Table 1: Pin/ Drive Modes**

| Pin Mode | Description | High Output (Data = 1) | Low Output (Data = 0) | Input Buffer |
|---|---|---|---|---|
| CMOS_Out | Strong CMOS out | Strong 1 | Strong 0 | On |
| Hi_Z (default) | Hi – Z Digital – input buffer on | High-Z | High-Z | On |
| ResPull_Up | Resistive pull up | Res 1 (5k) | Strong 0 | On |
| ResPull_Down | Resistive pull down | Strong 1 | Res 0 (5k) | On |
| OpenDrain_Lo | Open Drain (drive lo) | High-Z | Strong 0 | On |
| OpenDrain_Hi | Open Drain (drive hi) | Strong 1 | High-Z | On |
| ResPull_UpDown | Resistive pull up/down | Res 1 (5k) | Res 0 (5k) | On |

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### Slew Rate

The slew rate of a device is the rate of change of its output. The options are fast (default) and slow.

### Hysteresis Enabled

Enables the SIO differential hysteresis for the pin when set to true. The default is false.

### Interrupt Mode

Indicates the conditions under which the pin will trigger the port interrupt. The interrupt mode can only be set if UseInterrupt is true. The available conditions are:

- **None** (default)
- Rising Edge
- Falling Edge
- On Change

## Placement

There is no placement specific information.

## Resources

All ports consume one physical pin, per bit of their width parameter.

## Application Programming Interface

Not applicable.

## Functional Description

Not applicable.

# DC and AC Electrical Characteristics

The following values are indicative of expected performance and based on initial characterization data.

## 5.0V/3.3V DC and AC Electrical Characteristics

| Parameter | Typical | Min | Max | Units | Conditions and Notes |
|---|---|---|---|---|---|
| Input | | | | | |
| Input Voltage Range | --- | | Vss to Vdd | V | |
| Input Capacitance | --- | | --- | pF | |
| Input Impedance | --- | | --- | Ω | |
| Maximum Clock Rate | --- | | 67 | MHz | |



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