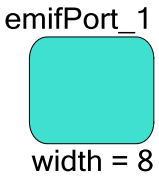
EMIF Port
1.0

Features



- Address and data selection
- Output enables for data selection
- Variable address width

General Description

The EMIF port provides access to external data via an appropriately configured I/O. All ports allow for the creation of per-pin aliases which may be viewed in the PSoC Creator Pin Editor and used in the generated port APIs.

When to use a Port

Use a port when a design needs to generate or access an off-device signal. Use an appropriate port for the type of signal being accessed. EMIF ports are optimized for external memory interface applications.

Input/Output Connections

This section describes the various input and output connections for the port components. An asterisk (*) in the list of I/O's states that the I/O may be hidden on the symbol under the conditions listed in the description of that I/O.

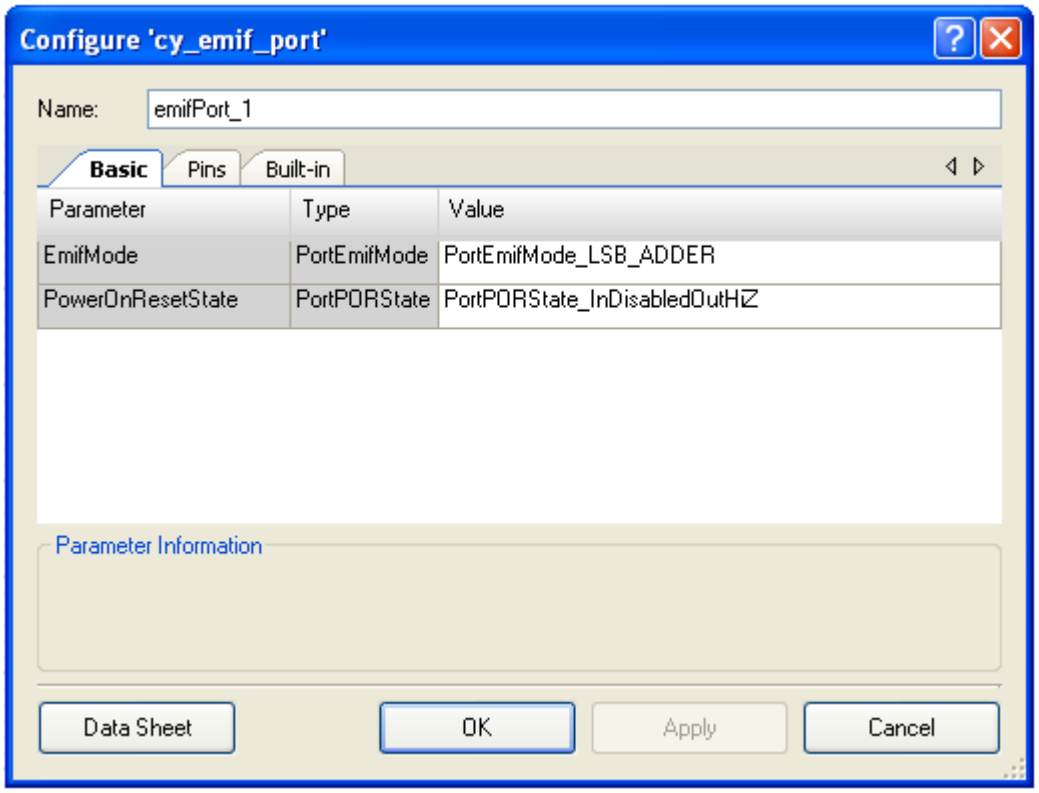
oe – Input *

Provides the ability for the design to drive the EMIF data output enable signal. This connection is only available when the EmifMode parameter is configured with the value PortEmifMode_MSB_DATA or PortEmifMode_LSB_DATA.

Component Parameters

Drag a Port onto your design and double-click it to open the Configure dialog.

Basic Tab



EmifMode

Indicates what mode the EMIF port should operate in. Available values include:

- MSB_ADDR – Most significant byte of an address
- MID_ADDR – Middle byte of an address
- **LSB_ADDR** (default) – Least significant byte of an address
- MSB_DATA – Most significant byte of the data
- LSB_DATA – Least significant byte of the data

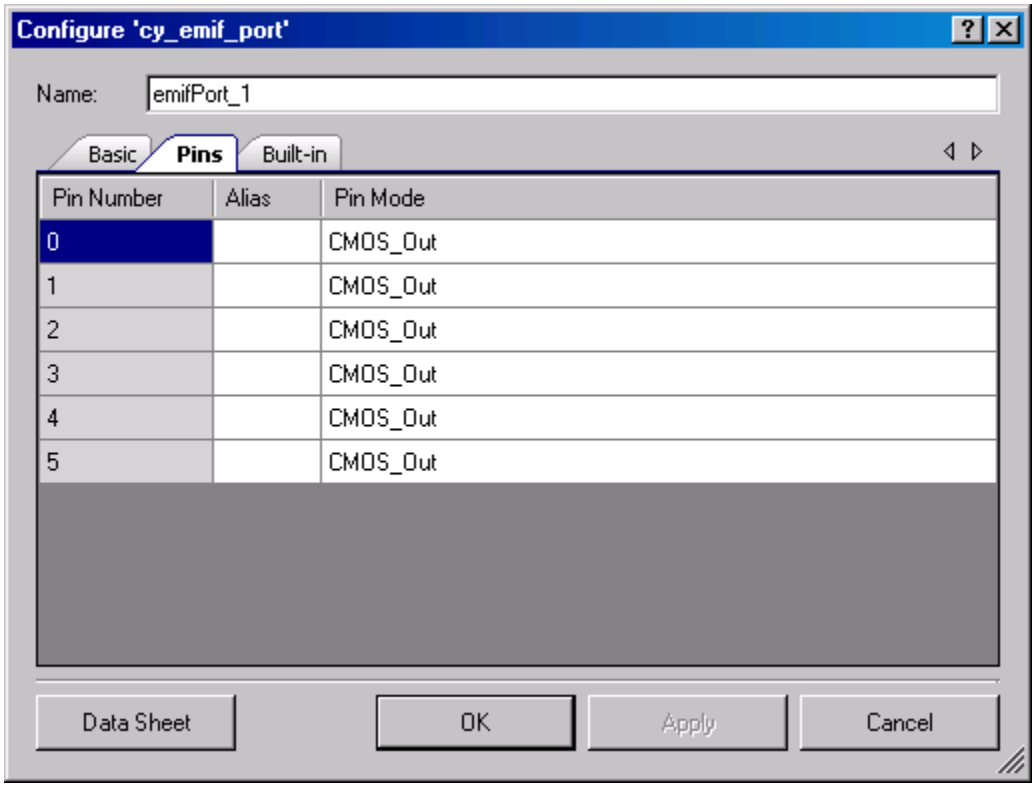
PowerOnResetState

Specifies the power on reset state of the port. Legal values include:

- **InDisabledOutHiZ** (default) – input disabled the output is Hi-Z
- InEnabledOut1 – input enabled the output is a logic one

- InEnabledOut0 – input enabled the output is a logic zero
- InEnabledOutHiZ – input enabled the output is Hi-Z

Pins Tab



Alias

Allows an alias to be assigned to each pin in the port. The alias is presented in the Pin Editor and in the generated APIs for the port.

Pin Mode

Allows for the configuration of the pin mode to the following:

- **CMOS_Out** (default) – CMOS out
- Hi_Z – Hi-Z digital
- ResPull_Up – resistive pull up
- ResPull_Down – resistive pull down
- ResPull_UpDown – resistive pull up/down
- OpenDrain_Lo – open drain low
- OpenDrain_Hi – open drain drive high

Resources

All ports consume one physical pin, per bit of their width parameter.

Application Programming Interface

Not applicable.

Functional Description

The EMIF uses the port interface to connect to external memory. When in EMIF mode, the ports directly pass to the pads (port pins) the address and data out from the PHUB and consequently the processor. Data reads from the EMIF pass through the port to the processor. Using the EMIF requires five ports for 24-bit addressing or four ports for 16-bit addressing. The EMIF may use any GPIO port for external memory interface. The control component of the EMIF does not require a complete port. The control signals are sent from the UDB to the ports over the digital signal interface (DSI).

DC and AC Electrical Characteristics

The following values are indicative of expected performance and based on initial characterization data. Unless otherwise specified in the tables below, all T_A = 25˚C, V_{dd} = 5.0V, Power HIGH, Op-Amp bias LOW, output referenced to Analog Ground = V_{ssa}.

5.0V/3.3V DC and AC Electrical Characteristics

Parameter	Typical	Min	Max	Units	Conditions and Notes
Input					
Input Voltage Range	---		Vss to Vdd	V	
Input Capacitance	---		---	pF	
Input Impedance	---		---	Ω	
Maximum Clock Rate	---		67	MHz	