Analog Net Constraint

1.50

Features

- Limits analog routing of a signal to a specific routing resource
- All terminals on the signal must connect directly to the routing resource

  Note Routing is strict. All of the devices connected to the net with the resource constraint must have a direct hardware connection to the resource. Refer to the Analog Routing Diagram in the applicable Technical Reference Manual (TRM), which is available from the Cypress website, www.cypress.com. If the resources do not have a hardware connection to the specified constraint, an error will occur.

General Description

The Analog Net Constraint Component allows you to define the route of the analog signal to which it is connected. This is an advanced feature that is not needed for most designs, and should be used with caution.

When to Use an Analog Net Constraint

The Analog Net Constraint should be used to manually control analog routing when strict control over the signal routing is required.

Input/Output Connections

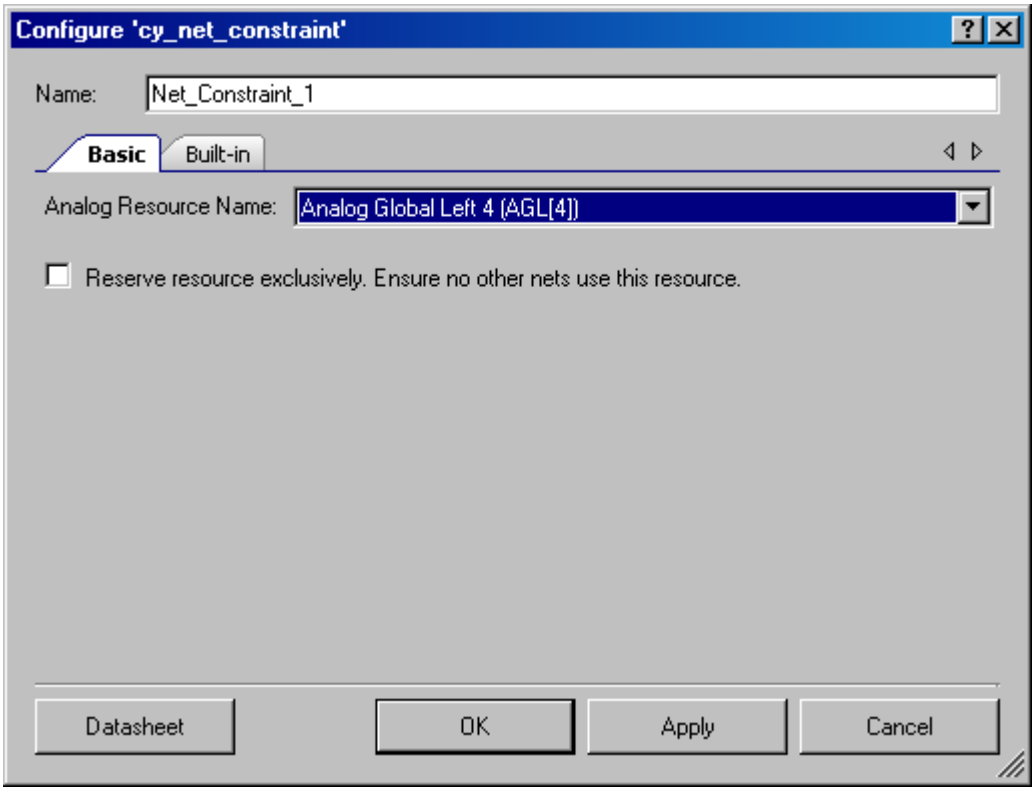
This section describes the various input and output connections for the Analog Net Constraint.

connect – Input /Output

Provides the connection to the analog signal to which the Analog Net Constraint applies.

Component Parameters

Drag an Analog Net Constraint onto your design and double-click it to open the **Configure** dialog.



The Analog Net Constraint provides the following parameters:

Analog Resource Name

The analog resource to assign to the connected signal. The default value, **Auto**, has no effect. The routing resource list depends on the selected family.

Exclusive Use

Allows the Analog Net Constraint to reserve the resource exclusively. If another Analog Net Constraint is configured to use the same analog resource, the net will not be short-circuited. An error will be generated instead.

Placement

The Analog Net Constraint consumes hardware resources because it specifies which hardware resource must be used by the router. It has no other placement specification.

Resources

The Analog Net Constraint Component causes the connected analog signal to consume the selected analog routing resource.

Functional Description

The following analog routing resource names are available for PSoC 3 and PSoC 5. Not every analog routing resource connects to every Component terminal. For detailed information about analog connectivity, refer to the applicable device datasheet and TRM. These documents are available on the Cypress website, www.cypress.com.

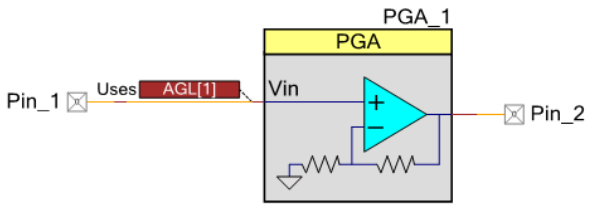
- Analog globals: AGL[0] – AGL[7], AGR[0] – AGR[7]
- Analog local bus: abusl0 – abusl3, abusr0 – abusr3
- Analog mux bus: AMUXBUSL, AMUXBUSR
- Combined left/right resources: AG[0] – AG[7], abus0 – abus3, AMUXBUS

When an Analog Net Constraint is present on a signal, the signal will be routed using **only** the specified resource. All of the Component terminals connected to the signal must have a direct connection to the routing resource. The analog placer might not be able to automatically ensure that Components are placed in way that satisfies Analog Net Constraints. Components connected to constrained signals should be placed manually.

Analog Net Constraint Example

In this example, the Analog Net Constraint is used to force a signal (Pin_1) on P4[4] to be routed on Analog Global Left 4.

Figure 1. Analog Net Constraint Example



Design-Wide Resources Settings

The following figures show settings in the Design-Wide Resources editors.

Figure 2. Directives Editor

Component (Signal) Name	Directive Type	Directive Value
\PGA_1:SC\	ForceComponentFixed	F(SC,0)

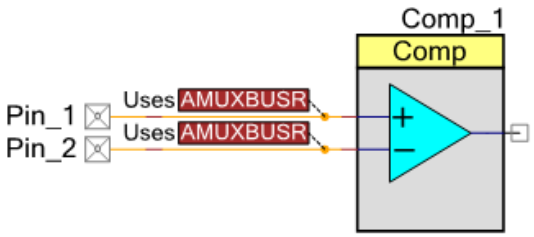
Figure 3. Pin Editor

Alias	Name	Pin	Lock
	Pin_1	P4[4]	☑
	Pin_2	P4[5]	☑

Short Circuit Example

If the same analog routing resource is specified for multiple signals that are not connected to an AMux, the signals will be connected to each other, which is not always the intended behavior.

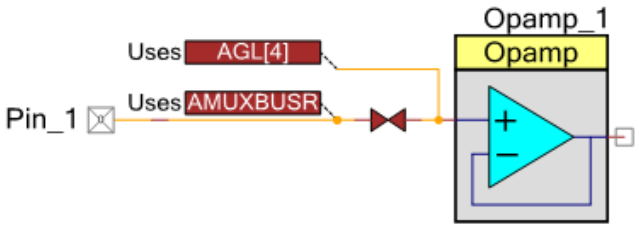
Figure 4. Short Circuit Example



Analog Net Tie Example

To apply multiple constraints to a signal or constrain a subset of the connections in a signal, use a Net Tie Component. Refer to the Net Tie Component datasheet for details (available from the PSoC Creator Component Catalog).

Figure 5. Net Tie Example



Component Changes

This section lists the major changes in the Component from the previous version.

Version	Description of Changes	Reason for Changes / Impact
1.50.c	Minor datasheet edits.	
1.50.b	The Component was made visible for PSoC 6.	
1.50.a	Minor datasheet edits and updates	