

Stay Awake

1.50



Features

- Use routes that remain active during sleep

General Description

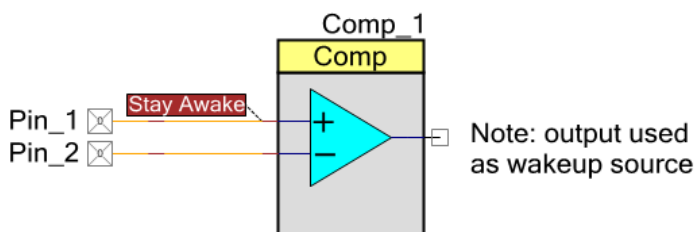
On certain devices, to avoid signal integrity issues, specific analog blocks disconnect their terminals when the device goes to sleep. This also disconnects any routes (static or dynamic) that use the block terminal as a via.

You can identify those routes that must stay awake during device sleep using the Stay Awake component, which has a single connection and no parameters. The net to which the Stay Awake component is attached is routed without using the affected analog block terminals.

When to Use a Stay Awake

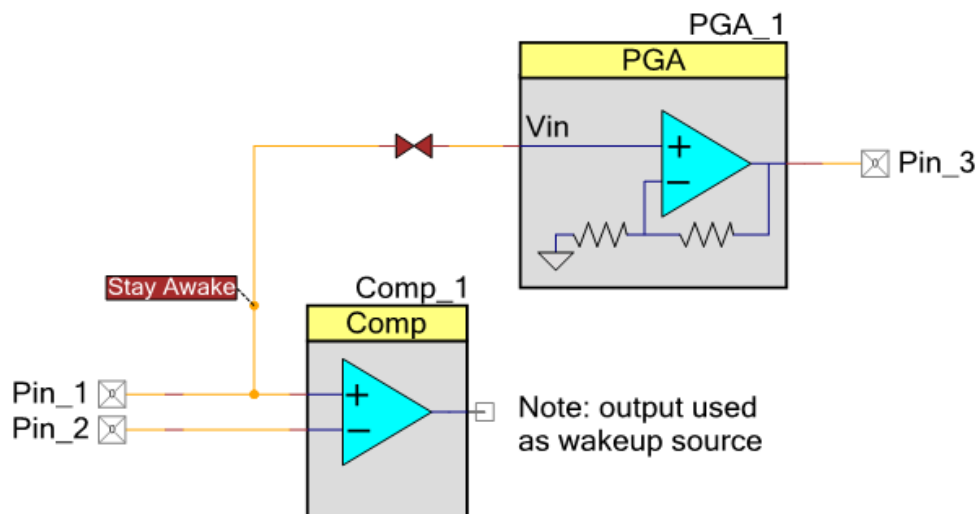
You can use a Stay Awake component to establish a route where a net needs to remain connected while the device is asleep or hibernating.

Example 1



In those cases where a net needs to remain connected while the device is asleep, but also must connect to an affected analog block terminal, use a Net Join component to isolate the routing restriction.

Example 2



The SC/CT block is used for, among other things, the PGA. When routing a net connected to Stay Awake, connections to the SC/CT block are not allowed. This can lead to a failure to route if the connection is to the SC/CT. See [Example 2](#) to deal with this issue.

Input/Output Connections

This section describes the various input and output connections for the Stay Awake component.

connect – Input/Output

Connects to a signal to prevent it from disconnecting when the device goes to sleep.

Resources

The connected terminal is consumed by the Stay Awake component.

Functional Description

When routing a net connected to the Stay Awake, the connections to the SC/CT node (used for PGA and other components) and SAR are not allowed.

This can lead to failure to route if the connection is to the SC/CT or SAR block.

Component Changes

This section lists the major changes in the component from the previous version.

| Version | Description of Changes |
|---------|---|
| 1.50.i | Minor datasheet edits. |
| 1.50.h | The component was made visible for PSoC 6. |
| 1.50.g | Minor datasheet edits. |
| 1.50.f | Minor datasheet edits. |
| 1.50.e | Minor datasheet edits and updates. |
| 1.50.d | Release to the internet. |
| 1.50.c | Cosmetic change; updated the symbol and diagrams |
| 1.50.b | Cosmetic change removing wire guide from terminal |
| | Updated datasheet to clarify usage |
| 1.50.a | Minor datasheet edits and updates |

© Cypress Semiconductor Corporation, 2010-2017. This document is the property of Cypress Semiconductor Corporation and its subsidiaries, including Spansion LLC ("Cypress"). This document, including any software or firmware included or referenced in this document ("Software"), is owned by Cypress under the intellectual property laws and treaties of the United States and other countries worldwide. Cypress reserves all rights under such laws and treaties and does not, except as specifically stated in this paragraph, grant any license under its patents, copyrights, trademarks, or other intellectual property rights. If the Software is not accompanied by a license agreement and you do not otherwise have a written agreement with Cypress governing the use of the Software, then Cypress hereby grants you a personal, non-exclusive, nontransferable license (without the right to sublicense) (1) under its copyright rights in the Software (a) for Software provided in source code form, to modify and reproduce the Software solely for use with Cypress hardware products, only internally within your organization, and (b) to distribute the Software in binary code form externally to end users (either directly or indirectly through resellers and distributors), solely for use on Cypress hardware product units, and (2) under those claims of Cypress's patents that are infringed by the Software (as provided by Cypress, unmodified) to make, use, distribute, and import the Software solely for use with Cypress hardware products. Any other use, reproduction, modification, translation, or compilation of the Software is prohibited.

TO THE EXTENT PERMITTED BY APPLICABLE LAW, CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS DOCUMENT OR ANY SOFTWARE OR ACCOMPANYING HARDWARE, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. To the extent permitted by applicable law, Cypress reserves the right to make changes to this document without further notice. Cypress does not assume any liability arising out of the application or use of any product or circuit described in this document. Any information provided in this document, including any sample design information or programming code, is provided only for reference purposes. It is the responsibility of the user of this document to properly design, program, and test the functionality and safety of any application made of this information and any resulting product. Cypress products are not designed, intended, or authorized for use as critical components in systems designed or intended for the operation of weapons, weapons systems, nuclear installations, life-support devices or systems, other medical devices or systems (including resuscitation equipment and surgical implants), pollution control or hazardous substances management, or other uses where the failure of the device or system could cause personal injury, death, or property damage ("Unintended Uses"). A critical component is any component of a device or system whose failure to perform can be reasonably expected to cause the failure of the device or system, or to affect its safety or effectiveness. Cypress is not liable, in whole or in part, and you shall and hereby do release Cypress from any claim, damage, or other liability arising from or related to all Unintended Uses of Cypress products. You shall indemnify and hold Cypress harmless from and against all claims, costs, damages, and other liabilities, including claims for personal injury or death, arising from or related to any Unintended Uses of Cypress products.

Cypress, the Cypress logo, Spansion, the Spansion logo, and combinations thereof, WICED, PSoC, CapSense, EZ-USB, F-RAM, and Traveo are trademarks or registered trademarks of Cypress in the United States and other countries. For a more complete list of Cypress trademarks, visit cypress.com. Other names and brands may be claimed as property of their respective owners.

