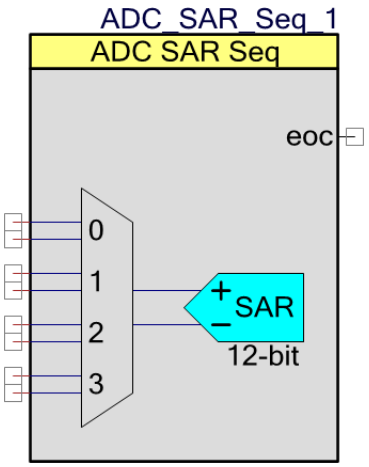
Sequencing Successive Approximation ADC (ADC_SAR_Seq)

2.10



Features

- Supports PSoC 5LP devices
- Selectable resolution (8, 10 or 12 bit) and sample rate (up to 1 Msps)
- Scans up to 64 single ended or 32 differential channels automatically, or just a single input

  Note Only GPIOs can be connected to the channel inputs. The actual maximum number of input channels depends on the number of routable analog GPIOs available on a specific PSoC part and package.

General Description

The Sequencing SAR ADC Component enables makes it possible for you to configure and then use the different operational modes of the SAR ADC on PSoC 5LP. You also have schematic level and firmware level support for seamless use of the Sequencing SAR ADC in PSoC Creator designs and projects. You are able to configure multiple analog channels that are automatically scanned with the results placed in individual SRAM locations.

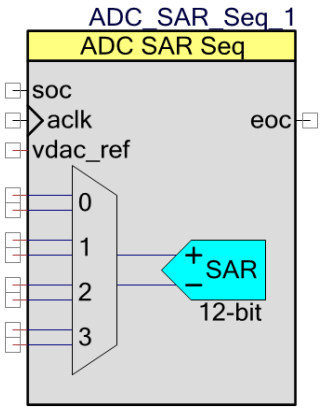
When to Use the ADC_SAR_Seq

The Sequencing SAR ADC is commonly used in high sample rate systems where multiple channels must be sampled without CPU intervention until all channels are sampled.

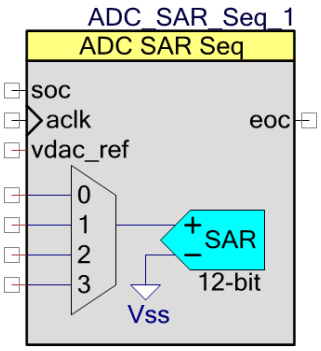
Input/Output Connections

This section describes the input and output connections for the ADC_SAR_Seq. An asterisk (*) in the list of I/Os indicates that the I/O may be hidden on the symbol under the conditions listed in the description of that I/O.

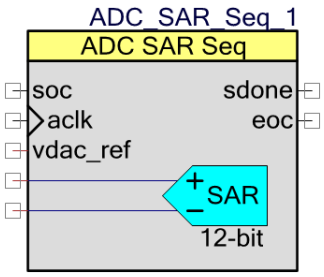
Differential Inputs



Single-ended inputs



Differential inputs – 1 channel (sdone is visible)



+Input – Analog

This input is the positive analog signal input to the ADC_SAR_Seq. The conversion result is a function of the +Input signal minus the voltage reference. The voltage reference is either the Input signal or V_{SSA}.

–Input – Analog *

When shown, this optional input is the negative analog signal (or reference) input to the ADC_SAR_Seq. The conversion result is a function of +Input minus –Input. You see this pin when you set the **Input Range** parameter to one of the differential modes.

vdac_ref – Input *

The VDAC reference (vdac_ref) is an optional pin. To see it, select **Vssa to VDAC*2 (Single Ended)** or **0.0 +/- VDAC (Differential)** input range; otherwise, this I/O is hidden.

Note You can only connect this pin to a VDAC Component output. Do not connect it to any other signal.

soc – Input *

The start of conversion (soc) is an optional pin. You see it if you select the **Hardware trigger** sample mode. A rising edge on this input starts an ADC conversion. The first **soc** rising edge should be generated at least 10 us after the Component is started to guarantee reference and

pump voltage stability. You can connect the output of a PWM Component to this input. It can also be connected to any GPIO pin or a UDB. This signal should be synchronized to the ADC_SAR_Seq clock and must be at least one ADC_SAR_Seq clock cycle wide.

This input is hidden if you set the **Sample Mode** parameter to **Free-running** or **Software trigger**.

aclk – Input *

You see this optional pin if you set the **Clock Source** parameter to **External**; otherwise, the pin is hidden. This clock determines the conversion rate as a function of the conversion method and resolution.

eoc – Output

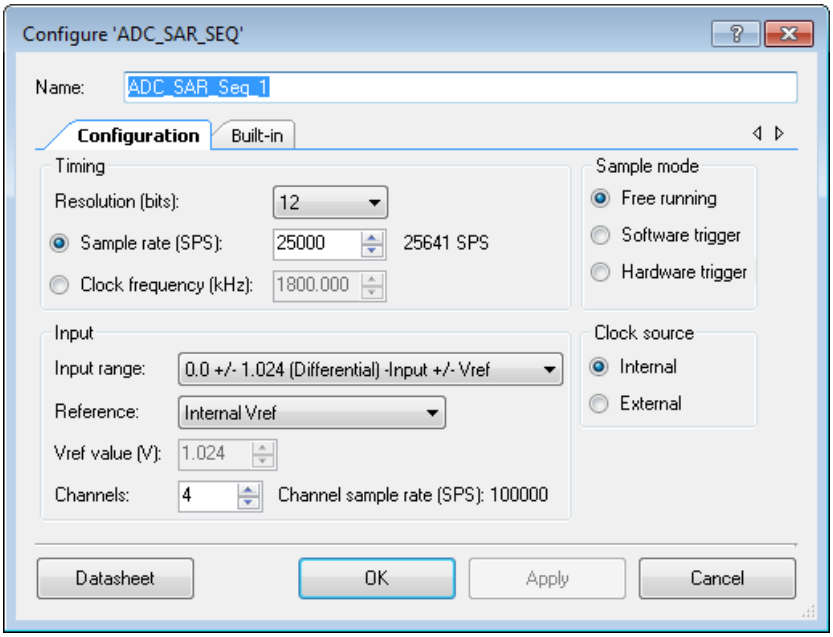
A rising edge on the end of conversion (eoc) output means that one conversion cycle is complete. At this moment, conversion results for all channels are ready to be read from the SRAM. An internal interrupt is also connected to this signal, or you may connect your own interrupt.

sdone – Output *

A rising edge on this output means that sampling is complete. This is a direct connection from EOS output of the ADC SAR Component. This signal is only visible when the Component is configured for one channel operation.

Component Parameters

Drag an ADC_SAR_Seq Component onto your design and double-click it to open the **Configure** dialog.



The ADC_SAR_Seq has the following parameters. The option shown in bold is the default.

Timing

Resolution (bits)

Sets the resolution of the ADC_SAR_Seq.

Resolution	Description
12	Sets resolution to 12 bits
10	Sets resolution to 10 bits
8	Sets resolution to 8 bits

Sample Rate (SPS)

This parameter shows the sample rate in samples per second (SPS) for all channels. It is automatically calculated based on the clock frequency and number of channels. Channel Sample Rate is shown near the Channels numeric up-down control.

The actual sample rate may differ based on the available clock speed and divider range. It is shown on the right side from selected sample rate.

The actual sample rate also depends on a sample mode and availability of the data bus for DMA transfer. Refer to the Functional Description section for details on how to calculate the number of clocks required for sampling.

Clock Frequency (kHz)

This text box is read-only by default (always grayed out) that displays the required clock rate for the selected operating conditions: resolution and conversion rate. It is updated when either or both of these conditions change. It can be changed if **Clock Source** is set to Internal. Clock frequency can be anywhere between 1 MHz and 18 MHz. The duty cycle should be 50 percent. Make the minimum pulse width greater than 25.5 ns. PSoC Creator generates an error during the build process if the clock does not fall within these limits. In there is an error, change the Master Clock in the Design-Wide Resources Clock Editor.

Sample mode

This parameter determines how the ADC operates.

SampleMode	Description
Free Running	ADC_SAR_Seq runs continuously. Use the ADC_SAR_Seq_StartConvert() function to start and the ADC_SAR_Seq_StopConvert() function to stop continuous conversions.
Software trigger	Calling of the ADC_SAR_Seq_StartConvert() starts a single cycle of conversion for all channels
Hardware trigger	A rising-edge pulse on the SOC pin starts a single cycle of conversion for all channels

Input

Input Range

This parameter configures the ADC for a given input range. The analog signals connected to the PSoC must be between V_{SSA} and V_{DDA} regardless of the input range settings.

InputRange	Description
0.0 to 2.048V (Single Ended) 0 to Vref*2	When using the internal reference (1.024 V), the usable input range is 0.0 to 2.048 V. The ADC is configured to operate in a single-ended input mode with –Input connected internally to Vrefhi_out. If you are using an external reference voltage, the usable input range is 0.0 to Vref*2.
Vssa to Vdda (Single Ended)	This mode uses the $V_{DDA}/2$ reference; the usable input range covers the full analog supply voltage. The ADC is put in a single-ended input mode with –Input connected internally to Vrefhi_out. If you are using an external reference voltage, the usable input range is 0.0 to Vref*2.
Vssa to VDAC*2 (Single Ended)	This mode uses the VDAC reference, which should be connected to the vdac_ref pin. The usable input range is Vssa to VDAC*2 volts. The ADC is configured to operate in a single-ended input mode with –Input connected internally to Vrefhi_out.

InputRange	Description
0.0 ± 1.024V (Differential) –Input ± Vref	This mode is configured for differential inputs. When using the internal reference (1.024 V), the input range is –Input ± 1.024 V. For example, if –Input is connected to 2.048 V, the usable input range is 2.048 ± 1.024 V or 1.024 to 3.072 V. For systems in which both single-ended and differential signals are scanned, connect –Input to Vssa when scanning a single-ended input. You can use an external reference to provide a wider operating range. You can calculate the usable input range with the same equation, –Input ± Vref.
0.0 ± Vdda (Differential) –Input ± Vdda	This mode is configured for differential inputs and is ratiometric with the supply voltage. The input range is –Input ± Vdda. For systems in which both single-ended and differential signals are scanned, connect –Input to Vssa when scanning a single-ended input. If you are using an external reference voltage, the usable input range is –Input ± Vref.
0.0 ± Vdda/2 (Differential) –Input ± Vdda/2	This mode is configured for differential inputs and is ratiometric to the supply voltage. The input range is –Input ± Vdda/2. For systems in which both single-ended and differential signals are scanned, connect –Input to Vssa when scanning a single-ended input. If you are using an external reference voltage, the usable input range is –Input ± Vref.
0.0 ± VDAC (Differential) –Input ± VDAC	This mode is configured for differential inputs and uses the VDAC reference, which should be connected to the vdac_ref pin. The input range is –Input ±VDAC. For systems in which both single-ended and differential signals are scanned, connect –Input to Vssa when scanning a single-ended input.

Reference

This parameter selects the switches for reference configuration for the ADC_SAR.

ADC_Reference	Allowed Clock Frequency (MHz)	Description
Internal Vref	1 ~ 1.6 MHz	Uses the internal reference. This clock frequency range is valid with all input ranges except “0.0 ± Vdda”. Uses the Internal Vref, bypassed option for higher clock frequency.
	1 ~ 9 MHz	Uses the internal reference. This clock frequency range is valid with “0.0 ± Vdda” input range.
Internal Vref, bypassed	1 ~ 18 MHz	Uses the internal reference. You must place a bypass capacitor on pin P0[2] [1] for SAR1 or on pin P0[4] [1] for SAR0. This mode is not applicable with “0.0 ± Vdda” input range.
External Vref	1 ~ 18 MHz	Uses an external reference on pin P0[2] for SAR1 or on pin P0[4] for SAR0.

1 The use of an external bypass capacitor is recommended if the internal noise caused by digital switching exceeds an application's analog performance requirements. To use this option, configure either port pin P0[2] or P0[4] as an analog HI-Z pin and connect an external capacitor with a value between 0.01 µF and 10 µF.

Note The same internal reference is used for ADC_SAR and for ADC_DelSig Components. If both types of the ADC need to work with an internal reference simultaneously, use the **Internal Vref, bypassed** option for the best performance.

Voltage Reference

The voltage reference is used for the ADC count to voltage conversion functions that is discussed in the Application Programming Interface section. This parameter is read-only when using the internal reference. When using an external reference, change this value to match the external reference voltage.

- When selecting input range **Vssa to Vdda**, **-Input +/- Vdda**, or **-Input +/- Vdda/2**, the value is derived from the V_{DDA} setting in System tab of the Design Wide Resources (DWR).
- When selecting the input range **Vssa to VDAC*2** or **–Input +/- VDAC**, type the VDAC supply voltage value.

Note The input range and reference voltage is limited by the V_{DDA} voltage.

Clock Source

This parameter allows you to select either a clock that is internal to the ADC_SAR_Seq module or an external clock.

ADC_Clock	Description
Internal	Use the internal clock of the ADC_SAR_Seq
External	Use an external clock. The clock source can be analog, digital, or generated by another Component.

Application Programming Interface

Application Programming Interface (API) routines allow you to configure the Component using software. This table lists and describes the interface to each function. The following sections discuss each function in more detail.

By default, PSoC Creator assigns the instance name " ADC_SAR_Seq_1" to the first instance of a Component in a given design. You can rename the instance to any unique value that follows the syntactic rules for identifiers. The instance name becomes the prefix of every global function name, variable, and constant symbol. For readability, the instance name used in the following table is "ADC_SAR_Seq".

Functions

Function	Description
ADC_SAR_Seq_Start()	Powers up the ADC_SAR_Seq and resets all states
ADC_SAR_Seq_Stop()	Stops ADC_SAR_Seq conversions and reduces the power to the minimum
ADC_SAR_Seq_SetResolution()	Sets the resolution of the ADC_SAR_Seq
ADC_SAR_Seq_StartConvert()	Starts conversions
ADC_SAR_Seq_StopConvert()	Stops conversions
ADC_SAR_Seq_IRQ_Enable()	An internal IRQ is connected to the eoc. This API enables the internal ISR
ADC_SAR_Seq_IRQ_Disable()	An internal IRQ is connected to the eoc. This API disables the internal ISR
ADC_SAR_Seq_IsEndConversion()	Returns a nonzero value if conversion is complete
ADC_SAR_Seq_GetAdcResult()	Returns a signed 16-bit conversion result available in the ADC SAR Data Register not the result buffer
ADC_SAR_Seq_GetResult16()	Returns a signed16-bit conversion result for specified channel
ADC_SAR_Seq_SetOffset()	Sets the offset of the ADC_SAR_Seq
ADC_SAR_Seq_SetScaledGain()	Sets the ADC_SAR_Seq gain in counts per 10 volts
ADC_SAR_Seq _CountsTo_Volts()	Converts ADC_SAR_Seq counts to floating-point volts
ADC_SAR_Seq_CountsTo_mVolts()	Converts ADC_SAR_Seq counts to millivolts
ADC_SAR_Seq_CountsTo_uVolts()	Converts ADC_SAR_Seq counts to microvolts
ADC_SAR_Seq_Sleep()	Stops ADC_SAR_Seq operation and saves the user configuration
ADC_SAR_Seq_Wakeup()	Restores and enables the user configuration
ADC_SAR_Seq_Init()	Initializes the default configuration provided with the customizer
ADC_SAR_Seq_Enable()	Enables the clock and power for the ADC_SAR_Seq
ADC_SAR_Seq_SaveConfig()	Saves the current user configuration
ADC_SAR_Seq_RestoreConfig()	Restores the user configuration

void ADC_SAR_Seq_Start(void)

Description: This is the preferred method to begin Component operation. ADC_SAR_Seq_Start() sets the initVar variable, calls the ADC_SAR_Seq _Init() function, and then calls the ADC_SAR_Seq_Enable() function. It is not recommended to call this API a second time without stopping the Component first.

Side Effects: If the initVar variable is already set, this function only calls the ADC_SAR_Seq_Enable() function.

void ADC_SAR_Seq_Stop(void)

Description: Stops ADC_SAR_Seq conversions and reduces the power to the minimum.

Note This API does not power down the ADC, but reduces power to a minimum level. This device has a defect that causes connections to several analog resources to be unreliable when the device is not powered. The unreliability manifests itself in silent failures (for example, unpredictable bad results from analog Components) when the Component using that resource is stopped.

void ADC_SAR_Seq_SetResolution(uint8 resolution)

Description: Sets the resolution for the GetResult16() and GetAdcResult() APIs.

Parameters: uint8 resolution: Resolution setting

Parameters Name	Value	Description
ADC_SAR_Seq_ADC_BITS_12	12	Sets resolution to 12 bits.
ADC_SAR_Seq_ADC_BITS_10	10	Sets resolution to 10 bits.
ADC_SAR_Seq_ADC_BITS_8	8	Sets resolution to 8 bits.

Side Effects: You cannot change the ADC resolution during a conversion cycle. The recommended best practice is to stop conversions with ADC_SAR_SeqStopConvert(), change the resolution, then restart the conversions with ADC_SAR_Seq_StartConvert().

If you decide not to stop conversions before calling this API, use ADC_SAR_Seq_IsEndConversion() to wait until conversion is complete before changing the resolution.

If you call ADC_SAR_Seq_SetResolution() during a conversion, the resolution does not change until the current conversion is complete. Data will not be available in the new resolution for another 6 + “New Resolution(in bits)” clock cycles. You may need add a delay of this number of clock cycles after ADC_SAR_Seq_SetResolution() is called before data is valid again.

Affects ADC_SAR_Seq_CountsTo_Volts(), ADC_SAR_Seq_CountsTo_mVolts(), and ADC_SAR_Seq_CountsTo_uVolts() by calculating the correct conversion between ADC_SAR_Seq counts and the applied input voltage. Calculation depends on resolution, input range, and voltage reference.

void ADC_SAR_Seq_StartConvert(void)

Description: This forces the ADC to initiate a conversion. In free-running mode, the ADC_SAR_Seq runs continuously. In software trigger mode, the function also acts as a software version of the SOC and every conversion must be triggered by ADC_SAR_Seq_StartConvert(). In Hardware trigger mode this function is unavailable.

Side Effects: Calling ADC_SAR_Seq_StartConvert() disables the external SOC pin.

void ADC_SAR_Seq_StopConvert(void)

Description: This forces the ADC_SAR_Seq to stop conversions. If a conversion is currently executing, that conversion completes, but no further conversions happen. This only applies to free-running mode.

Side Effects: In free-running and software trigger mode, this function sets a software version of the SOC to low level and switches the SOC source to hardware SOC input (Hardware trigger).

void ADC_SAR_Seq_IRQ_Enable(void)

Description: This enables interrupts to occur at the end of a conversion. Global interrupts must also be enabled for the ADC interrupts to occur. To enable global interrupts, call the enable global interrupt macro "`CyGlobalIntEnable;`" in your *main.c* file before enabling any interrupts.

Side Effects: Enables interrupts to occur. Reading the result clears the interrupt.

void ADC_SAR_Seq_IRQ_Disable(void)

Description: Disables interrupts at the end of a conversion.

uint32 ADC_SAR_Seq_IsEndConversion(uint8 retMode)

Description: Immediately returns the status of the conversion or does not return (blocking) until the conversion completes, depending on the retMode parameter.

Parameters: uint8 retMode: Check conversion return mode. This table describes the available options.

Options	Description
ADC_SAR_Seq_RETURN_STATUS	Immediately returns the status. If the value returned is zero, the conversion is incomplete, and this function should be retried until a nonzero result is returned.
ADC_SAR_Seq_WAIT_FOR_RESULT	Does not return a result until the ADC_SAR_Seq conversion is complete.

Return Value: uint32: If a nonzero value is returned, the last conversion is complete. If the returned value is zero, the ADC_SAR_Seq is still calculating the last result.

Side Effects: This function reads the end of conversion status, which is cleared on read.

int16 ADC_SAR_Seq_GetAdcResult(void)

Description: Gets the data available in the SAR DATA register, not the results buffer.

Return Value: int16: The last ADC conversion result.

Side Effects: Converts the ADC counts to the 2's complement form.

int16 ADC_SAR_Seq_GetResult16(uint16 chan)

Description: Returns the conversion result for channel "chan".

Parameters: uint16 chan: The ADC channel in which to return the result. The first channel is 0 and the last channel is the total number of channels – 1.

Return Value: int16: Returns converted data as a signed 16-bit integer

Side Effects: Converts the ADC counts to the 2's complement form.

void ADC_SAR_Seq_SetOffset(int32 offset)

Description: Sets the ADC_SAR_Seq offset, which is used by ADC_SAR_Seq_CountsTo_Volts(), ADC_SAR_Seq_CountsTo_mVolts(), and ADC_SAR_Seq_CountsTo_uVolts(), to subtract the offset from the given reading before calculating the voltage conversion.

Parameters: int32 offset: This value is measured when the inputs are shorted or connected to the same input voltage.

Side Effects: Affects ADC_SAR_Seq_CountsTo_Volts(), ADC_SAR_Seq_CountsTo_mVolts(), and ADC_SAR_Seq_CountsTo_uVolts() by subtracting the given offset.

void ADC_SAR_Seq_SetScaledGain(int32 adcGain)

Description: Sets the ADC_SAR_Seq gain in counts per 10 volts for the voltage conversion functions that follow. This value is set by default by the reference and input range settings. It should only be used to further calibrate the ADC_SAR_Seq with a known input or if the ADC_SAR_Seq is using an external reference. To calibrate the gain, supply close to reference voltage to ADC inputs and measure it by multimeter. Calculate the gain coefficient using following formula.

$$adcGain = \frac{counts \times 10}{V_{measured}}$$

Where the **counts** is returned from ADC_SAR_Seq_GetResult16() value, $V_{measued}$ – measured by multimeter voltage in volts.

Parameters: int32 adcGain: ADC_SAR_Seq gain in counts per 10 volts

Side Effects: Affects ADC_SAR_Seq_CountsTo_Volts(), ADC_SAR_Seq_CountsTo_mVolts(), ADC_SAR_Seq_CountsTo_uVolts() by supplying the correct conversion between ADC counts and the applied input voltage.

float32 ADC_SAR_Seq_CountsTo_Volts(int16 adcCounts)

Description: Converts the ADC_SAR_Seq output to volts as a floating-point number. For example, if the ADC_SAR_Seq measured 0.534 volts, the return value would be 0.534. The calculation of voltage depends on the value of the voltage reference. When the Vref is based on Vdda, the value used for Vdda is set for the project in the System tab of the Design Wide Resources (DWR).

Parameters: int16 adcCounts: Result from the ADC_SAR_Seq conversion

Return Value: float32: Result in volts

int32 ADC_SAR_Seq_CountsTo_mVolts(int16 adcCounts)

Description: Converts the ADC_SAR_Seq output to millivolts as a 32-bit integer. For example, if the ADC_SAR_Seq measured 0.534 volts, the return value would be 534. The calculation of voltage depends on the value of the voltage reference. When the Vref is based on Vdda, the value used for Vdda is set for the project in the System tab of the Design Wide Resources (DWR).

Parameters: Int32 adcCounts: Result from the ADC_SAR_Seq conversion

Return Value: int32: Result in mV

int32 ADC_SAR_Seq_CountsTo_uVolts(int16 adcCounts)

Description: Converts the ADC_SAR_Seq output to microvolts as a 32-bit integer. For example, if the ADC_SAR_Seq measured 0.534 volts, the return value would be 534000. The calculation of voltage depends on the value of the voltage reference. When the Vref is based on Vdda, the value used for Vdda is set for the project in the System tab of the Design Wide Resources (DWR).

Parameters: int16 adcCounts: Result from the ADC conversion

Return Value: int32: Result in µV

void ADC_SAR_Seq_Sleep(void)

Description: This is the preferred routine to prepare the Component for sleep. The ADC_SAR_Seq_Sleep() routine saves the current Component state. Then it calls the ADC_SAR_Seq_Stop() function and calls ADC_SAR_Seq_SaveConfig() to save the hardware configuration.

Call the ADC_SAR_Seq_Sleep() function before calling the CyPmSleep() or the CyPmHibernate() function. See the PSoC Creator *System Reference Guide* for more information about power-management functions.

void ADC_SAR_Seq_Wakeup(void)

Description: This is the preferred routine to restore the Component to the state when ADC_SAR_Seq_Sleep() was called. The ADC_SAR_Seq_Wakeup() function calls the ADC_SAR_Seq_RestoreConfig() function to restore the configuration. If the Component was enabled before the ADC_SAR_Seq_Sleep() function was called, the ADC_SAR_Seq_Wakeup() function also re-enables the Component.

Side Effects: Calling the ADC_SAR_Seq_Wakeup() function without first calling the ADC_Sleep() or ADC_SAR_Seq_SaveConfig() function can produce unexpected behavior.

void ADC_SAR_Seq_Init(void)

Description: Initializes or restores the Component according to the customizer Configure dialog settings. It is not necessary to call ADC_SAR_Seq_Init() because the ADC_SAR_Seq_Start() routine calls this function and is the preferred method to begin Component operation.

Side Effects: All registers will be set to values according to the customizer Configure dialog.

void ADC_SAR_Seq_Enable(void)

Description: Activates the hardware and begins Component operation. It is not necessary to call ADC_SAR_Seq_Enable() because the ADC_SAR_Seq_Start() routine calls this function, which is the preferred method to begin Component operation. It is not recommended to call this API a second time without stopping the Component first.

void ADC_SAR_Seq_SaveConfig(void)

Description: This function saves the Component configuration and nonretention registers. It also saves the current Component parameter values, as defined in the Configure dialog or as modified by the appropriate APIs. This function is called by the ADC_SAR_Seq_Sleep() function.

Side Effects: All ADC_SAR_Seq configuration registers are retained. This function does not have an implementation and is meant for future use. It is shown here so that the APIs are consistent across Components.

void ADC_SAR_Seq_RestoreConfig(void)

Description: This function restores the Component configuration and nonretention registers. It also restores the Component parameter values to what they were before calling the ADC_SAR_Seq_Sleep() function.

Side Effects: Calling this function without first calling the ADC_SAR_Seq_Sleep() or ADC_SAR_Seq_SaveConfig() function can produce unexpected behavior. This function does not have an implementation and is meant for future use. It is provided here so that the APIs are consistent across Components.

Global Variables

Variable	Description
ADC_SAR_Seq_initVar	This variable indicates whether the ADC has been initialized. The variable is initialized to 0 and set to 1 the first time ADC_SAR_Seq _Start() is called. This allows the Component to restart without reinitialization after the first call to the ADC_SAR_Seq _Start() routine. If reinitialization of the Component is required, then the ADC_SAR_Seq _Init() function can be called before the ADC_SAR_Seq _Start() or ADC_SAR_Seq _Enable() functions.
ADC_SAR_Seq_finalArray	This array contains valid conversion results for all channels each time after EOC pulse has been generated and EOC status is set. **Note** When using the values from this array directly (not using ADC_SAR_Seq_GetResult16() API function), the fact should be taken into account, that channels are scanned in a reverse order, so the conversion result for the last channel will be placed at ADC_SAR_finalArray[0]. Do not use this array directly in any of Differential modes because the ADC_SAR_offset is not taken into account. Use ADC_SAR_Seq_GetResult16(), where it is handled. If used directly, you must manually handle the ADC_SAR_offset.

Macro Callbacks

Macro callbacks allow users to execute code from the API files that are automatically generated by PSoC Creator. Refer to the PSoC Creator Help and *Component Author Guide* for the more details.

In order to add code to the macro callback present in the Component's generated source files, perform the following:

- Define a macro to signal the presence of a callback (in *cyapicallbacks.h*). This will "uncomment" the function call from the Component's source code.
- Write the function declaration (in *cyapicallbacks.h*). This will make this function visible by all the project files.
- Write the function implementation (in any user file).

Callback Function [2]	Associated Macro	Description
ADC_SAR_Seq_ISR_InterruptCallback	ADC_SAR_Seq_ISR_INTERRUPT_CALLBACK	Used in the ADC_SAR_Seq_ISR() interrupt handler to perform additional application-specific actions.

MISRA Compliance

This section describes the MISRA-C:2004 compliance and deviations for the Component. There are two types of deviations:

- project deviations – deviations that are applicable for all PSoC Creator Components
- specific deviations – deviations that are applicable only for this Component

This section provides information on Component-specific deviations. Project deviations are described in the MISRA Compliance section of the *System Reference Guide* along with information on the MISRA compliance verification environment.

The ADC_SAR_Seq Component does not have any specific deviations.

This Component has the following embedded Components: ADC_SAR, DMA, interrupt, clock, Hardware AMUX. Refer to the corresponding Component datasheets for information on their MISRA compliance and specific deviations.

2 The callback function name is formed by Component function name optionally appended by short explanation and "Callback" suffix.

API Memory Usage

The Component memory usage varies significantly depending on the compiler, device, number of APIs used and Component configuration. This table gives the memory usage for all APIs available in the default Component configuration.

The measurements were done with the associated compiler configured in release mode with optimization set for size. For a specific design, analyze the map file generated by the compiler to determine the memory usage.

Configuration	PSoC 5LP (GCC)	
	Flash Bytes	SRAM Bytes
Default	1486	32

Interrupt Service Routine

The ADC_SAR_Seq contains a blank interrupt service routine in the file *ADC_SAR_Seq_INT.c* file, where “ADC_SAR_Seq” is the instance name. You can place custom code in the designated areas to perform whatever function is required at the end of a conversion. A copy of the blank interrupt service routine is shown below. Place custom code between the “`/* `#START MAIN_SEQ_ADC_ISR` */`” and “`/* `#END` */`” comments. This ensures that the code will be preserved when a project is regenerated.

```
CY_ISR( ADC_SAR_Seq_ISR )
{
    #ifdef ADC_SAR_Seq_ISR_INTERRUPT_CALLBACK
        ADC_SAR_Seq_ISR_InterruptCallback();
    #endif /* ADC_SAR_Seq_ISR_INTERRUPT_CALLBACK */

    /***************************************************************************
    *  Custom Code
    *  - add user ISR code between the following #START and #END tags
    ***************************************************************************/
      /* `#START MAIN_SEQ_ADC_ISR`  */

      /* `#END`  */
}
```

A second designated area is available to place variable definitions and constant definitions.

```
/* `#START SEQ_ADC_SYS_VAR `  */

/* `#END`  */
```

Note You may use an alternative Interrupt service routine, located in your *main.c* file. In this case use the following template:

Implement interrupt service routine in *main.c*:

```
CY_ISR( ADC_SAR_Seq_ISR_LOC )
```

```
{
        /* Place your code here */
}
```

Enable ADC interrupt and set interrupt handler to local routine:

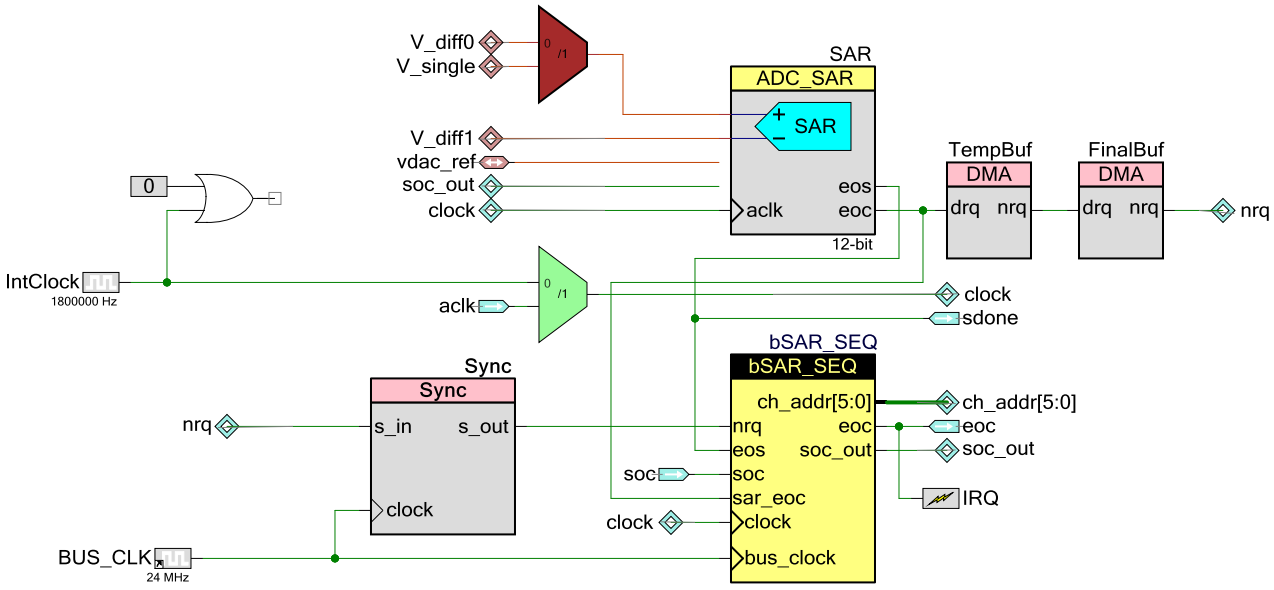
```
ADC_SAR_Seq_IRQ_StartEx(ADC_SAR_Seq_ISR_LOC);
```

Refer to Macro Callbacks section for details how to use callback from ISR.

Refer to the Interrupt Component datasheet for more information.

Functional Description

This block diagram shows how input analog signals from the hardware AMUX are sampled and converted by the ADC SAR Component. The first DMA channel moves the results one at a time from the SAR ADC to the temporary RAM buffer. When a complete set of data for all channels is collected in the temporary RAM buffer, the contents of the temporary RAM buffer are transferred to the results (SRAM) buffer in one transfer. Using a temporary buffer allows all data to be collected so that the results buffer are updated once per scan, so that you have the necessary time to do one scan sequence to move the last results.



Converting one sample in free running sample mode takes 12+6 clock cycles, or 12+4 clock cycles if Reference is Internal Vref (not bypassed), where 12 is a resolution in bits ($RESOLUTION_{bits}$), 6 (or 4) is a sample width and auto-zeroing ($SAMPLE_{width}$).

The conversion time of the each sample is more than four cycles when hardware trigger sample mode is used (SOC_{hw}). One cycle more for whole sampling is used for the soc edge detect logic by sequencer (SOC_{edge}).

The total number of clock required for sampling a selected number of channels could be calculated by the following formula:

$$SAR\_Seq_{clk}=SOC_{edge}+(RESOLUTION_{bits}+SAMPLE_{width}+SOC_{hw}) * Channels + DMA_{bus\_clk}$$

The DMA operates at the same frequency as the CPU, which is the bus clock frequency. If the ideal conditions are met, the number of bus clock cycles required for a data transfer from the SAR to the RAM is equal to N+7 and from the RAM to the RAM is equal to 2N+6 where N is a number of bursts. When the latest conversion is complete the DMA transfers last result from the SAR to the RAM buffer and whole results from temporary RAM buffer to the results RAM buffer:

$$DMA_{bus\_clk}= 1+7 + 2*Channels+6$$

Refer to AN84810 for details on how to calculate the exact number of bus clock cycles required for a DMA transaction under non-ideal conditions.

Refer to the ADC_SAR Component datasheet for more information.

Registers

Status Register

ADC_SAR_SEQ_STATUS_REG

Bits	7	6	5	4	3	2	1	0
Value	Unused							EOC

- EOC – End of Conversion. This register is set when one cycle of conversion for all channels is complete.

Resources

The ADC_SAR_Seq uses SAR ADC Component, which in turn is placed on a fixed-block SAR in the silicon.

Configuration	Resource Type					
	Datapath Cells	Macrocells	Status Cells	Control/ Counter7 Cells	DMA Channels	Interrupts
Default	-	43	3	2	2	1

DC and AC Electrical Characteristics

These values indicate expected performance and are based on initial characterization data. Unless otherwise specified, operating conditions are:

- Fclk = 1-18 MHz

  Note The desired sample rate is guaranteed only if bus clock frequency value is at least twice as large as the Component clock frequency.

- Input range = $\pm V_{REF}$
- Bypass capacitor of 10 µF

See the appropriate section of the ADC SAR Component datasheet for more details.

Component Changes

This section lists the major changes in the Component from the previous version.

Version	Description of Changes	Reason for Changes / Impact
2.10	Updated version of the embedded ADC_SAR Component to the most current version.	Out of date Components may contain defects or incompatibilities.
	Fixed a potential issue with the Component configured in “Hardware trigger” sample mode described in Errata section of the previous component version.	Removed Component Errata section.
2.0.c	Datasheet update.	Updated the Functional Description section with details on how to calculate the number of clocks required for sampling. Added Interrupt Service Routine section.
2.0.b	Datasheet update.	Added Macro Callbacks section.
2.0.a	Updated ADC_SAR_Seq_Start() and ADC_SAR_Seq_Enable() descriptions.	Added a note that these APIs should not be called a second time without first stopping the Component.
	Added Component Errata section.	Document a potential issue and workaround if the Component configured in “Hardware trigger” sample mode.
2.0	The maximum sampling rate when operating with VDDA reference was reduced from 1 Msps to 500 Ksps.	1 Msps rate is not guaranteed by the silicon when used without a bypass capacitor. Refer to the VRef Select parameter for more information.
	Changed the conversion time from 18 to 16 cycles for Internal Vref Reference. Limited usage of the XTAL clock source. Higher than 15 MHz XTAL must be divided by 2 or greater.	Limited configurations which violate DC/AC Specifications.

Version	Description of Changes	Reason for Changes / Impact
	Updated version of the embedded ADC_SAR Component to version 3.0.	Out of date Component may contain defects or incompatibilities.
	Corrected channels scanning sequence	Incorrect results of last scanned channels
	Corrected synchronization for high frequency clock	Warning of static timing analyze for high frequency clock
	Edited datasheet to remove Component Errata section.	This section does not apply to this version of the Component.
	Datasheet edits	Updated Features section to show inputs restriction. Updated MISRA Compliance section to remove MISRA deviations. Updated parameters description for ADC_SAR_Seq_GetResult16 API. Updated Resources section. Updated API Memory Usage section. Updated Functional Description section. Updated Reference section.
1.10.a	Edited datasheet to add Component Errata section.	Document that the Component was changed, but there is no impact to designs.
1.10	Updated the gain calibration to have better resolution. Added new ADC_SAR_Seq_SetScaledGain() API which sets the gain coefficient with more than 12-bit resolution.	New API added according to changes in the ADC SAR Component (gain coefficient (ADC_countsPerVolt) had 10-bits resolution in Vssa to Vdda input range.) This issue affected ADC_SAR_Seq_CountsTo_Volts(), ADC_SAR_Seq _CountsTo_mVolts(), and ADC_SAR_Seq _CountsTo_uVolts() API.
1.0	First Component release	