



**Habib University**  
**Electrical Engineering Department**  
**Dhanani School of Science & Engineering**

Course	EE – 211 – Basic Electronics
Semester	Fall 2022
Section	Section L2
Exam	Midterm Exam – 2
Instructor	Dr. Ahmad Usman
Total Marks	25

Name: SOLUTION Student ID: \_\_\_\_\_

**Note:**

- i. Attempt all questions.
- ii. No cheat sheets or formula sheets are allowed.
- iii. You can use your own calculators.
- iv. There are seven printed pages in this exam booklet. Don't open staple of the booklet.

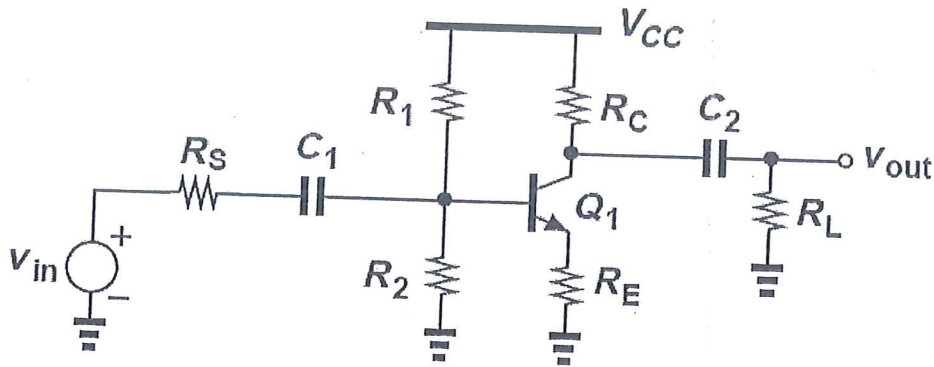
Questions	Points
Q1 (CLO – 2)	/8
Q2 (CLO – 3)	/7
Q3 (CLO – 1)	/4
Q4 (CLO – 1)	/6
<b>Total Obtained</b>	<b>/25</b>

### Question # 1 (CLO – 2 – Points: 8, 3 + 5)

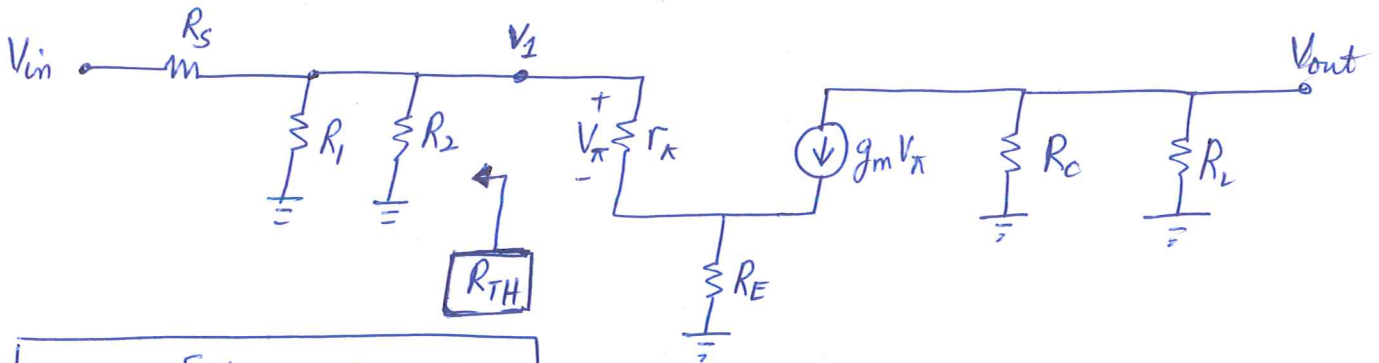
Draw the small-signal model for the circuit shown below. Also, calculate the voltage gain  $V_{out} / V_{in}$ . The specifications of the circuit are as follows:

$I_S = 8 \times 10^{-16} \text{ A}$ ,  $V_{CC} = 2.5 \text{ V}$ ,  $V_A = \infty$ ,  $\beta = 100$ ,  $R_C = 10 \text{ k}\Omega$ ,  $R_E = 500 \Omega$ ,  $R_1 = 14 \text{ k}\Omega$ ,  $R_2 = 11 \text{ k}\Omega$ ,  $R_S = 1 \text{ k}\Omega$ ,  $R_L = 100 \text{ k}\Omega$

Assume extremely high value capacitors.



#### Small Signal Model



$$V_1 = \left[ \frac{(R_1 // R_2)}{R_S + (R_1 // R_2)} \right] V_{in}$$

$$R_{TH} = R_S // R_1 // R_2$$

$$V_1 = \left( \frac{6.016 \text{ K}}{1 \text{ K} + 6.016 \text{ K}} \right) V_{in}$$

$$\frac{V_1}{V_{in}} = 0.86033$$

$$R_{TH} = 0.86033 \text{ K}\Omega$$

$$I_C = I_S \exp\left(\frac{V_{BE}}{V_T}\right)$$

$$\text{Let } V_{BE} = 0.7 \text{ V} \\ V_T = 26 \text{ mV}$$

$$I_C = 394.124 \mu\text{A}$$

$$g_m = \frac{I_C}{V_T}$$

$$g_m = 15.1586 \text{ mS}$$

### Input Resistance @ Emitter

$$R_{in} = \frac{R_x}{\beta} + R_E + \frac{R_{TH}}{\beta+1}$$

$$R_{in} = \frac{1}{g_m} + R_E + \frac{R_{TH}}{\beta+1}$$

$$R_{in} = \frac{1}{15.1586m} + 500 + \frac{0.8603K}{101}$$

$$R_{in} = 574.4869 \Omega$$

$$\boxed{R_{in} = 574.49 \Omega}$$

### Output Resistance

$$R_{out} = R_C \parallel R_L = \boxed{9.0909 K \Omega}$$

$$Gain = A_v = - \left( \frac{R_1 \parallel R_2}{R_s + R_1 \parallel R_2} \right) \left( \frac{R_C \parallel R_L}{\frac{1}{g_m} + R_E + \frac{R_{TH}}{\beta+1}} \right)$$

$$A_v = - (0.86033) \left( \frac{9.0909 K}{574.49} \right)$$

$$\boxed{A_v = -13.614}$$

## Question # 2 (CLO – 3 – Points: 7)

Design a self-bias (collector feedback bias) BJT configuration with the following specifications:

$I_{C,Q} = 5 \text{ mA}$ ,  $V_{CC} = 10\text{V}$ ,  $V_{CE,Q} = 5\text{V}$ ,  $V_{BE} = 0.7\text{V}$ , and  $\beta = 100$ .

Draw the circuit diagram. Determine  $R_C$ ,  $R_E$ , and  $R_B$ . Assume  $V_E$  as 10% of  $V_{CC}$ .

$$V_E = 10\% \text{ of } V_{CC}$$

$$V_E = \frac{10}{100} \times 10 = 1\text{V}$$

$$\boxed{V_E = I_E R_E}$$

$$I_E = I_C + I_B \Rightarrow I_E = (5\text{m})(1 + \frac{1}{100})$$

$$I_C = \beta I_B$$

$$\boxed{I_E = 5.05 \text{ mA}}$$

$$R_E = \frac{1}{5.05 \text{ m}} = \boxed{198.0198 \Omega}$$

Output Loop:

$$V_{CC} - I R_C - V_{CE} - V_E = 0$$

$$10 - (5.05 \text{ m}) R_C - 5 - 1 = 0$$

$$R_C = \frac{4}{5.05 \text{ m}}$$

$$\boxed{R_C = 792.079 \Omega}$$

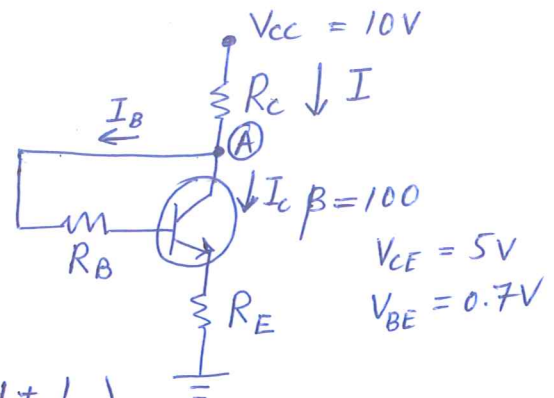
@ node A

$$V_A = V_{CE} + V_E \quad \text{--- (1)}$$

$$V_A = I_B R_B + V_{BE} + I_E R_E \quad \text{--- (2)}$$

$$I_B R_B + V_{BE} + \cancel{I_E R_E} = V_{CE} + \cancel{V_E}$$

$$R_B = \frac{5 - 0.7}{(5/100) \text{ m}} = \boxed{86 \text{ k}\Omega}$$

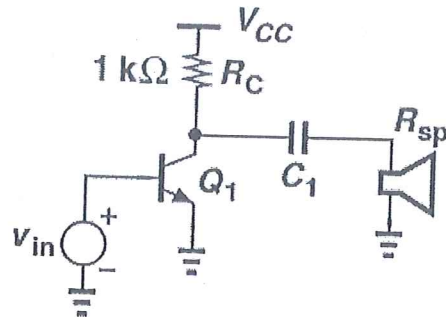


$R_E = 198.02 \Omega$
$R_C = 792.08 \Omega$
$R_B = 86 \text{ k}\Omega$

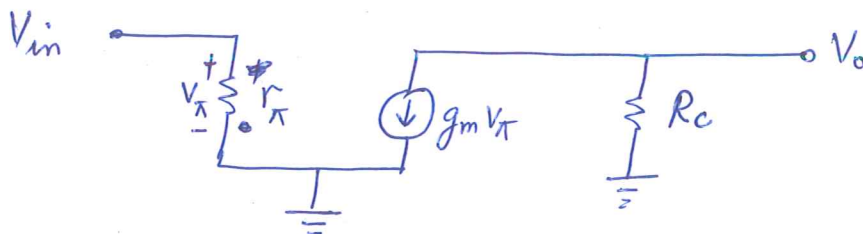


### Question # 3 (CLO – 1 – Points: 4)

A CE stage exhibits a voltage gain of 20 and an output resistance of  $1\text{ k}\Omega$ . Determine the voltage gain of the CE amplifier if the stage drives an  $8\text{-}\Omega$  speaker directly. Explain in your own words what happened to the gain?



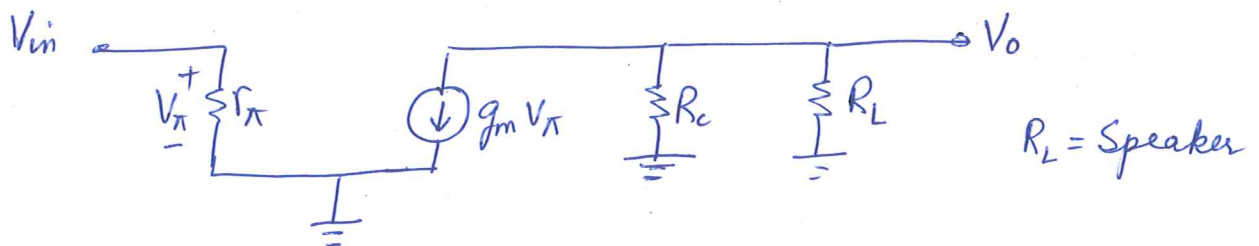
Without Speaker



$$\text{Gain} = |A_v| = |g_m R_C|$$

$$20 = g_m (1\text{ k}) \rightarrow \boxed{g_m = 0.02\text{ S}}$$

After Speaker



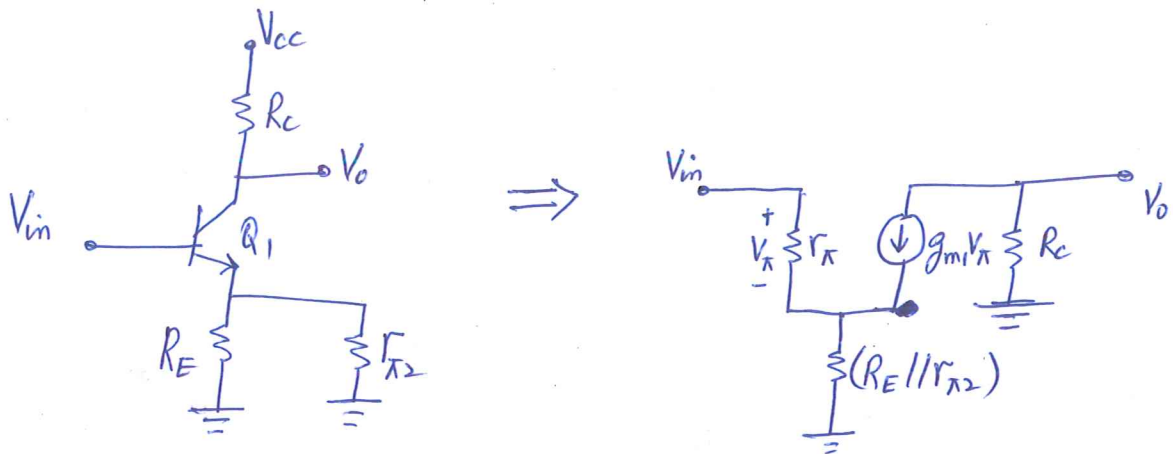
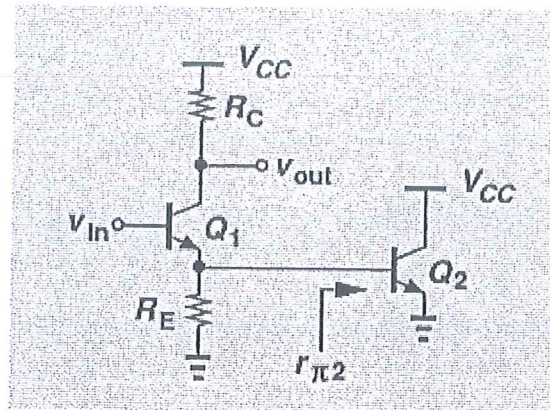
$$\text{Gain} = |A_v| = |g_m (R_C || R_L)|$$

$$\boxed{A_v = 0.1587}$$

→ The gain decreases when the speaker was added as a load.

**Question # 4 (CLO – 1 – Points: 6, 3 + 3)**

(a) Determine the voltage gain of the stage shown in the figure below.

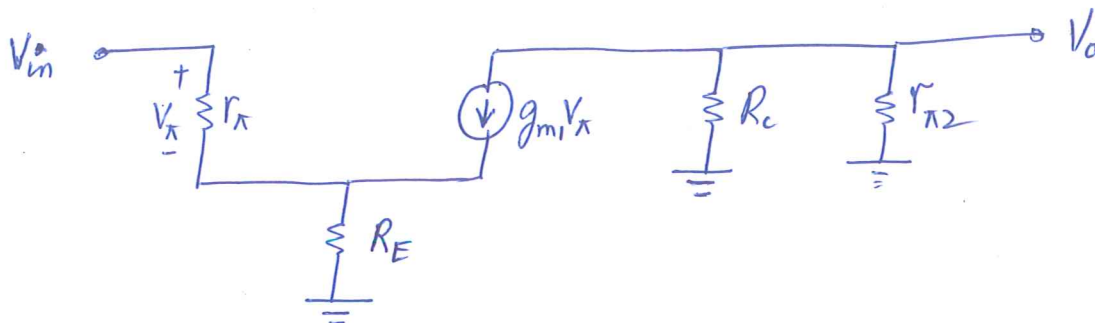
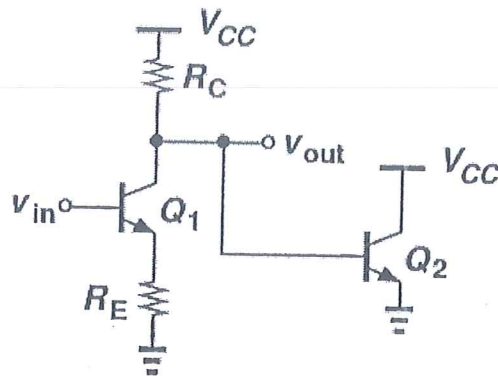


$$A_v = \frac{-g_{m1} R_c}{1 + g_{m1} (R_E // r_{\pi 2})}$$

OR

$$A_v = \frac{-R_c}{1/g_{m1} + (R_E // r_{\pi 2})}$$

(b) Determine the voltage gain of the stage shown in the figure below.



$$A_v = \frac{-g_{m1} (R_C \parallel r_{\pi 2})}{1 + g_{m1} R_E}$$

OR

$$A_v = \frac{-(R_C \parallel r_{\pi 2})}{1/g_{m1} + R_E}$$