EE / CE – 211
Basic Electronics
(Spring – 2024)

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- **Reading for this Lecture**
  - Chapter # 4 and 5 of **“Introduction to Microelectronics”** by Behzad Razavi
  - Chapter # 10 of “Semiconductor Device Fundamentals” by R.F. Pierret

Physics of Bipolar Junction Transistors

- **What we shall be doing in this chapter**
  - Voltage-Controlled Device as an Amplifier
  - Structure of Bipolar Junction Transistor (BJT)
  - Operation of BJT
  - Large-Signal Model of BJT
  - Small-Signal Model of BJT

Physics of Bipolar Junction Transistors

❑Voltage-dependant Current Source and Amplifier

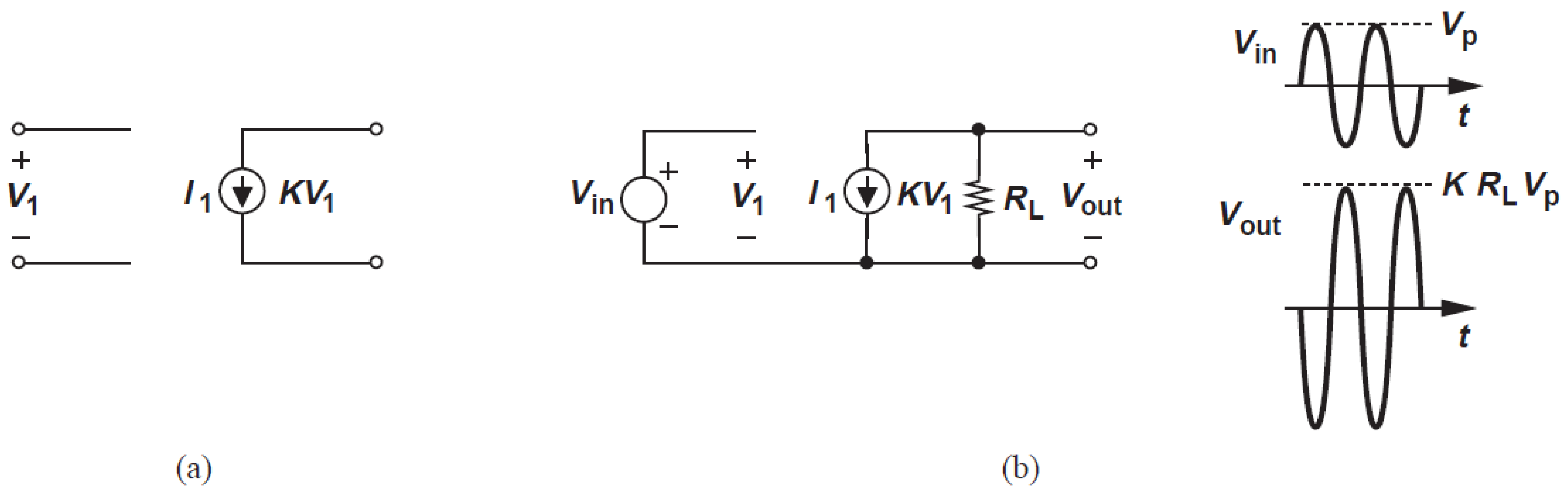


Figure 4.1 (a) Voltage-dependent current source, (b) simple amplifier.

Physics of Bipolar Junction Transistors

Example 4.1

Consider the circuit shown in Fig. 4.2, where the voltage-controlled current source exhibits an "internal" resistance of r_{in}. Determine the voltage gain of the circuit.

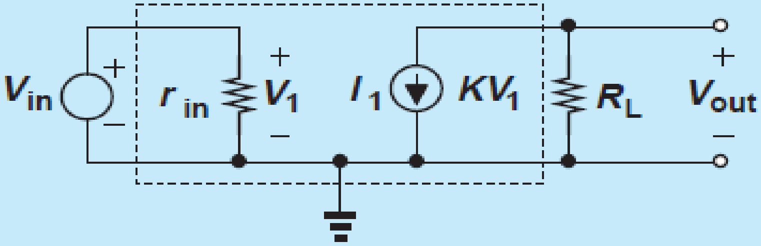


Figure 4.2 Voltage-dependent current source with an internal resistance r_{in}.

Physics of Bipolar Junction Transistors

❑Structure of Bipolar Junction Transistors (BJTs)

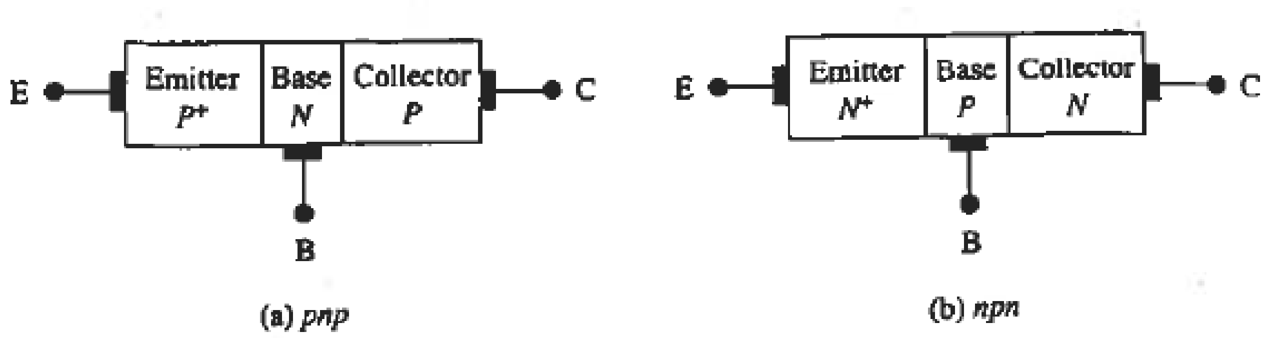


Figure 10.1 Schematic representation of the (a) *pnp* and (b) *npn* BJT showing device regions and the terminal designations.

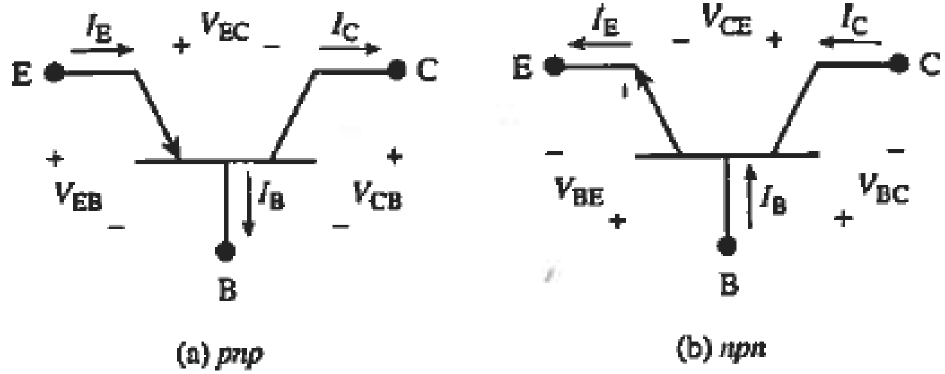


Figure 10.2 (a) *pnp* and (b) *npn* BJT circuit symbols. The d.c. terminal currents, voltages, and reference polarities are also noted in the figure.

Physics of Bipolar Junction Transistors

❑Structure of Bipolar Junction Transistors (BJTs)

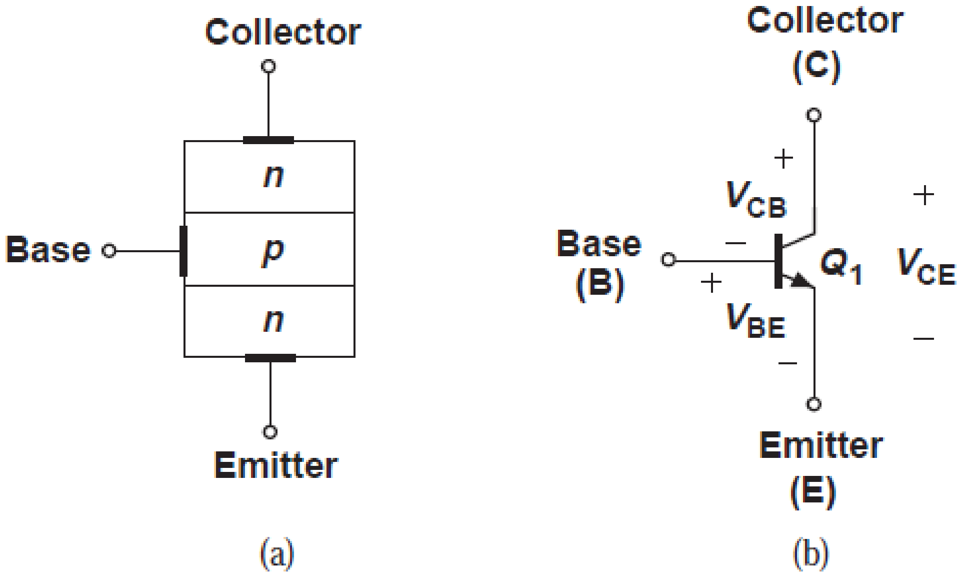
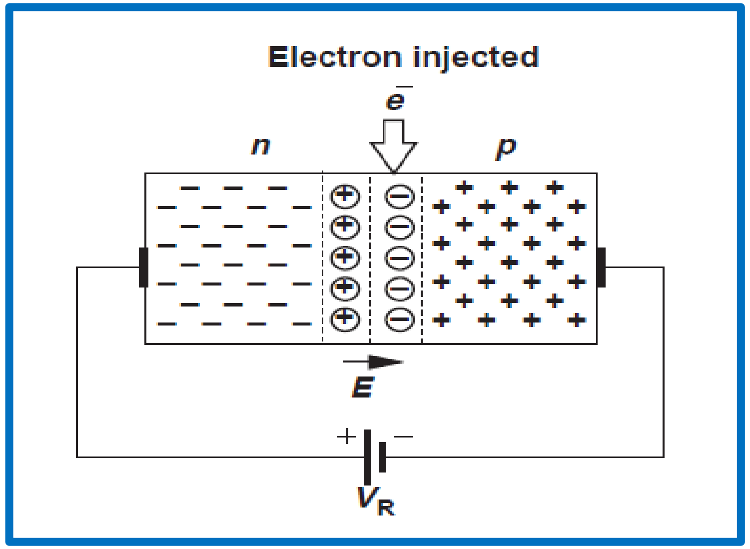


Figure 4.4 (a) Structure and (b) circuit symbol of bipolar transistor.

Physics of Bipolar Junction Transistors

❑Carrier Injection

- ❑Reverse Biased pn-junction
- ❑Electrons are injected into the depletion region
- ❑Experiences E-field in the depletion region
- ❑Swept away into the n-side of the pn-junction



- ❑**"Reverse biased"** pn-junction can efficiently "collect" **externally injected electrons**

Physics of Bipolar Junction Transistors

❑Operation of Bipolar Junction Transistors (BJTs)

❑Circuit Configurations

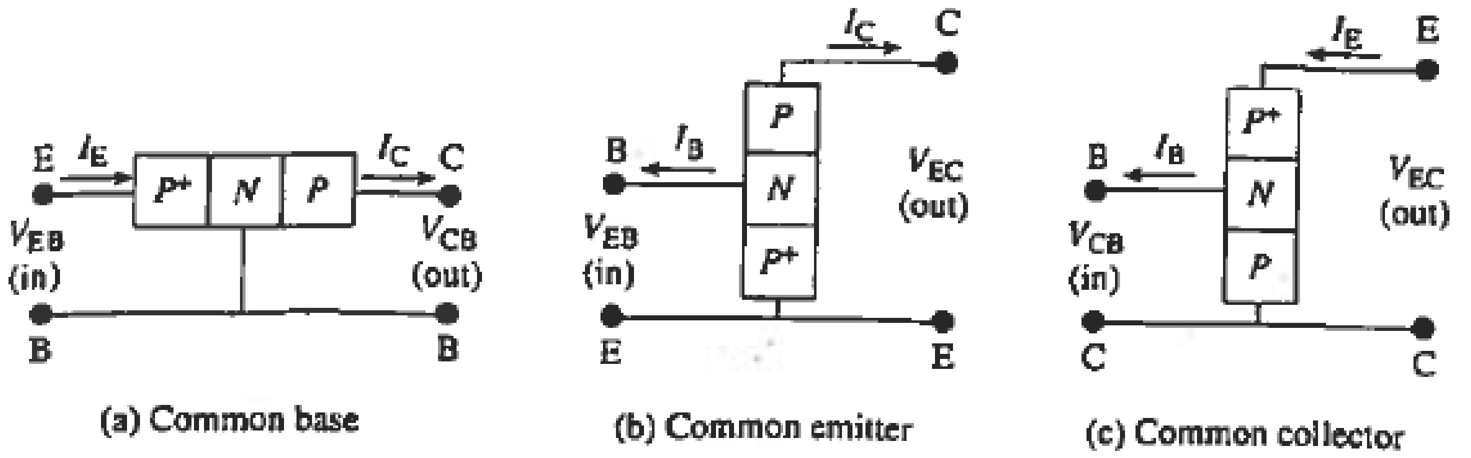


Figure 10.3 Circuit configurations: (a) common base; (b) common emitter; and (c) common collector.

$$\boxed{I_E = I_B + I_C}$$

$$\boxed{V_{EB} + V_{BC} + V_{CE} = 0}$$

Physics of Bipolar Junction Transistors

❑Operation of Bipolar Junction Transistors (BJTs)

❑Operation / Biasing Modes

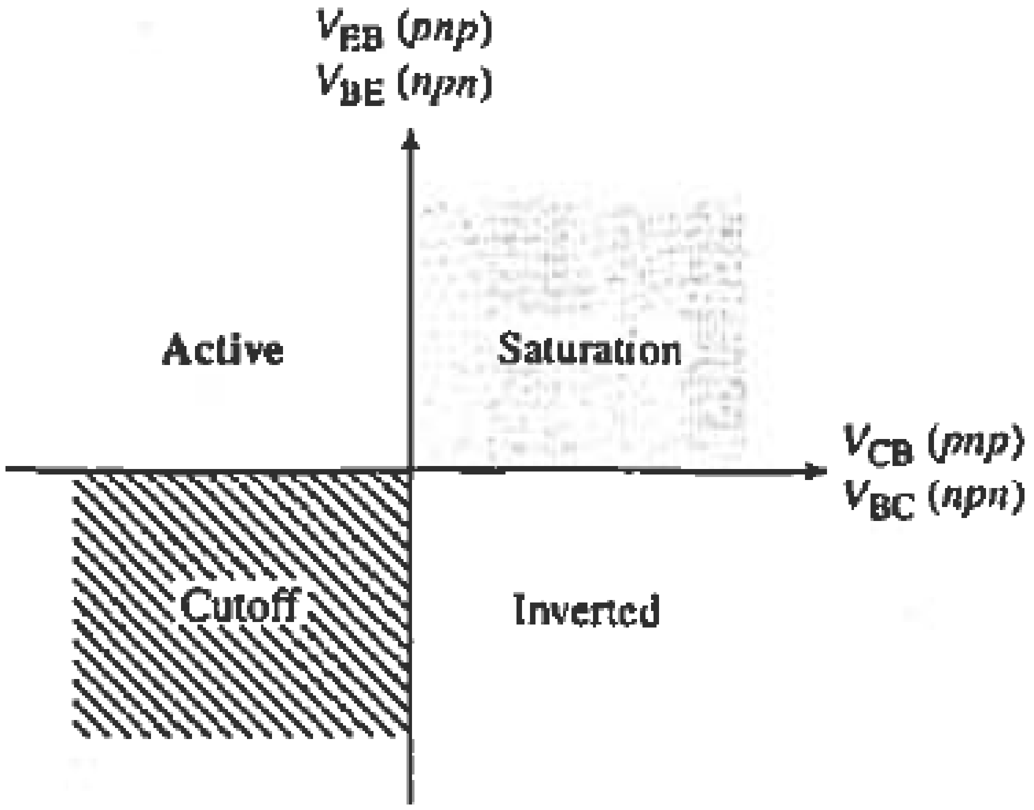


Table 10.1 Biasing Modes.

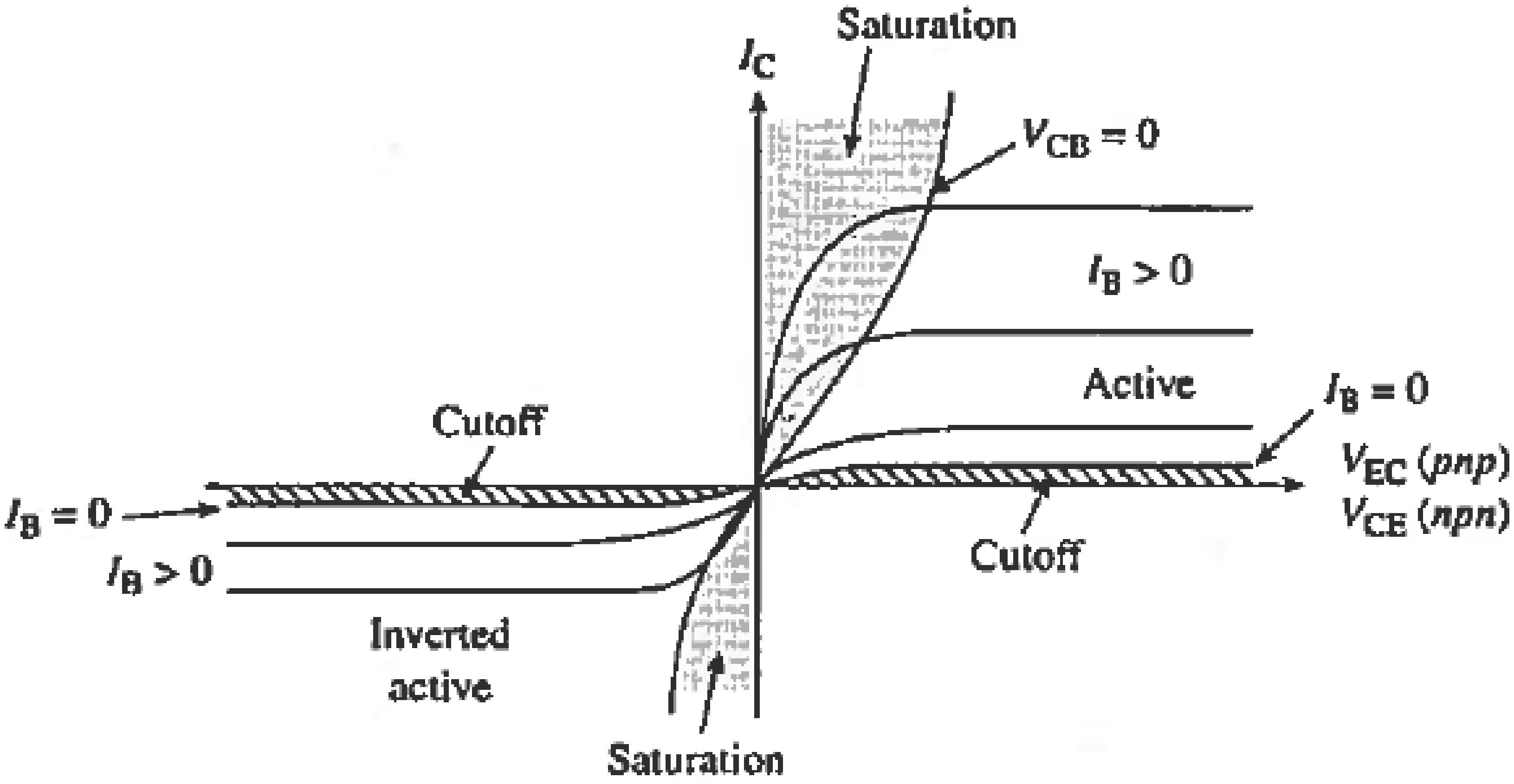
Biasing Mode	*Biasing Polarity E–B Junction*	*Biasing Polarity C–B Junction*
Saturation	Forward	Forward
Active	Forward	Reverse
Inverted	Reverse	Forward
Cutoff	Reverse	Reverse

Physics of Bipolar Junction Transistors

❑Operation of Bipolar Junction Transistors (BJTs)

❑Output Characteristics

❑Common Emitter (CE) Biasing Configuration



Physics of Bipolar Junction Transistors

❑Operation of Bipolar Junction Transistors (BJTs)

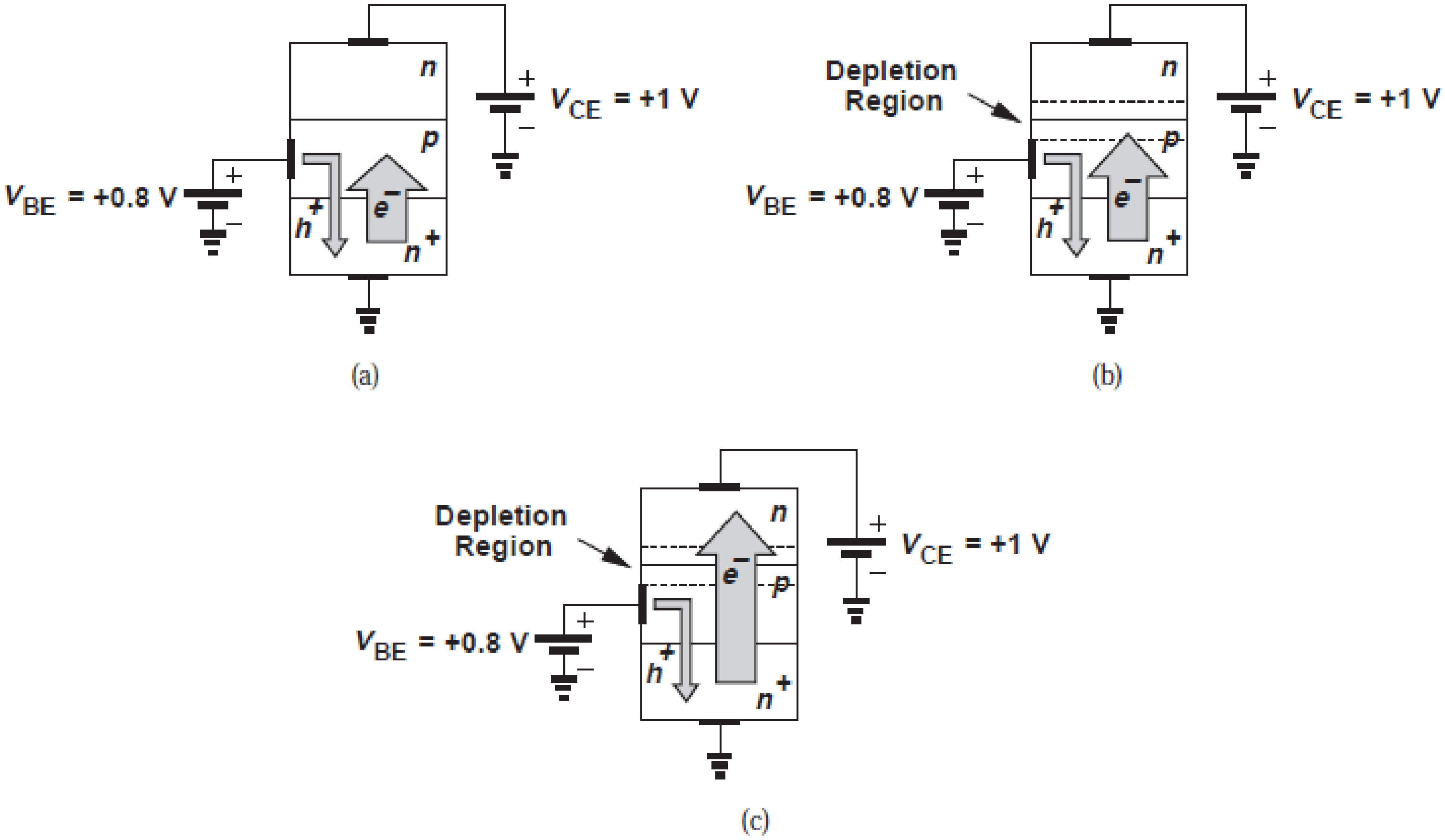


Figure 4.7 (a) Flow of electrons and holes through base-emitter junction, (b) electrons approaching collector junction, (c) electrons passing through collector junction.

Physics of Bipolar Junction Transistors

❑Operation of Bipolar Junction Transistors (BJTs)

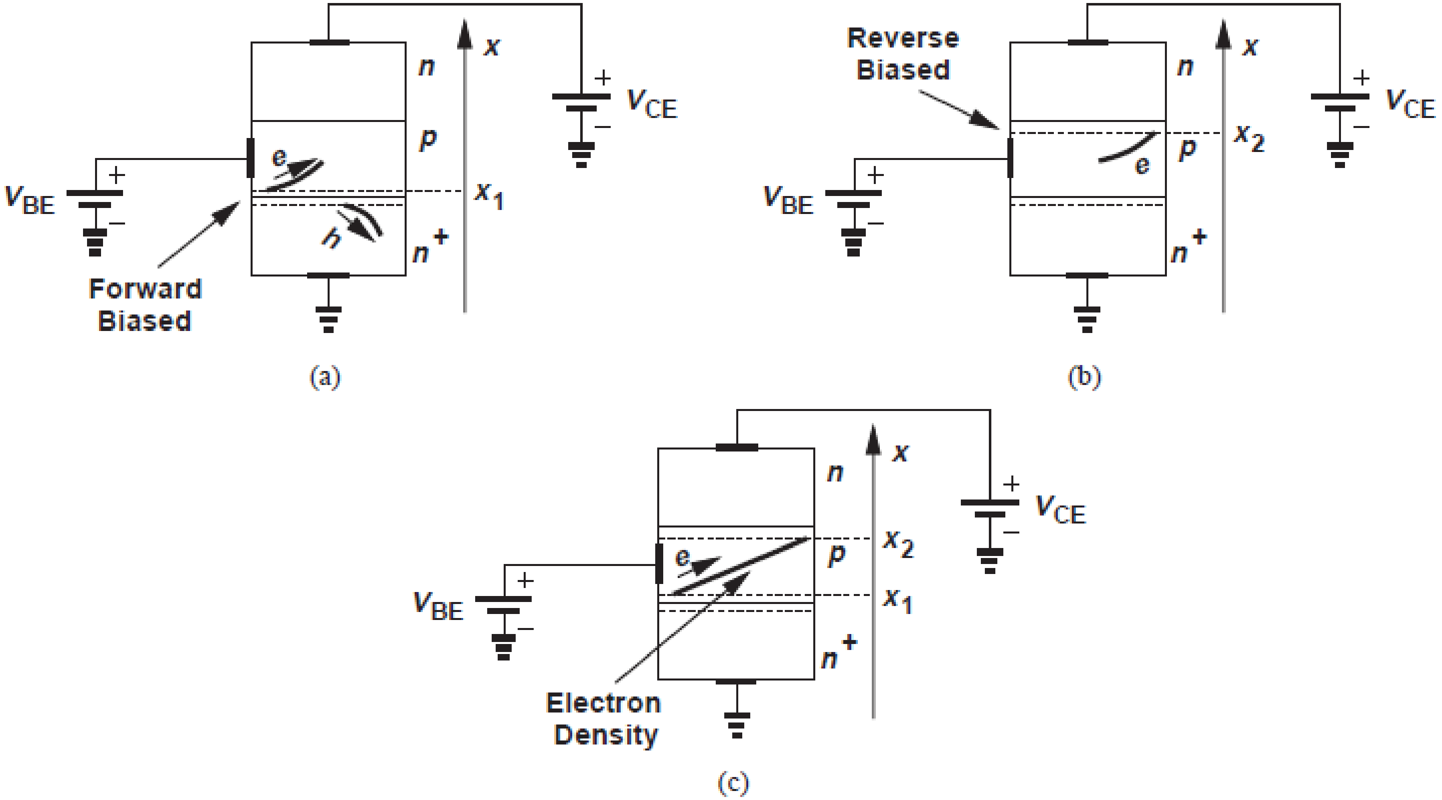


Figure 4.8 (a) Hole and electron profiles at base-emitter junction, (b) zero electron density near collector, (c) electron profile in base.

Physics of Bipolar Junction Transistors

❑Operation of Bipolar Junction Transistors (BJTs)

❑Collector Current and Terminal Voltages

$$\boxed{I_C = \frac{A_E q D_n n_i^2}{N_B W_B}\left(\exp\frac{V_{BE}}{V_T} - 1\right)}$$

Collector Current

$$\boxed{I_C = I_S \exp\frac{V_{BE}}{V_T}}$$

Diode Current Equation

❑Comparing the above equation, we can say that

- **In active mode operation, the collector current doesn't depend on collector voltage**
- **For a fixed V_{BE}, the device draws a constant current, acting as a current source, provided that $V_{CE} > V_{BE}$**

Physics of Bipolar Junction Transistors

❑Operation of Bipolar Junction Transistors (BJTs)

❑Collector Current and Terminal Voltages

- BJT operates as voltage-controlled current source (or voltage-dependent current source)
- BJT performs voltage to current conversion
- BJT is a good candidate for amplification

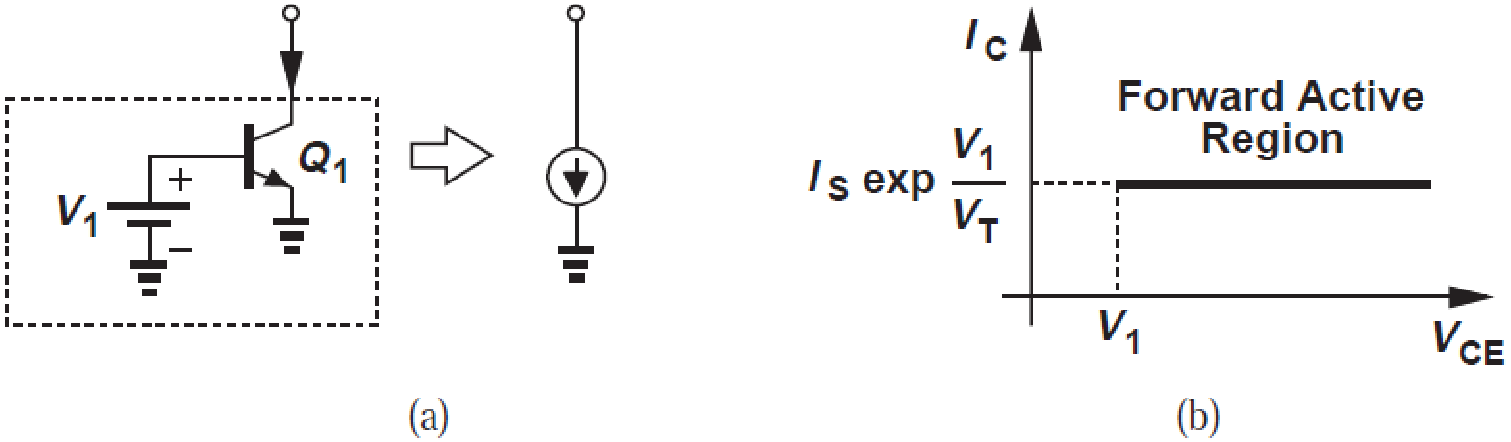


Figure 4.11 (a) Bipolar transistor as a current source, (b) I/V characteristic.

Physics of Bipolar Junction Transistors

Example 4.2

Determine the current I_X in Fig. 4.9(a) if Q_1 and Q_2 are identical and operate in the active mode and $V_1 = V_2$.

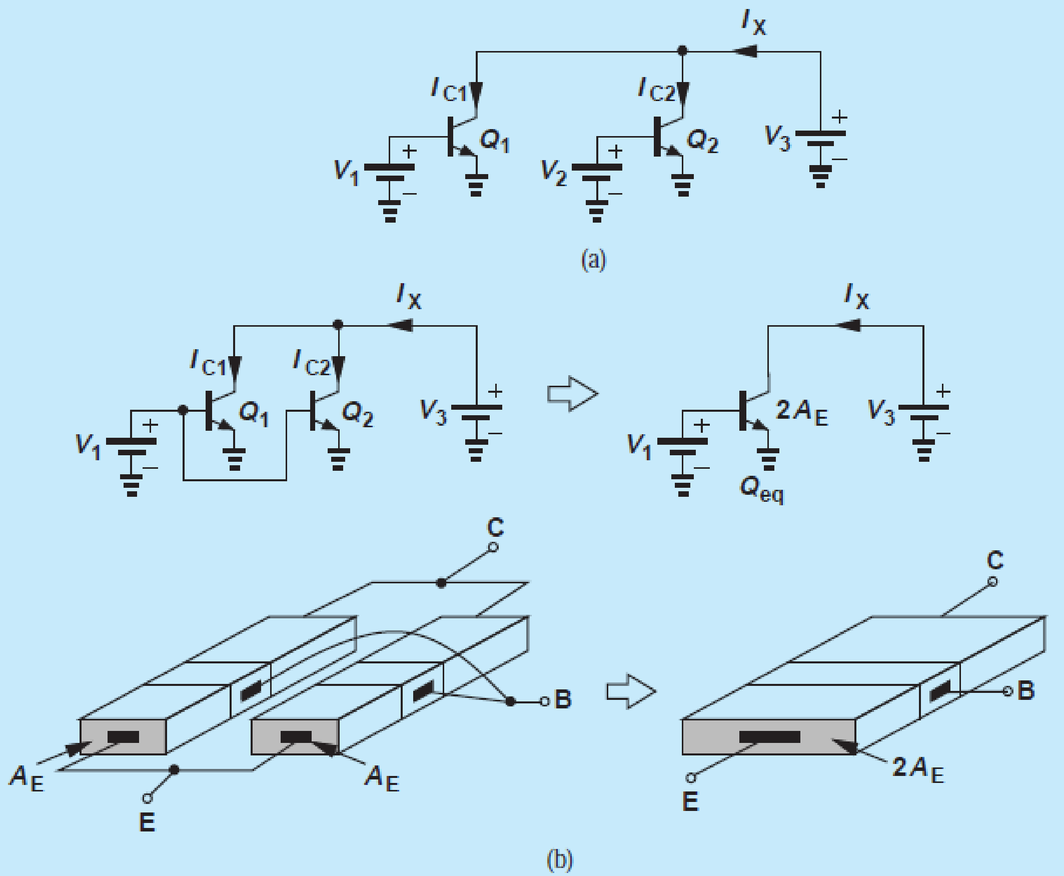


Figure 4.9 (a) Two identical transistors drawing current from V_C, (b) equivalence to a single transistor having twice the area.

Remember

$$\boxed{I_C = \frac{A_E q D_n n_i^2}{N_B W_B}\left(\exp\frac{V_{BE}}{V_T} - 1\right)}$$

Physics of Bipolar Junction Transistors

Example 4.3

In the circuit of Fig. 4.9 (a), Q_1 and Q_2 are identical and operate in the active mode. Determine $V_1 - V_2$ such that $I_{C1} = 10I_{C2}$.

Physics of Bipolar Junction Transistors

Example 4.4

Typical discrete bipolar transistors have a large area, e.g., 500 μm $\times$ 500 μm, whereas modern integrated devices may have an area as small as 0.5 μm $\times$ 0.2 μm. Assuming other device parameters are identical, determine the difference between the base-emitter voltage of two such transistors for equal collector currents.

Physics of Bipolar Junction Transistors

Example 4.5

Determine the output voltage in Fig. 4.10 if $I_S = 5 \times 10^{-16}$ A.

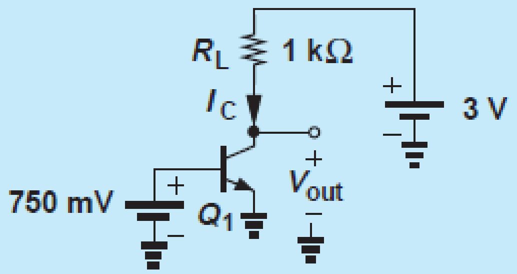


Figure 4.10 Simple stage with biasing.

Physics of Bipolar Junction Transistors

❑Base and Emitter Currents

- ❑β is the current gain of the BJT transistor
- ❑BJT equations are given below

$$\boxed{I_C = I_S \exp \frac{V_{BE}}{V_T}}$$

$$\boxed{I_E = I_C + I_B}$$

$$\boxed{I_C = \beta I_B}$$

$$\begin{aligned} I_E &= I_C + I_B \\ &= I_C\left(1 + \frac{1}{\beta}\right) \end{aligned}$$

$$I_C = I_S \exp \frac{V_{BE}}{V_T}$$

$$I_B = \frac{1}{\beta} I_S \exp \frac{V_{BE}}{V_T}$$

$$I_E = \frac{\beta + 1}{\beta} I_S \exp \frac{V_{BE}}{V_T}$$

Physics of Bipolar Junction Transistors

❑Large-Signal Model

- ❑Some textbooks consider this as DC – model

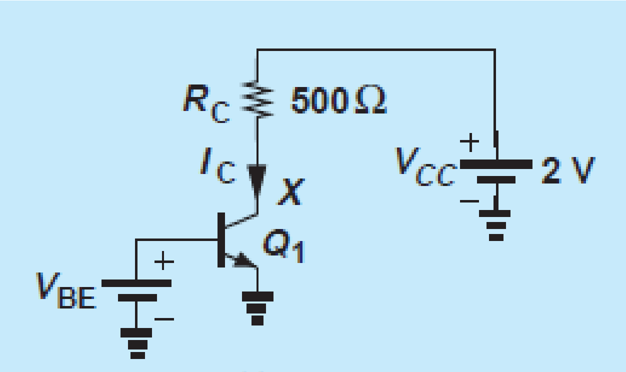
- ❑Large signal model is concerned with the biasing of the circuit with effort to make sure the BJT remains in its desired mode of operation e.g., Forward Active mode

- ❑The voltages and current applied are considerably of large values making sure the BJT remains in its desired mode of operation

Physics of Bipolar Junction Transistors

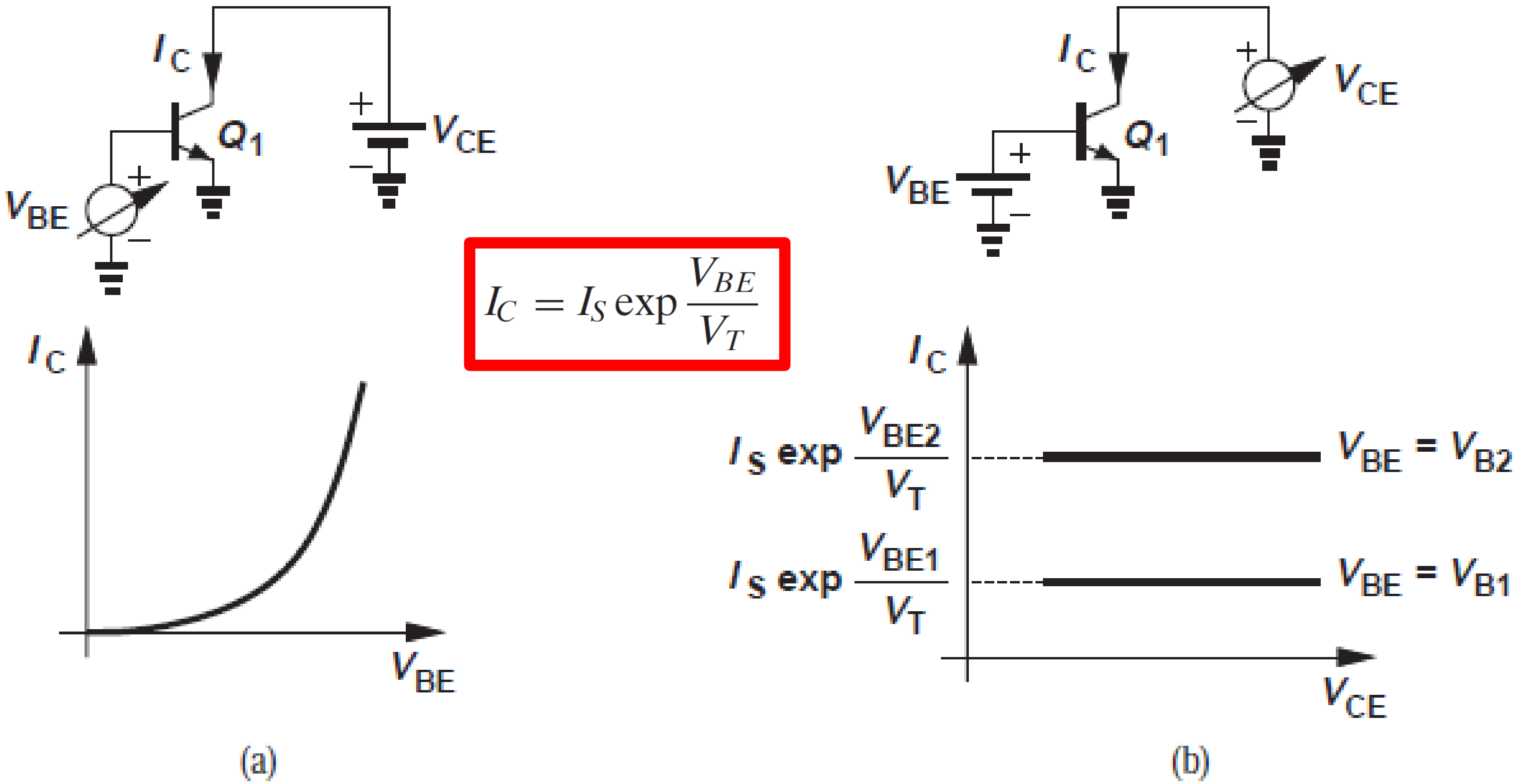
Example 4.7

Consider the circuit shown in Fig. 4.14 (a), where $I_{S,Q1} = 5 \times 10^{-17}$ A and $V_{BE} = 800$ mV. Assume $\beta = 100$. (a) Determine the transistor terminal currents and voltages and verify that the device indeed operates in the active mode. (b) Determine the maximum value of R_C that permits operation in the active mode.



Physics of Bipolar Junction Transistors

❑I-V Characteristics



$$\boxed{I_C = I_S \exp \frac{V_{BE}}{V_T}}$$

Figure 4.15 Collector current as a function of (a) base-emitter voltage and (b) collector-emitter voltage.

Physics of Bipolar Junction Transistors

Example 4.8 For a bipolar transistor, $I_S = 5 \times 10^{-17}$ A and $\beta = 100$. Construct the I_C-V_{BE}, I_C-V_{CE}, I_B-V_{BE}, and I_B-V_{CE} characteristics.

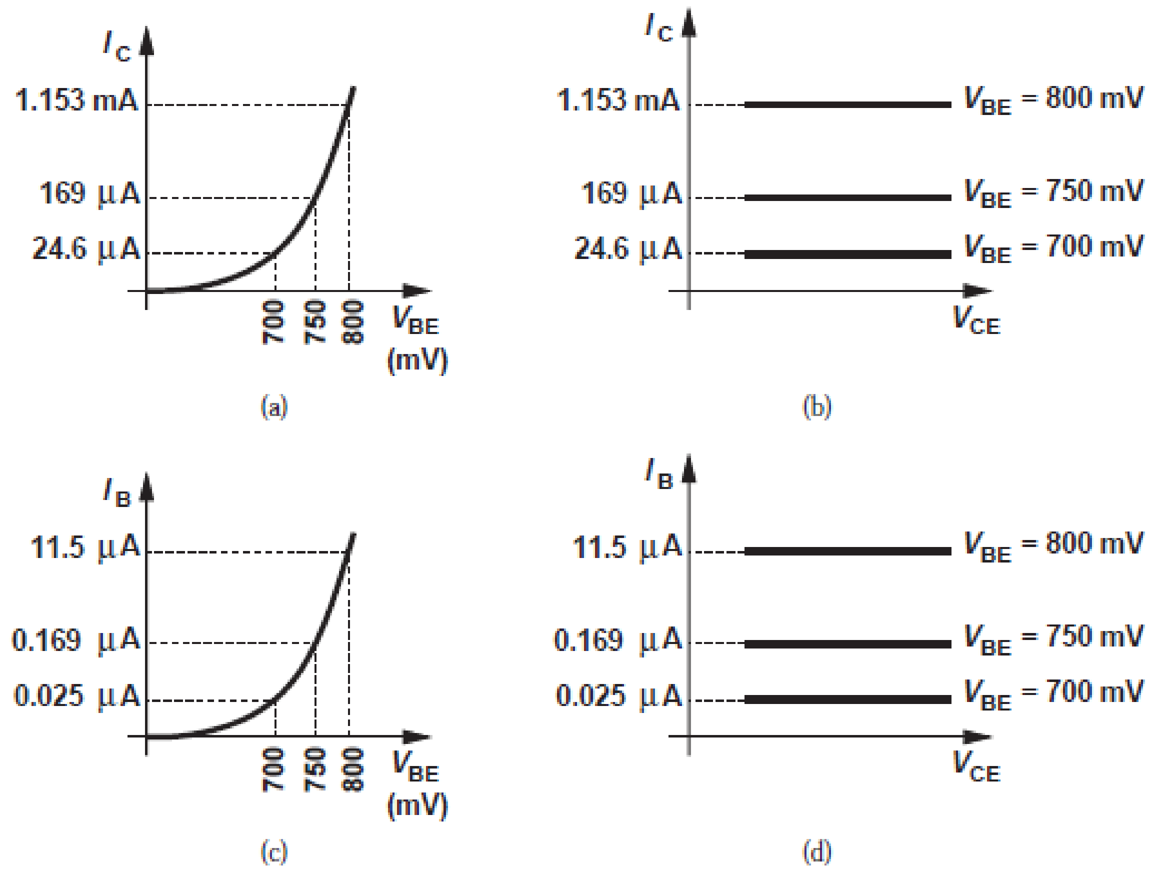
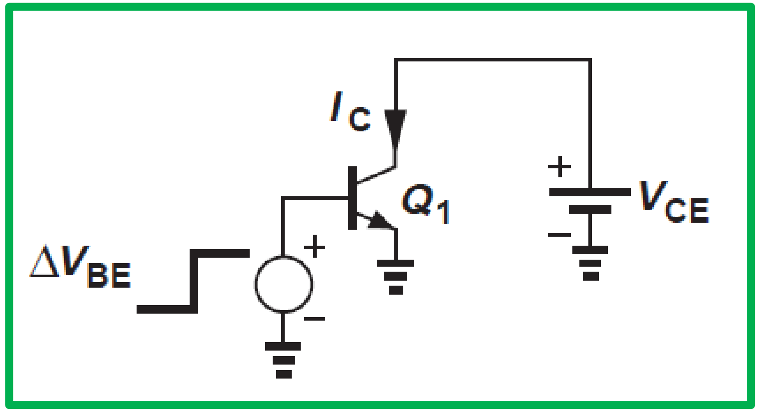


Figure 4.16 (a) Collector current as a function of V_{BE}, (b) collector current as a function of V_{CE}, (c) base current as a function of V_{BE}, (d) base current as a function of V_{CE}.

Physics of Bipolar Junction Transistors

❑Transconductance

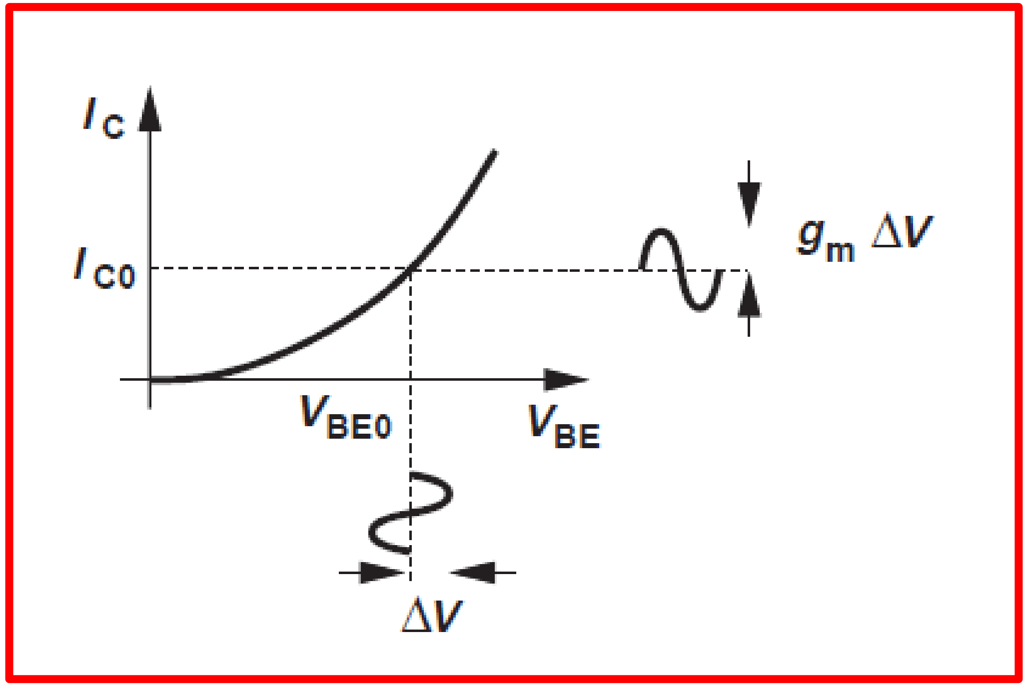
$$\boxed{g_m = \frac{dI_C}{dV_{BE}}}$$



$$g_m = \frac{d}{dV_{BE}}\left(I_S \exp \frac{V_{BE}}{V_T}\right)$$

$$= \frac{1}{V_T} I_S \exp \frac{V_{BE}}{V_T}$$

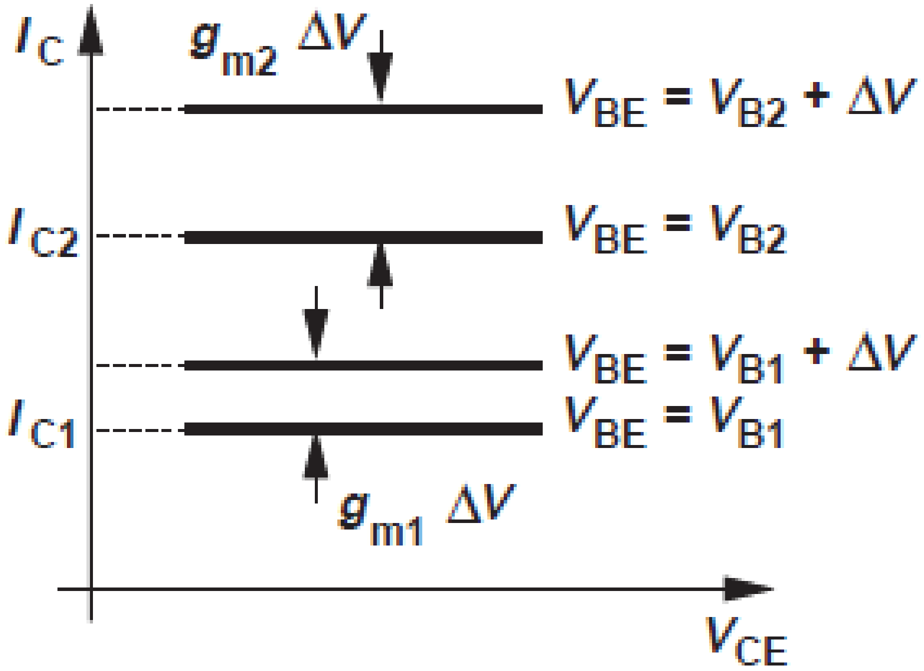
$$= \frac{I_C}{V_T}.$$



Physics of Bipolar Junction Transistors

❑Transconductance

❑Transconductance for different collector bias currents



$$g_m = \frac{I_C}{V_T}$$

$$\boxed{g_m = \frac{dI_C}{dV_{BE}}}$$

$$\boxed{I_C = I_S \exp\frac{V_{BE}}{V_T}}$$

- ❑ Two different bias currents I_{C1} and I_{C2}, the plots reveal that a change of ΔV in V_{BE} results in a greater change in I_C for operation around I_{C2} than around I_{C1} because $g_{m2} > g_{m1}$

Physics of Bipolar Junction Transistors

❑ Transconductance

- ❑ The BJT acts as a voltage-dependent current source when operating in the forward active region

- ❑ **What is the measure of goodness of a voltage-dependent current source ?**
  - ❑ Voltage-to-Current conversion property of a transistor (particularly for amplification of signals)
  - ❑ We ask ourselves – "If the input signal voltage at the base-emitter changes, how much change is produced in the collector current ?"
  - ❑ Basically, we are concerned with $\Delta I_C/\Delta V_{BE}$ .This ratio is called "transconductance, g_m"
  - ❑ Much similar to small signal resistance of diodes

$$\boxed{g_m = \frac{dI_C}{dV_{BE}}.}$$

Physics of Bipolar Junction Transistors

❑Transconductance

- ❑The transconductance is fundamentally a function of the collector current rather than the base current
  - ❑**For example:**
    - ✓ If I_C remains constant but β varies, then g_m does not change but I_B does

- ❑For this reason, the collector bias current plays a central role in the analysis and design, with the base current viewed as secondary, often undesirable effect

Physics of Bipolar Junction Transistors

❑Small-Signal Modeling

- ❑Remember the small-signal modeling help us to analyze the transistors in a linear fashion
- ❑Consider two cases
  - ❑Excitation (perturbation) at base-emitter terminal (from the input side)
  - ❑Excitation (perturbation) at collector-emitter terminal (from the output side)

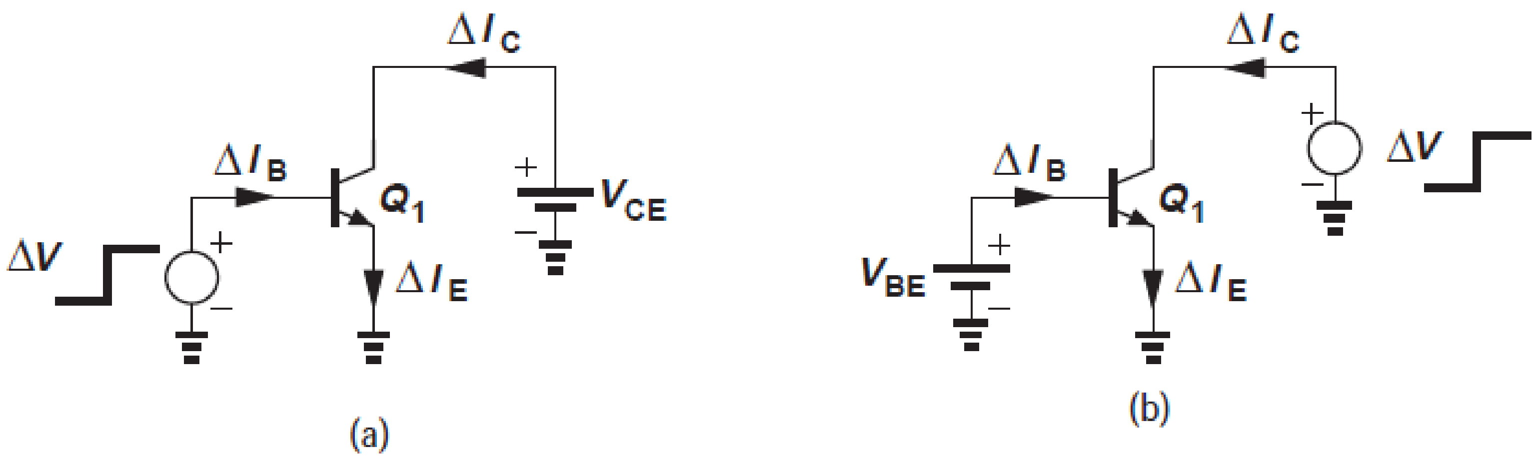


Figure 4.21 Excitation of bipolar transistor with small changes in (a) base-emitter and (b) collector-emitter voltage.

Physics of Bipolar Junction Transistors

❑Small-Signal Modeling

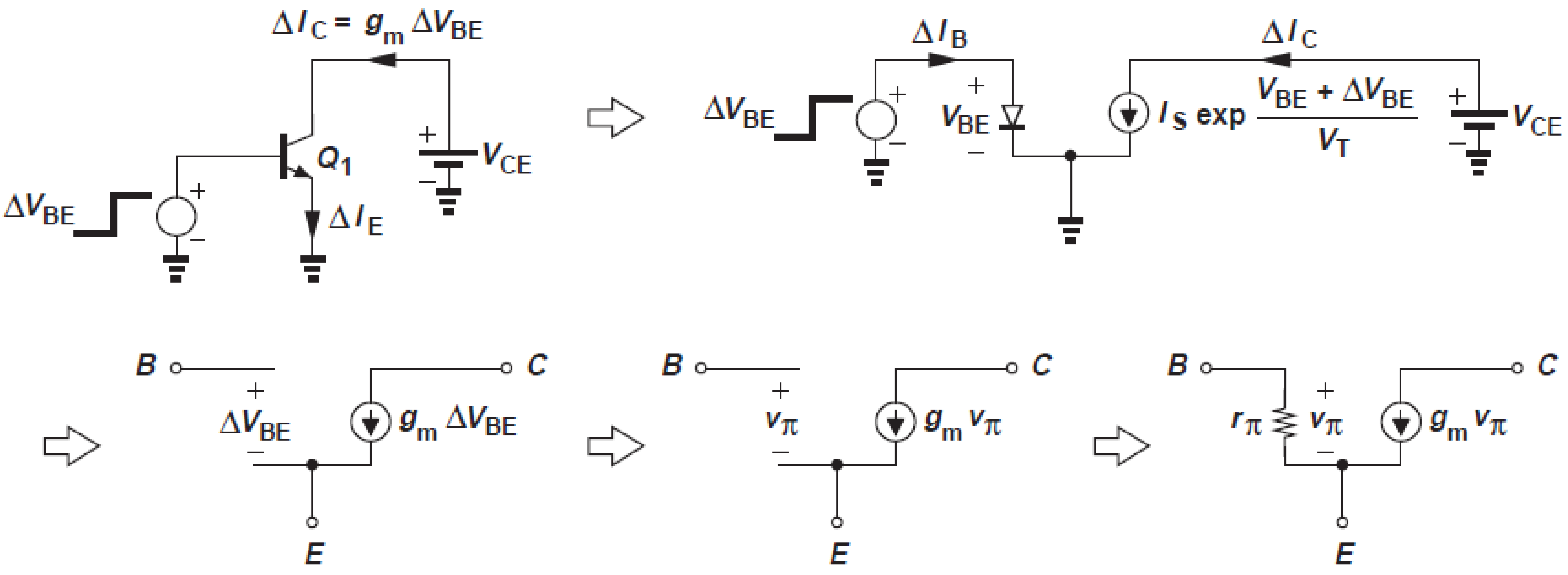


Figure 4.22 Development of small-signal model.

Physics of Bipolar Junction Transistors

❑Small-Signal Modeling

- ❑We know that

$$\Delta I_C = g_m \, \Delta V_{BE}$$

- ❑The change in V_{BE} creates a change in I_C but also creates a change in I_B

$$\Delta I_B = \frac{\Delta I_C}{\beta}$$

$$= \frac{g_m}{\beta} \Delta V_{BE}$$

- ❑The resistance between the base-emitter terminals is given by r_π

$$r_\pi = \frac{\Delta V_{BE}}{\Delta I_B}$$

$$= \frac{\beta}{g_m}.$$

Physics of Bipolar Junction Transistors

Small-Signal Modeling

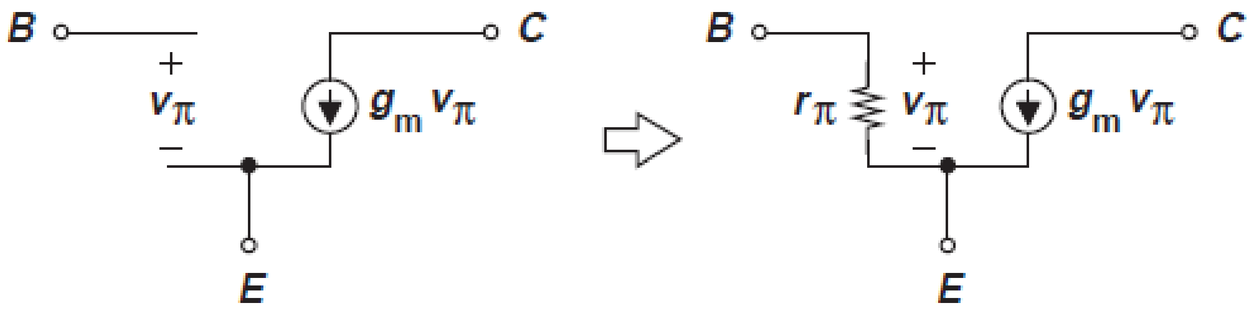
- This shows that the forward-biased diode between the base and the emitter is modeled by a small-signal resistance equal to β/g_m

- This result is expected because the diode carries a bias current equal to I_C / β and exhibits a small-signal resistance of $V_T / (I_C/\beta) = \beta (V_T/I_C) = \beta/g_m$

Physics of Bipolar Junction Transistors

❑Small-Signal Modeling

- ❑We now turn our attention to the collector and apply a voltage change with respect to the emitter i.e., from the output side
- ❑For a constant V_{BE}, the collector voltage has no effect on I_C or I_B because $I_C = I_S \exp(V_{BE}/V_T)$ and $I_B = I_C/\beta$
- ❑Since ΔV_{CE} leads to no change in any of the terminal currents, the model developed need not be altered

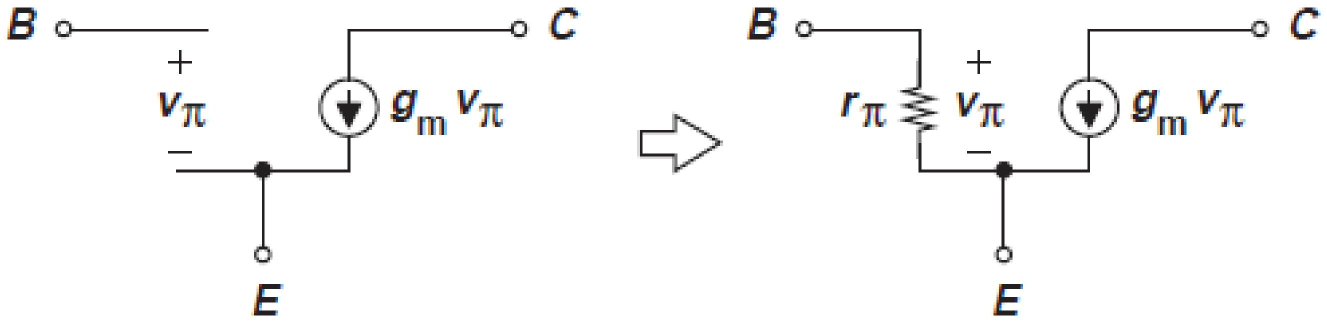


Physics of Bipolar Junction Transistors

❑Small-Signal Modeling

- ❑Both parameters of the model, g_m and r_π , depend on the bias current of the device

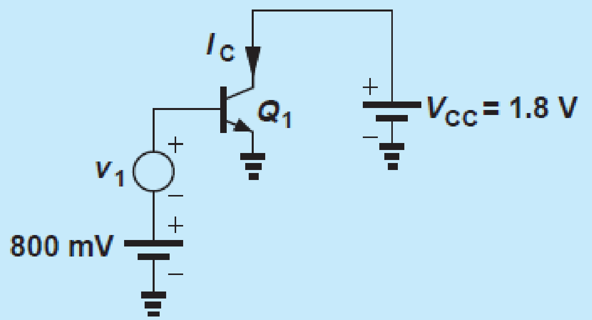
- ❑With a high collector bias current, a greater g_m is obtained, but the impedance between the base and emitter falls to lower values



Physics of Bipolar Junction Transistors

Example 4.10

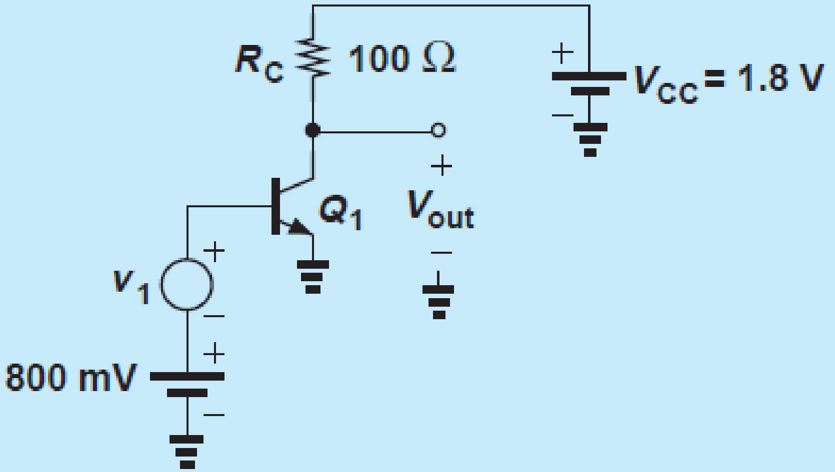
Consider the circuit shown in Fig. 4.24(a), where v_1 represents the signal generated by a microphone, $I_S = 3 \times 10^{-16}$ A, $\beta = 100$, and Q_1 operates in the active mode. (a) If $v_1 = 0$, determine the small-signal parameters of Q_1. (b) If the microphone generates a 1-mV signal, how much change is observed in the collector and base currents?



Physics of Bipolar Junction Transistors

Example 4.11

The circuit of Fig. 4.24 (a) is modified as shown in Fig. 4.25, where resistor R_C converts the collector current to a voltage. (a) Verify that the transistor operates in the active mode. (b) Determine the output signal level if the microphone produces a 1-mV signal.



Physics of Bipolar Junction Transistors

Example 4.12

Considering the circuit of Example 4.11, suppose we raise R_C to 200 Ω and V_{CC} to 3.6 V. Verify that the device operates in the active mode and compute the voltage gain.

Physics of Bipolar Junction Transistors

❑Early Effect

- ❑We have to incorporate the second order effects in our modeling to achieve a more realistic analysis
- ❑Early Effect is one of such effects that allows us to realize the practical picture of BJT amplifiers where the gain of the devices is “limited” instead of “infinite”

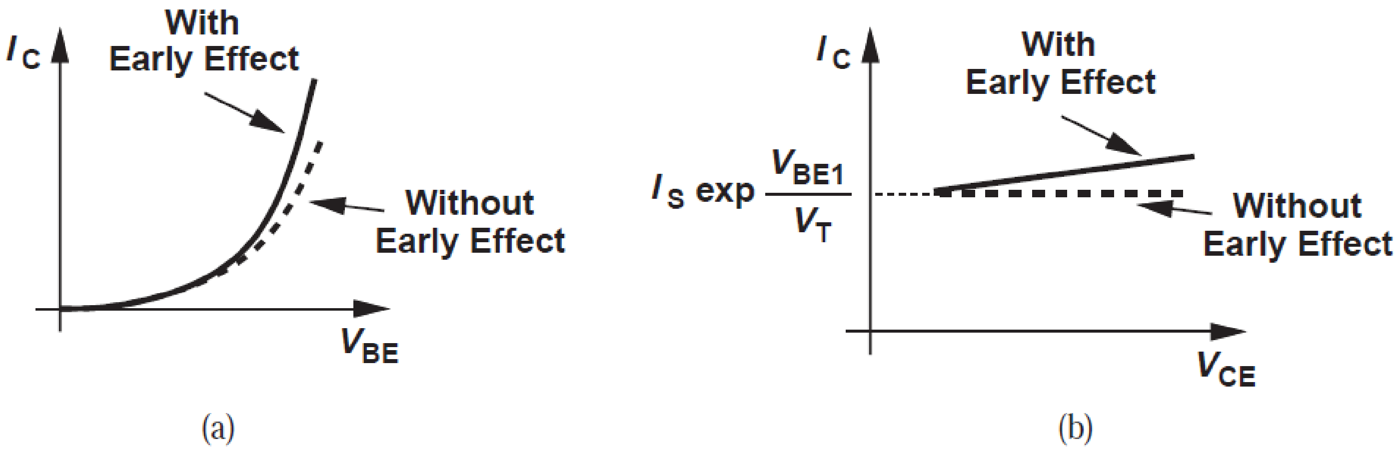


Figure 4.28 Collector current as a function of (a) V_{BE} and (b) V_{CE} with and without Early effect.

$$I_C = \frac{A_E q D_n n_i^2}{N_E W_B}\left(\exp \frac{V_{BE}}{V_T} - 1\right)\left(1 + \frac{V_{CE}}{V_A}\right),$$

$$\approx \left(I_S \exp \frac{V_{BE}}{V_T}\right)\left(1 + \frac{V_{CE}}{V_A}\right).$$

Physics of Bipolar Junction Transistors

❑Early Effect

- ❑The I_C – V_{CE} curves shows that the BJT transistor does not behave as a constant current source
- ❑The transistor can still be viewed as a two-terminal device but with a current that varies to some extent with V_{CE}

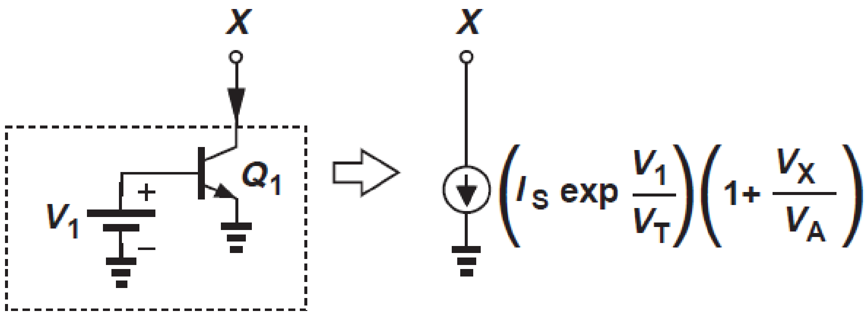


Figure 4.29 Realistic model of bipolar transistor as a current source.

$$I_C = \frac{A_E q D_n n_i^2}{N_E W_B}\left(\exp\frac{V_{BE}}{V_T} - 1\right)\left(1 + \frac{V_{CE}}{V_A}\right),$$

$$\approx \left(I_S \exp\frac{V_{BE}}{V_T}\right)\left(1 + \frac{V_{CE}}{V_A}\right).$$

Physics of Bipolar Junction Transistors

❑Early Effect – Large Signal Model

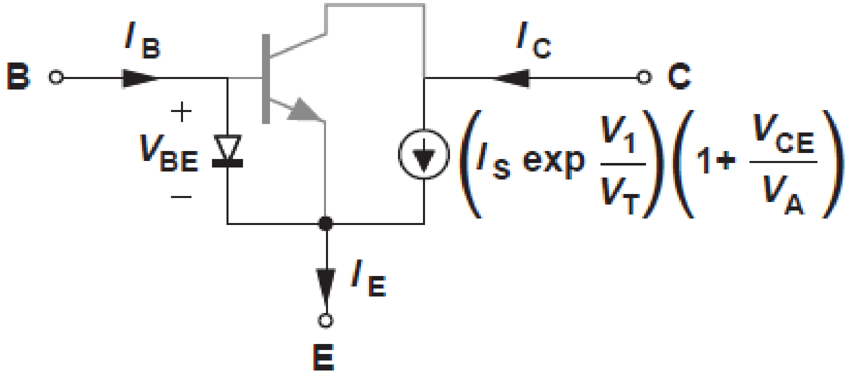


Figure 4.30 Large-signal model of bipolar transistor including Early effect.

$$I_C = \left(I_S \exp\frac{V_{BE}}{V_T}\right)\left(1+\frac{V_{CE}}{V_A}\right)$$

$$I_B = \frac{1}{\beta}\left(I_S \exp\frac{V_{BE}}{V_T}\right)$$

$$I_E = I_C + I_B.$$

Physics of Bipolar Junction Transistors

❑Early Effect – Small Signal Model

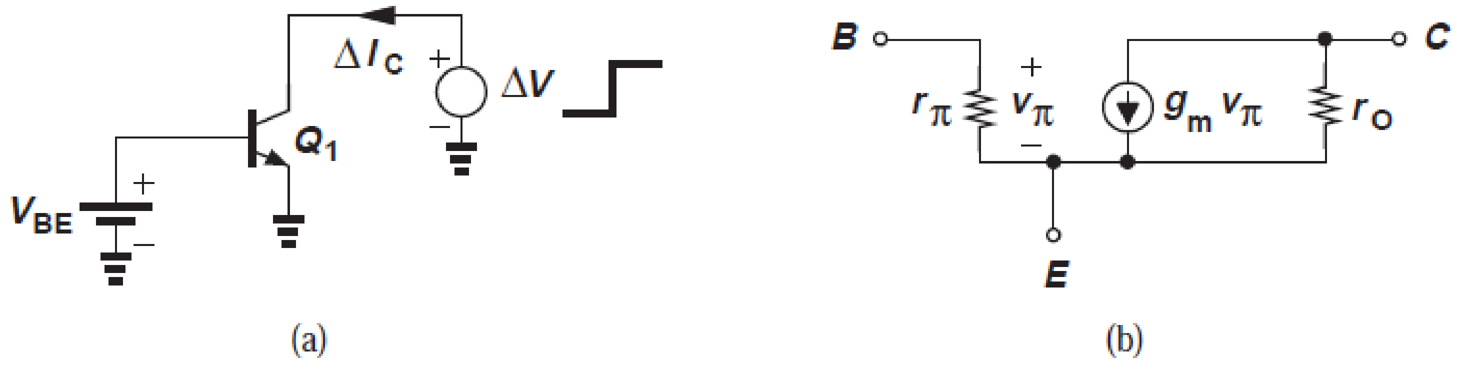


Figure 4.31 (a) Small change in V_{CE} and (b) small-signal model including Early effect.

$$r_O = \frac{\Delta V_{CE}}{\Delta I_C}$$

$$= \frac{V_A}{I_S \exp \frac{V_{BE}}{V_T}}$$

$$\approx \frac{V_A}{I_C}.$$

Physics of Bipolar Junction Transistors

❑Early Effect – Small Signal Model

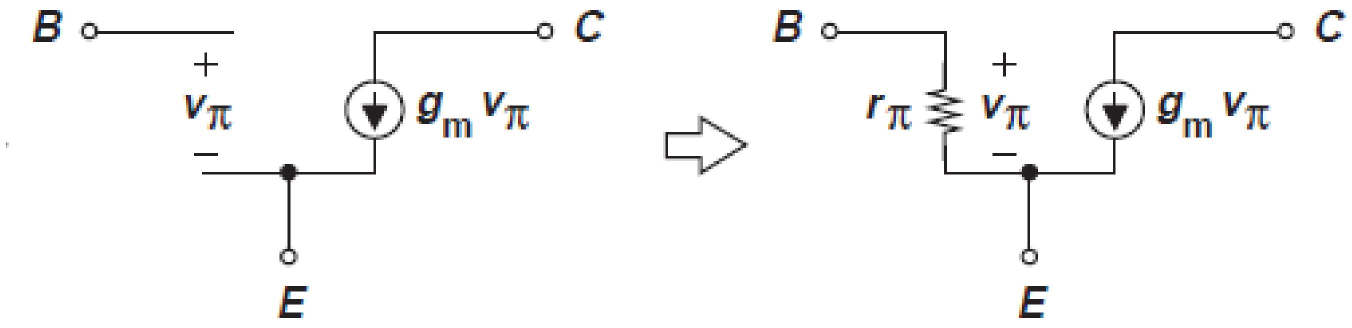
Example 4.14 A transistor is biased at a collector current of 1 mA. Determine the small-signal model if $\beta = 100$ and $V_A = 15$ V.

Physics of Bipolar Junction Transistors

❑Small-Signal Modeling

❑Both parameters of the model, g_m and r_π , depend on the bias current of the device

❑With a high collector bias current, a greater g_m is obtained, but the impedance between the base and emitter falls to lower values



$$\Delta I_C = g_m \, \Delta V_{BE}$$

$$\Delta I_B = \frac{\Delta I_C}{\beta}$$

$$= \frac{g_m}{\beta} \Delta V_{BE}$$

$$r_\pi = \frac{\Delta V_{BE}}{\Delta I_B}$$

$$= \frac{\beta}{g_m}.$$

Physics of Bipolar Junction Transistors

❑BJT Operation in Saturation Mode

Example 4.16

For the circuit of Fig. 4.36, determine the relationship between R_C and V_{CC} that guarantees operation in soft saturation or active region.

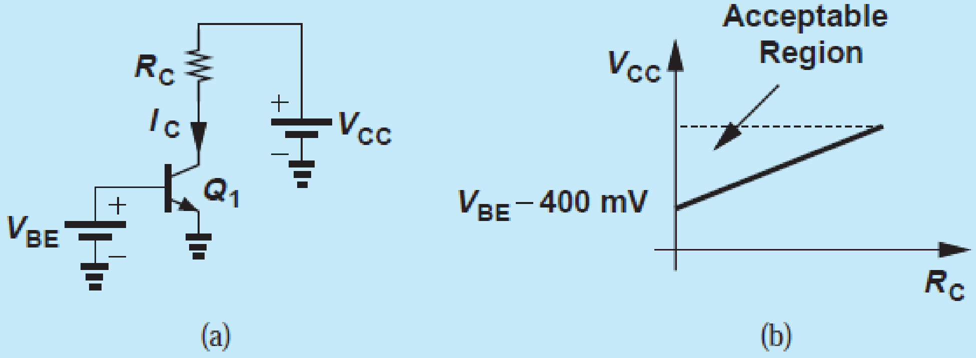
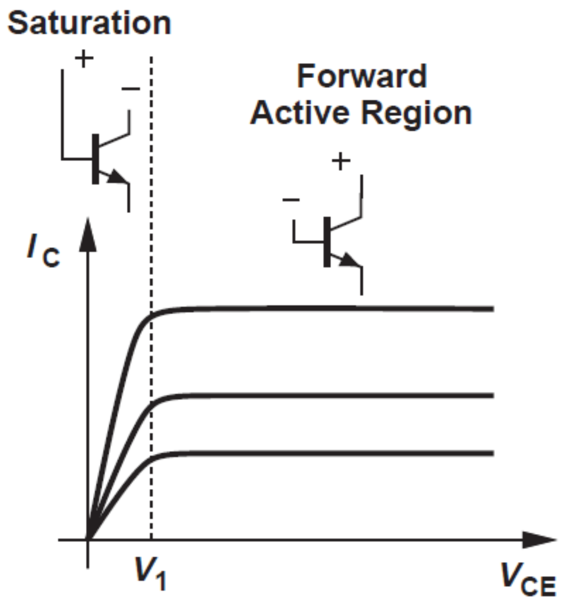


Figure 4.36 (a) Simple stage, (b) acceptable range of V_{CC} and R_C.



Chapter – 5

Bipolar Amplifiers

Bipolar Amplifiers

❑Input – Output Impedance of Amplifiers

❑Ideal Case

- ❑Input Impedance should be infinite
- ❑Output Impedance should be zero

❑Practical Case

- ❑Input Impedance should be maximized while design
- ❑Output Impedance should be minimized while design

Bipolar Amplifiers

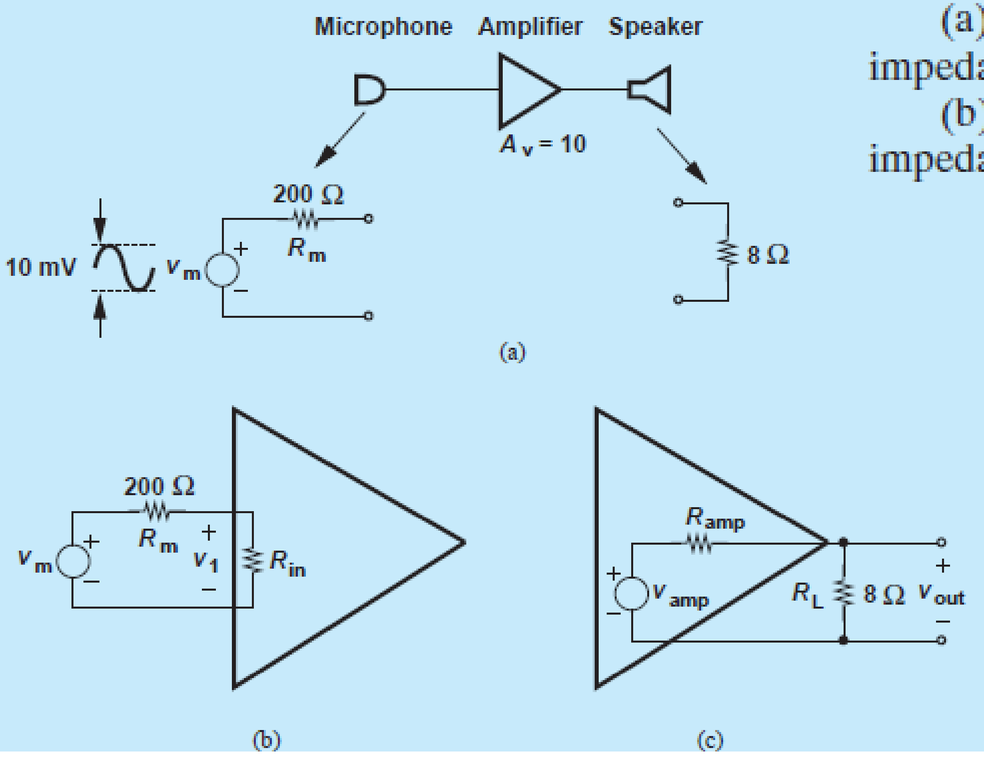
❑Input – Output Impedance of Amplifiers

Example 5.1

An amplifier with a voltage gain of 10 senses a signal generated by a microphone and applies the amplified output to a speaker [Fig. 5.1(a)]. Assume the microphone can be modeled with a voltage source having a 10-mV peak-to-peak signal and a series resistance of 200 Ω. Also assume the speaker can be represented by an 8-Ω resistor.

(a) Determine the signal level sensed by the amplifier if the circuit has an input impedance of 2 kΩ or 500 Ω.

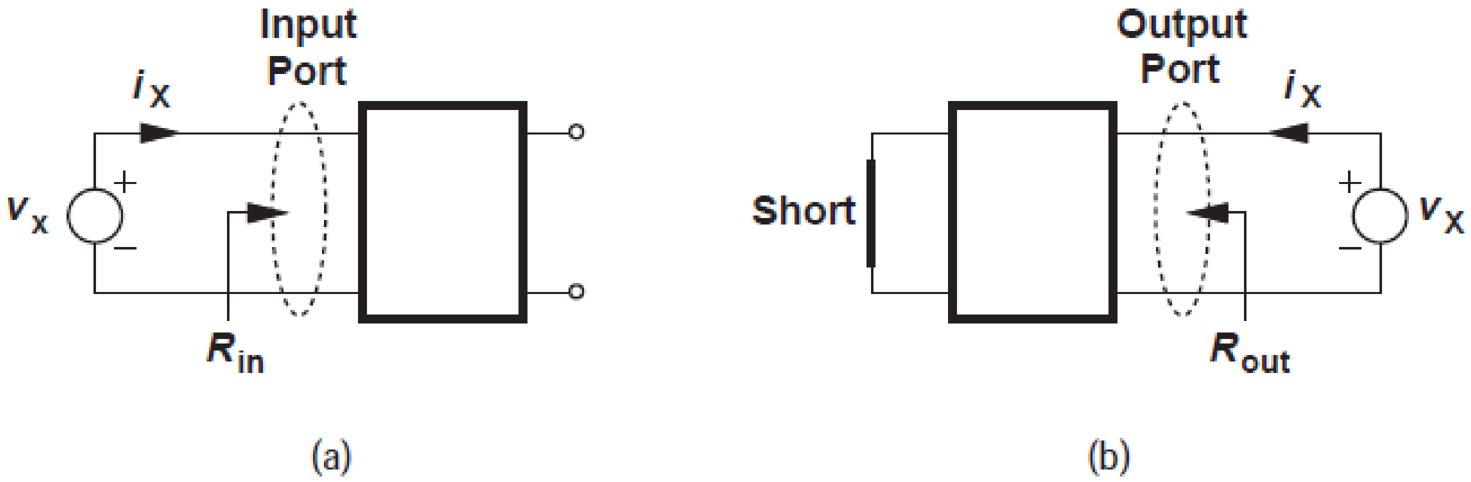
(b) Determine the signal level delivered to the speaker if the circuit has an output impedance of 10 Ω or 2 Ω.



Bipolar Amplifiers

❑Measurement of Input – Output Impedance

- ❑Remember the Thevenin's Theorem for finding the impedance

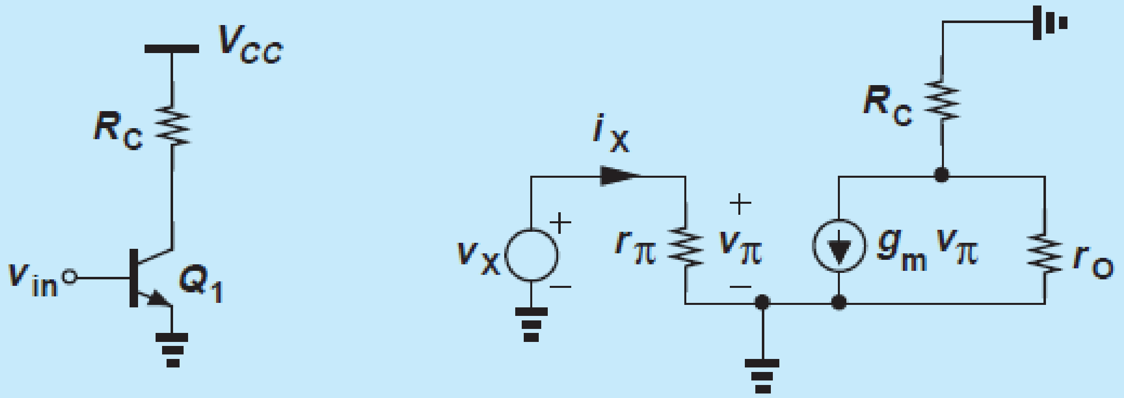


Measurement of (a) input and (b) output impedances.

Bipolar Amplifiers

❑Calculation of Input – Output Impedance

Example 5.2 Assuming that the transistor operates in the forward active region, determine the input impedance of the circuit shown in Fig. 5.3(a).



(a) (b)

Question: What happens when R_C is doubled ?

Bipolar Amplifiers

❑Calculation of Input – Output Impedance

Example 5.3

Calculate the impedance seen looking into the collector of Q_1 in Fig. 5.5(a).

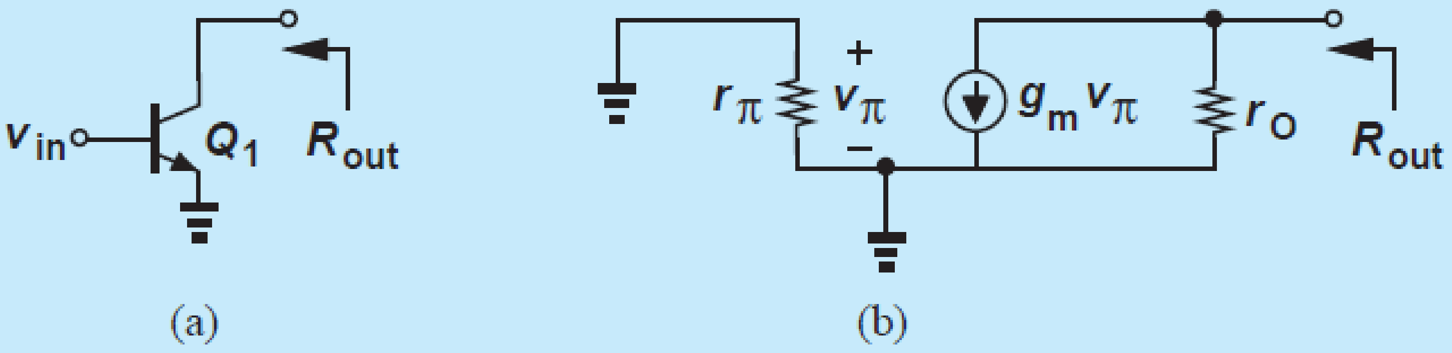


Figure 5.5 (a) Impedance seen at collector, (b) small-signal model.

Bipolar Amplifiers

❑Calculation of Input – Output Impedance

Example 5.4

Calculate the impedance seen at the emitter of Q_1 in Fig. 5.6(a). Neglect the Early effect for simplicity.

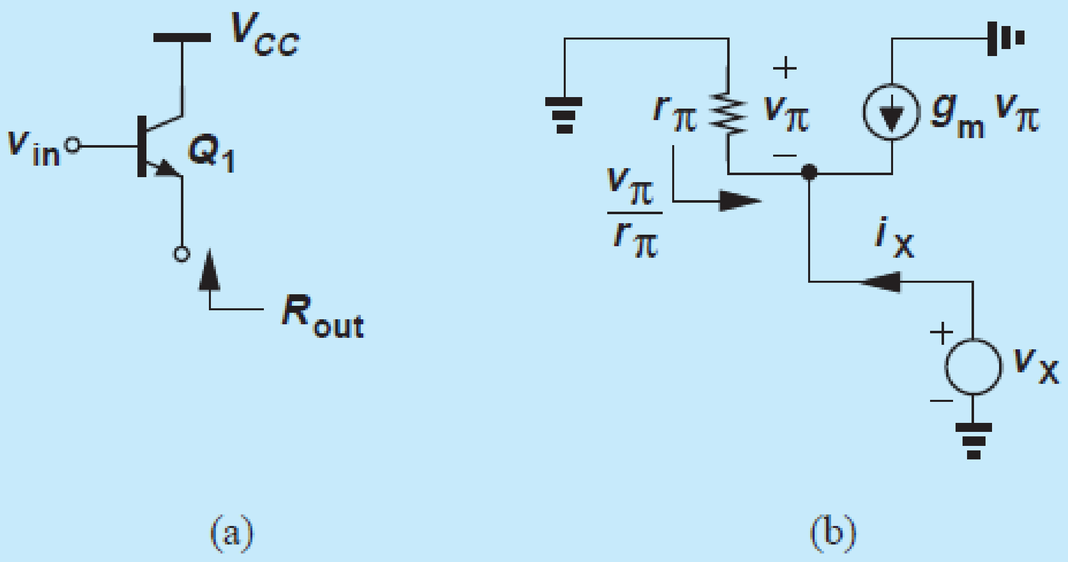
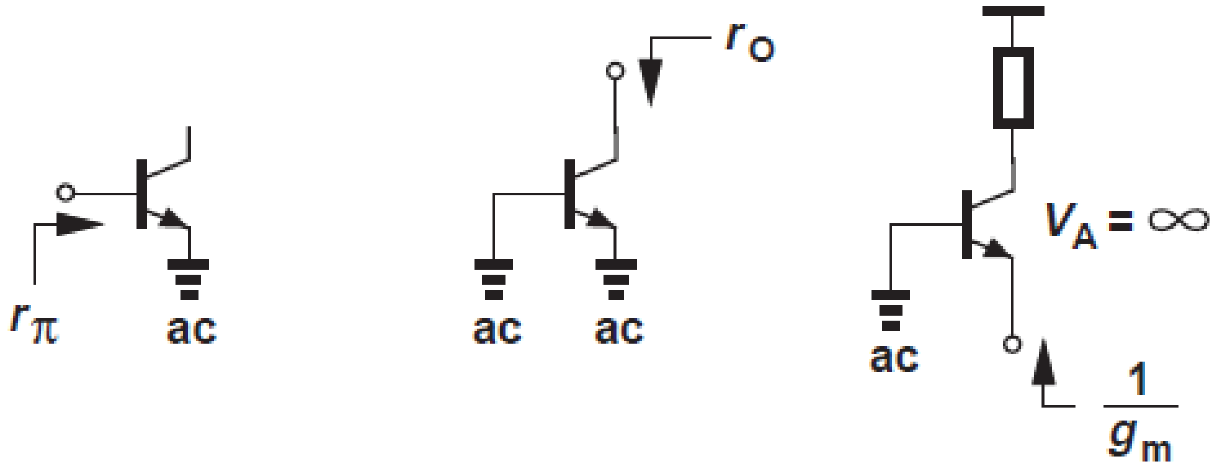


Figure 5.6 (a) Impedance seen at emitter, (b) small-signal model.

Bipolar Amplifiers

❑Summary – Calculation of Input – Output Impedance



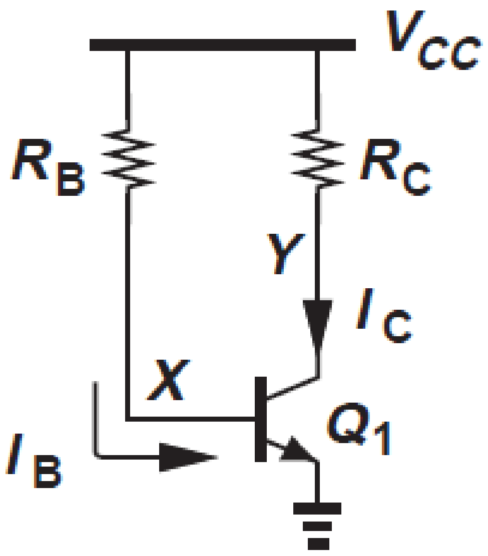
Summary of impedances seen at terminals of a transistor.

Bipolar Amplifiers

❑Biasing and Operating Point (Q-point) Analysis and Design

❑Common Emitter Stage

❑Case – 1 – Simple Biasing



Large Signal Analysis (DC – Analysis)

$$R_B I_B + V_{BE} = V_{CC}$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}.$$

$$I_C = \beta \frac{V_{CC} - V_{BE}}{R_B},$$

$$V_{CE} = V_{CC} - R_C I_C$$

$$= V_{CC} - \beta \frac{V_{CC} - V_{BE}}{R_B} R_C.$$

Design requirement to avoid saturation region operation

$$V_{CC} - \beta \frac{V_{CC} - V_{BE}}{R_B} R_C > V_{BE}.$$

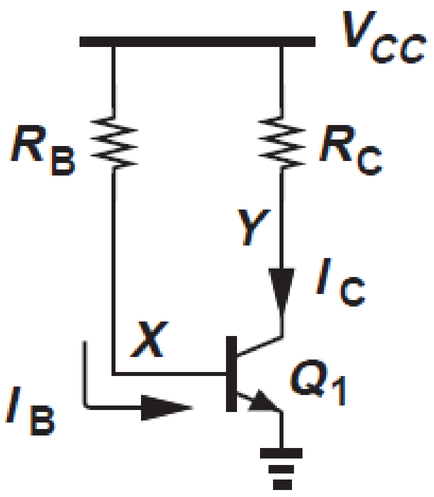
Bipolar Amplifiers

❑Biasing and Operating Point (Q-point) Analysis and Design

❑Case – 1 – Simple Biasing

❑Challenges

i. The bias is sensitive to V_{BE} variations
ii. The bias is sensitive to temperature variations
iii. I_C is highly dependent on β
iv. Uncertainty due to V_{BE} is very pronounced at low V_{CC}
   - ✓ $V_{CC} - V_{BE}$ determines the base current
   - ✓ Rarely used for low voltage designs which are very common in modern electronic systems



Bipolar Amplifiers

❑Biasing and Operating Point (Q-point) Analysis and Design

❑Common Emitter Stage

COMMON EMITTER BIAS CIRCUIT

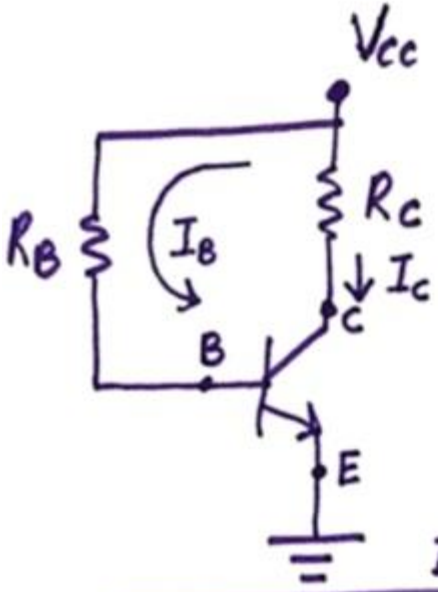
$$V_{BE} = 0.7\,V \ (Si)$$

$$V_{BE} = 0.3\,V \ (Ge)$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

$$I_C = \beta I_B$$

$$V_{CE} = V_{CC} - I_C R_C$$



DESIGN

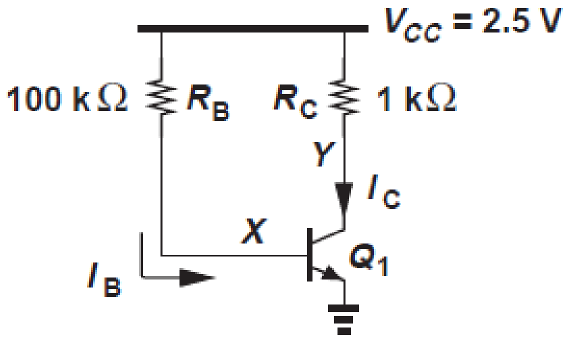
$$\boxed{\begin{aligned} R_B &= \frac{V_{CC} - V_{BE}}{I_C/\beta} \\ R_C &= \frac{V_{CC} - V_{CE}}{I_C} \end{aligned}}$$

Bipolar Amplifiers

❑Biasing and Operating Point (Q-point) Analysis and Design

Example 5.7

For the circuit shown in Fig. 5.14, determine the collector bias current. Assume $\beta = 100$ and $I_S = 10^{-17}$ A. Verify that Q_1 operates in the forward active region.



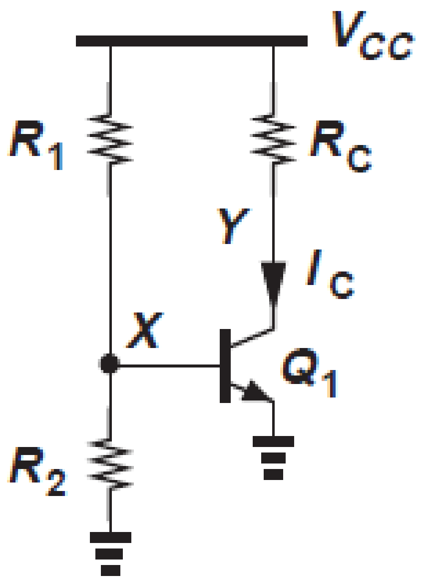
Assume $\mathbf{V_{BE} = 800\ mV}$

Bipolar Amplifiers

❑Biasing and Operating Point (Q-point) Analysis and Design

❑Common Emitter Stage

❑Case – 2a – Resistor-Divider Biasing without degenerate (Emitter) resistance R_E

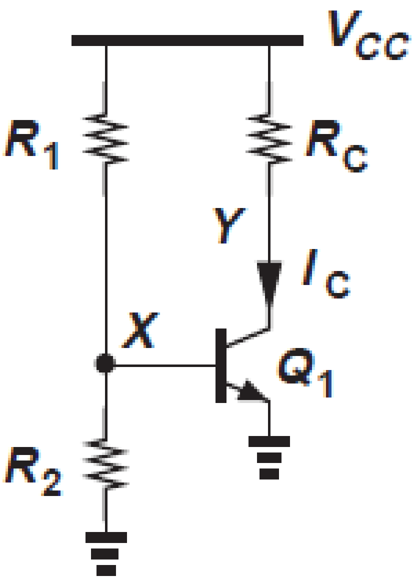


Bipolar Amplifiers

❑Biasing and Operating Point (Q-point) Analysis and Design

❑Common Emitter Stage – Analysis (Simple Method)

❑Case – 2a – Resistor-Divider Biasing without degenerate (Emitter) resistance R_E



$$V_X = \frac{R_2}{R_1 + R_2} V_{CC},$$

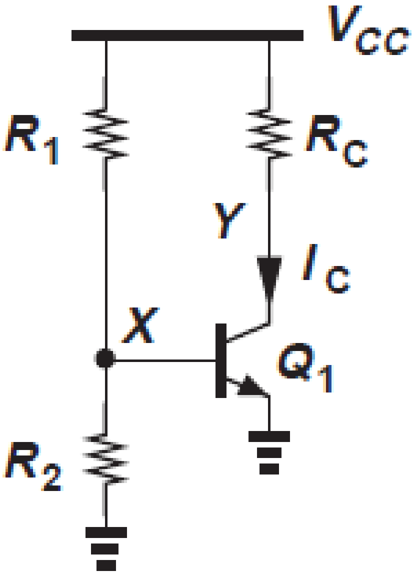
$$I_C = I_S \exp\left(\frac{R_2}{R_1 + R_2} \cdot \frac{V_{CC}}{V_T} \right),$$

Bipolar Amplifiers

❑Biasing and Operating Point (Q-point) Analysis and Design

❑Common Emitter Stage – Analysis (Accurate Method)

❑Case – 2a – Resistor-Divider Biasing without degenerate (Emitter) resistance R_E

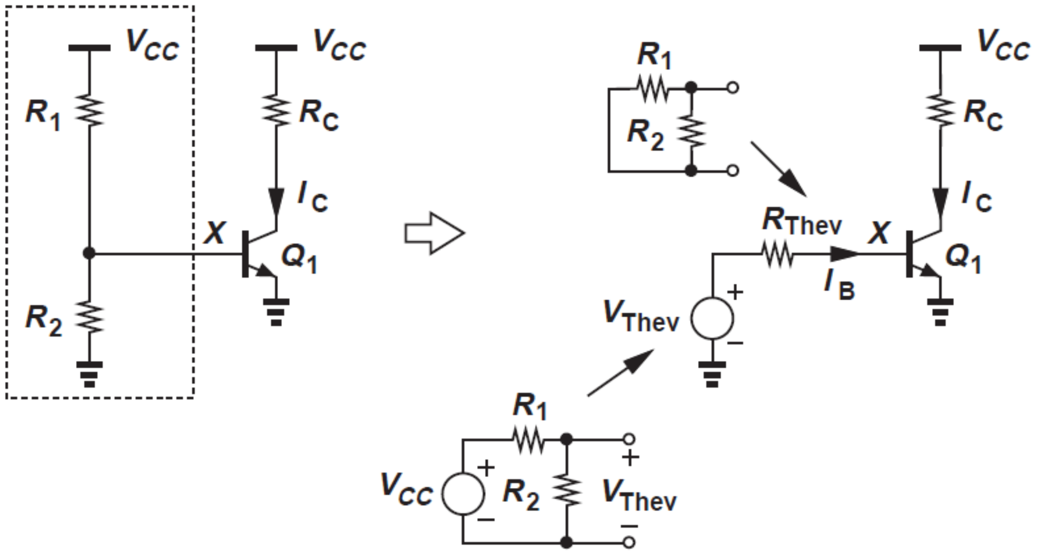


$$V_{Thev} = \frac{R_2}{R_1 + R_2} V_{CC}.$$

$$R_{Thev} = R_1 || R_2.$$

$$V_X = V_{Thev} - I_B R_{Thev}$$

$$I_C = I_S \exp \frac{V_{Thev} - I_B R_{Thev}}{V_T}.$$



Bipolar Amplifiers

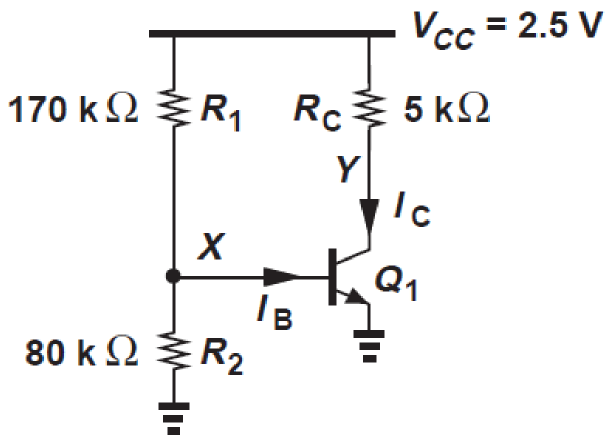
❑Biasing and Operating Point (Q-point) Analysis and Design

❑Common Emitter Stage - Analysis

❑Case – 2a – Resistor-Divider Biasing without degenerate (Emitter) resistance R_E

Example 5.9

Calculate the collector current of Q_1 in Fig. 5.18(a). Assume $\beta = 100$ and $I_S = 10^{-17}$ A.



Assume V_{BE} = 750mV

Bipolar Amplifiers

❑Biasing and Operating Point (Q-point) Analysis and Design

❑Common Emitter Stage – Advantages and Challenges

❑Case – 2a – Resistor-Divider Biasing without degenerate (Emitter) resistance R_E

- ❑ Proper selection of R_1 and R_2 will make the circuit topology insensitive to β
- ❑ The I_C still has exponential dependence to the voltage generated across the R_2 resistance i.e., V_{BE}
- ❑ Variations in the resistance values R_1 and R_2 will result in significant variation in the I_C values
  - ❑ **For example:** 1% variation in the resistor values shall result in ~ 36% variation in the desired I_C value

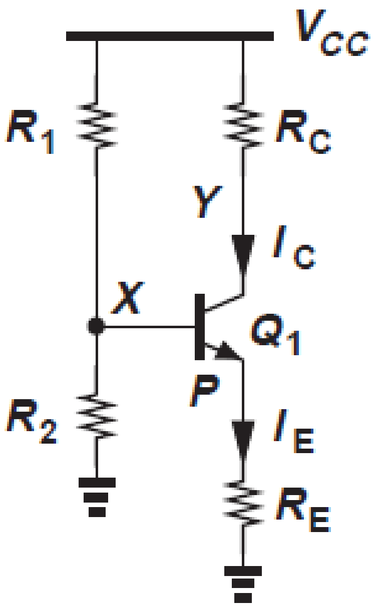
❑These problems can be adjusted by adding a resistance with the emitter in series i.e., R_E

Bipolar Amplifiers

❑Biasing and Operating Point (Q-point) Analysis and Design

❑Common Emitter Stage

❑Case – 2b – Resistor-Divider Biasing with degenerate (Emitter) resistance R_E



Bipolar Amplifiers

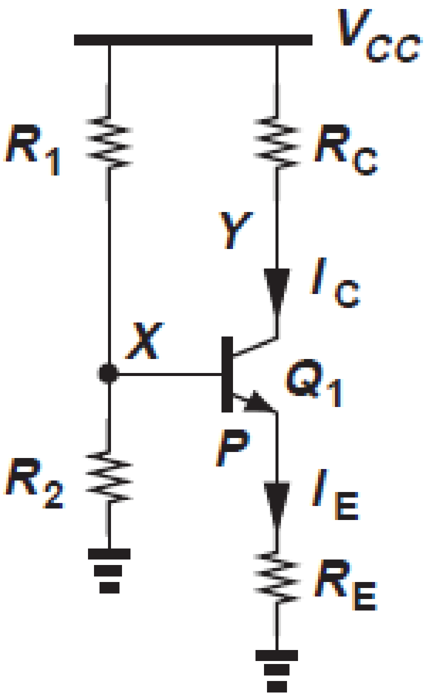
❑Biasing and Operating Point (Q-point) Analysis and Design

❑Common Emitter Stage – Analysis

❑Case – 2b – Resistor-Divider Biasing with degenerate (Emitter) resistance R_E

$V_{cc} = 12V$
$R_1 = 8.2k\Omega$
$R_2 = 3.9K\Omega$
$R_c = 1K\Omega$
$R_E = 1k\Omega$

$\beta = 100$
$V_{BE} = 0.7$ (Si)

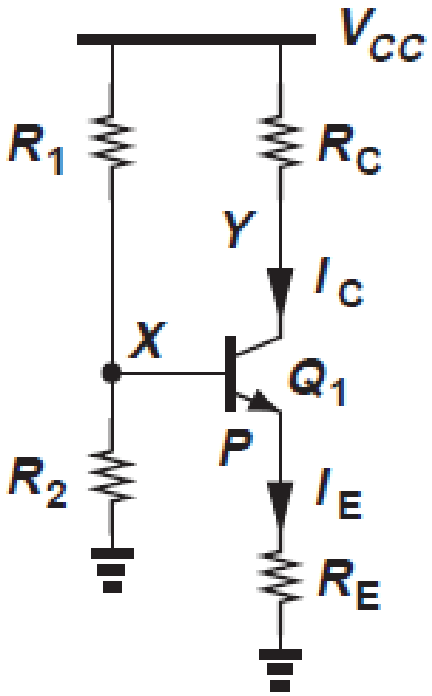


Bipolar Amplifiers

❑Biasing and Operating Point (Q-point) Analysis and Design

❑Common Emitter Stage - Analysis (using Accurate Approach)

❑Case – 2b – Resistor-Divider Biasing with degenerate (Emitter) resistance R_E



Bipolar Amplifiers

❑Biasing and Operating Point (Q-point) Analysis and Design

❑Common Emitter Stage - Design Approach # 1

❑Case – 2b – Resistor-Divider Biasing with degenerate (Emitter) resistance R_E

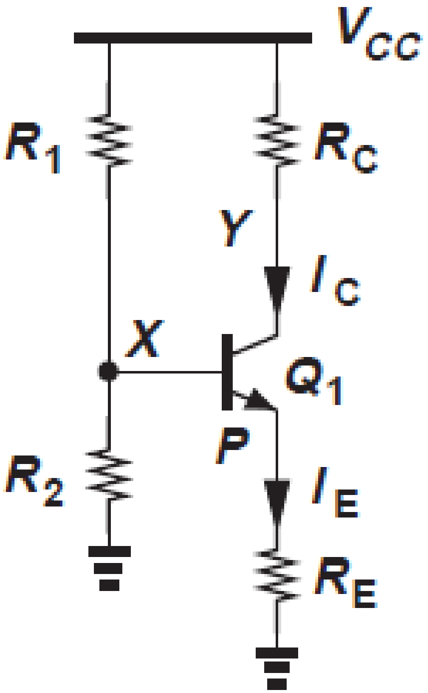
DESIGN PROBLEM:

$\beta = 100$, $I_{C,Q} = 5mA$

$V_{CE,Q} = 8V$, $V_{CC} = 20V$

$V_{BE} = 0.7$ (Si)

$V_E = 20\%$ of V_{CC}



Condition

$(1+\beta) R_E >> R_B$

Bipolar Amplifiers

❑Biasing and Operating Point (Q-point) Analysis and Design

❑Common Emitter Stage - Design Approach # 2

❑Case – 2b – Resistor-Divider Biasing with degenerate (Emitter) resistance R_E

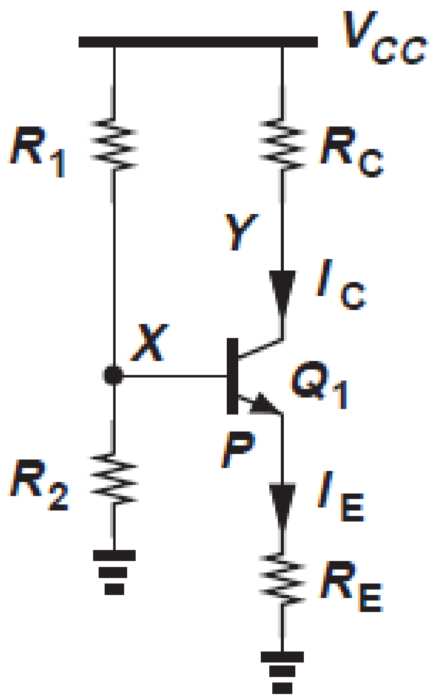
DESIGN PROBLEM:

$\beta = 100$, $I_{C,Q} = 5mA$

$V_{CE,Q} = 8V$, $V_{cc} = 20V$

$V_{BE} = 0.7$ (Si)

$V_E = 20\%$ of V_{cc}



Condition for Design

$\boxed{I_1 >> I_B}$

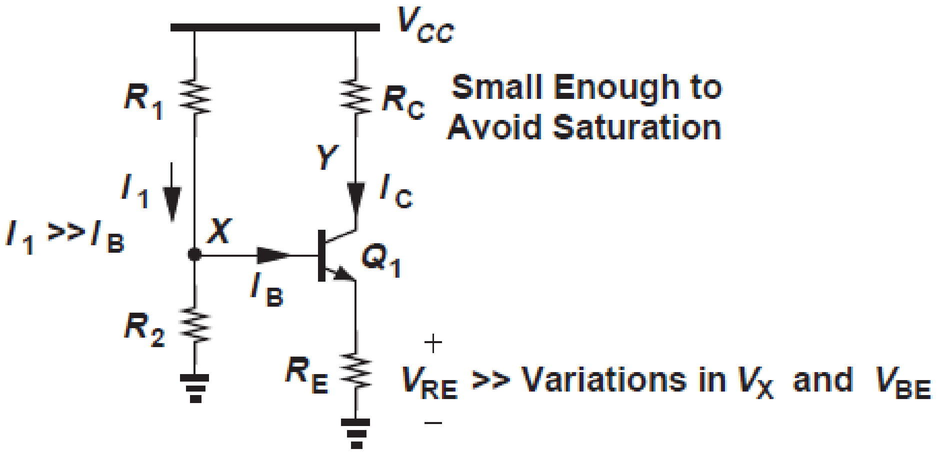
Bipolar Amplifiers

❑Biasing and Operating Point (Q-point) Analysis and Design

❑Common Emitter Stage – Advantages and Challenges

❑Case – 2b – Resistor-Divider Biasing with degenerate (Emitter) resistance R_E

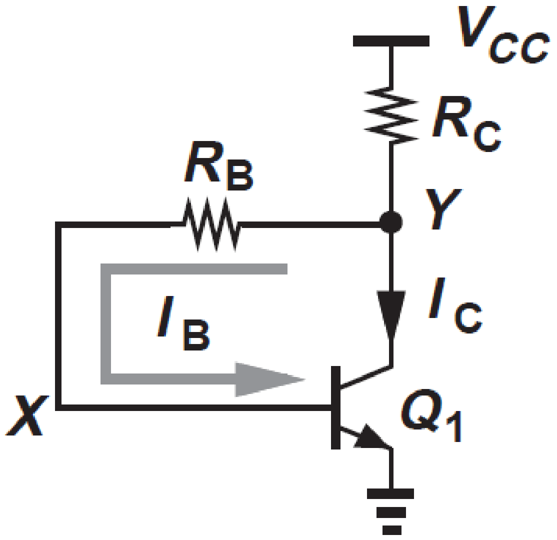
- ❑This bias topology is extensively used in the discrete circuits and occasionally in the integrated circuits
- ❑The rules for design are
  1. $I_1 >> I_B$ to lower the sensitivity of β
  2. V_{RE} must be large enough (~ 100mV or above) to suppress the effect of uncertainties in V_X and V_{BE}



Bipolar Amplifiers

❑Biasing and Operating Point (Q-point) Analysis and Design

❑Self-Biased Stage – Analysis



We now determine the collector bias current by assuming $I_B \ll I_C$; i.e., R_C carries a current equal to I_C, thereby yielding

$$V_Y = V_{CC} - R_C I_C. \tag{5.75}$$

Also,

$$V_Y = R_B I_B + V_{BE} \tag{5.76}$$

$$= \frac{R_B I_C}{\beta} + V_{BE}. \tag{5.77}$$

Equating the right-hand sides of Eqs. (5.75) and (5.77) gives

$$I_C = \frac{V_{CC} - V_{BE}}{R_C + \dfrac{R_B}{\beta}}. \tag{5.78}$$

Bipolar Amplifiers

❑Biasing and Operating Point (Q-point) Analysis and Design

❑Self-Biased Stage – Analysis Example

Problem:

Analyze a self-bias circuit with the following values, with and without R_E

$R_C = R_E = 1\ k\Omega$

$R_B = 150\ k\Omega$

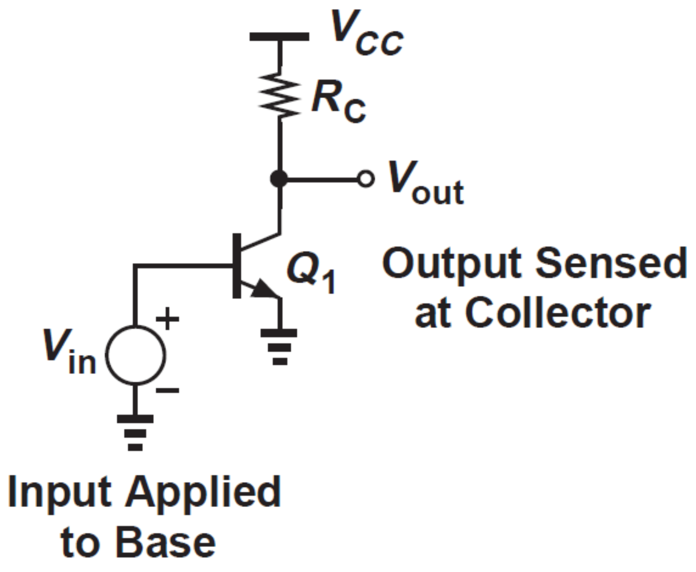
$V_{CC} = 15$

$\beta = 150$

Bipolar Amplifiers

❑BJT Amplifier Topologies

- ❑There are three commonly used topologies for the BJTs
  1. **Common-Emitter (CE) Topology**
  2. Common-Base (CB) Topology
  3. Common-Collector Topology
- ❑In this course we shall only be focusing towards Common-Emitter (CE) Topology

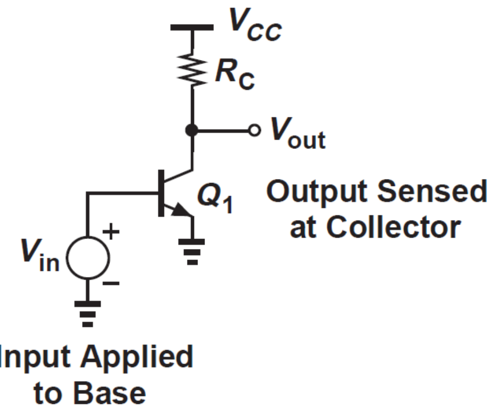


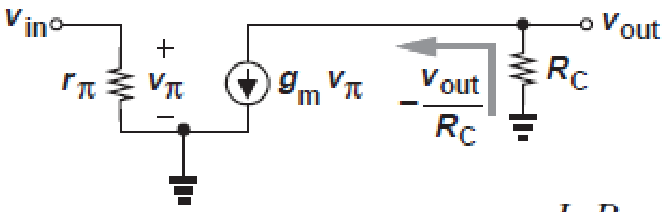
Bipolar Amplifiers

❑BJT Amplifier Topologies

❑Common-Emitter (CE) Topology

❑Small Signal Analysis





Small-signal model of CE stage.

$$A_v = -g_m R_C.$$

$$|A_v| = \frac{I_C R_C}{V_T}$$

$$= \frac{V_{RC}}{V_T}.$$

Since $V_{RC} < V_{CC}$,

$$|A_v| < \frac{V_{CC}}{V_T}.$$

Furthermore, the transistor itself requires a minimum collector-emitter voltage of about V_{BE} to remain in the active region, lowering the limit to

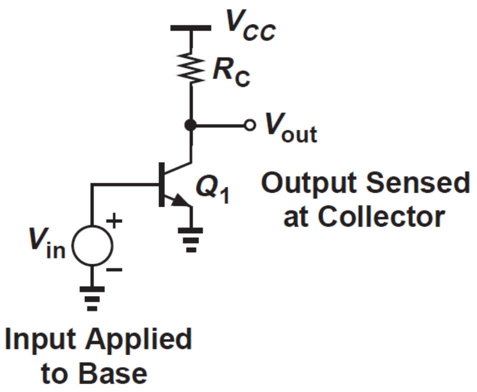
$$|A_v| < \frac{V_{CC} - V_{BE}}{V_T}.$$

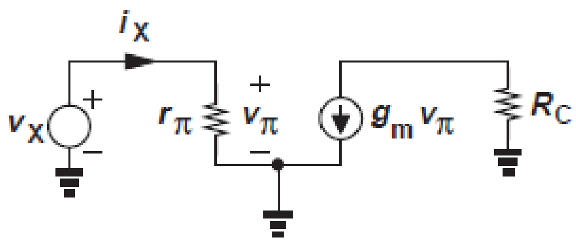
Bipolar Amplifiers

❑BJT Amplifier Topologies

❑Common-Emitter (CE) Topology

❑Small Signal Analysis – Input Impedance Calculation





$$R_{in} = \frac{v_X}{i_X}$$

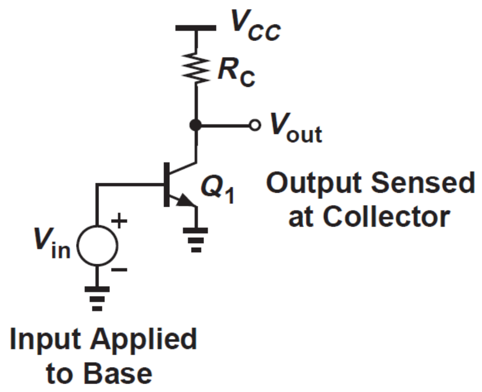
$$= r_\pi .$$

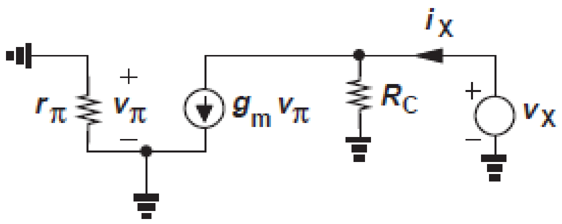
Bipolar Amplifiers

❑BJT Amplifier Topologies

❑Common-Emitter (CE) Topology

❑Small Signal Analysis – Output Impedance Calculation





$$R_{out} = \frac{v_X}{i_X}$$

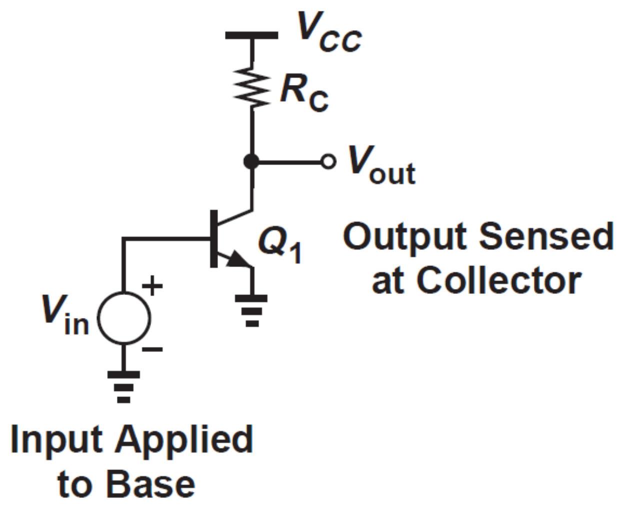
$$= R_C.$$

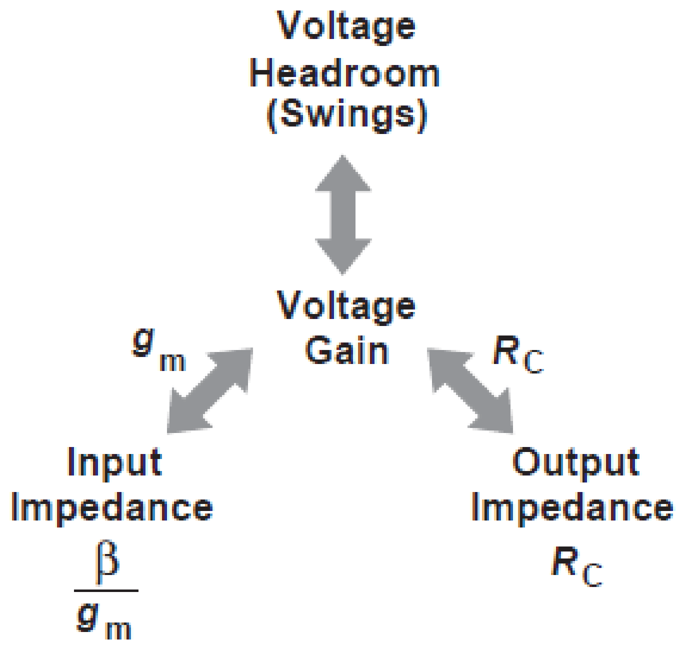
Bipolar Amplifiers

❑BJT Amplifier Topologies

❑Common-Emitter (CE) Topology – CE Stage Trade Offs

Figure 5.33 summarizes the trade-offs in the performance of the CE topology along with the parameters that create such trade-offs. For example, for a given value of output impedance, R_C is fixed and the voltage gain can be increased by increasing I_C, thereby lowering both the voltage headroom and the input impedance.



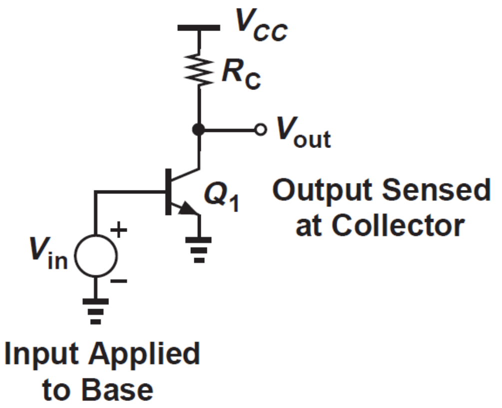


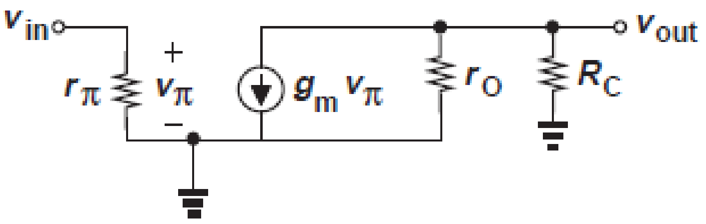
Bipolar Amplifiers

❑BJT Amplifier Topologies

❑Common Emitter Topology

❑With Early Effect





CE stage including Early effect.

$$R_{in} = r_\pi$$

$$R_{out} = R_C || r_O.$$

$$A_v = -g_m(R_C || r_O).$$

$$A_I = \frac{i_{out}}{i_{in}},$$

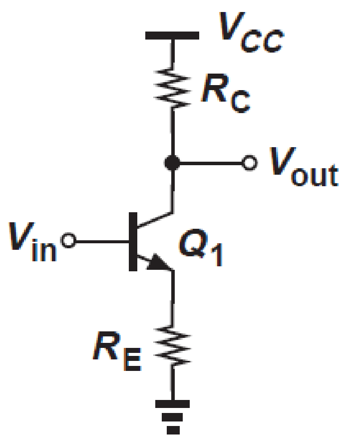
Bipolar Amplifiers

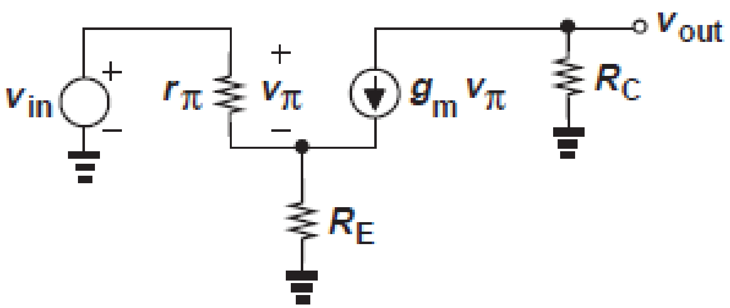
❑BJT Amplifier Topologies

❑Common Emitter Topology

❑With Emitter Degenerate Resistance R_E (without Early Effect)

❑ **Small-Signal Model**





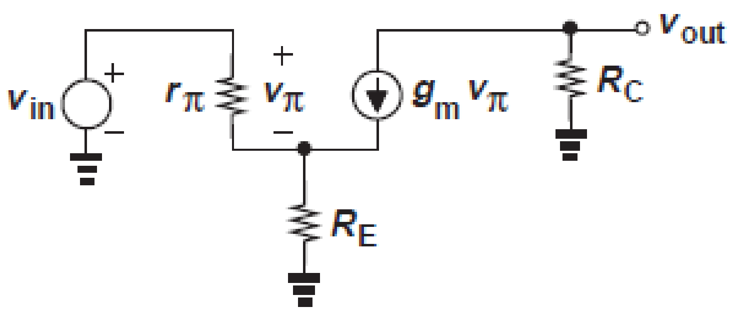
Bipolar Amplifiers

❑BJT Amplifier Topologies

❑Common Emitter Topology

❑With Emitter Degenerate Resistance R_E (without Early Effect)

❑ Voltage Gain Calculation



$$v_{in} = v_\pi + v_{RE}$$

$$= v_\pi + \left(\frac{v_\pi}{r_\pi} + g_m v_\pi\right) R_E$$

$$= v_\pi \left[1 + \left(\frac{1}{r_\pi} + g_m\right) R_E\right].$$

$$\boxed{\frac{v_{out}}{v_{in}} = -\frac{g_m R_C}{1 + \left(\frac{1}{r_\pi} + g_m\right) R_E}.}$$

@ Output Node (Apply KCL)

$$g_m v_\pi = -\frac{v_{out}}{R_C},$$

$$v_\pi = -\frac{v_{out}}{g_m R_C}.$$

Voltage drop across R_E

$$v_{RE} = \left(\frac{v_\pi}{r_\pi} + g_m v_\pi\right) R_E.$$

For β >> 1 , results in $g_m >> 1 / r_\pi$

$$\boxed{A_v = -\frac{g_m R_C}{1 + g_m R_E}.}$$

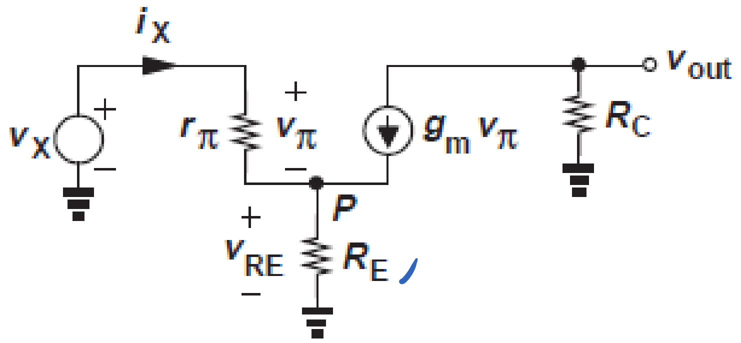
Bipolar Amplifiers

❑BJT Amplifier Topologies

❑Common Emitter Topology

❑With Emitter Degenerate Resistance R_E (without Early Effect)

- ❑ <u>Input Resistance Calculation</u>



$$v_X = r_\pi i_X + R_E(1+\beta)i_X,$$

$$R_{in} = \frac{v_X}{i_X}$$

$$= r_\pi + (\beta + 1)R_E.$$

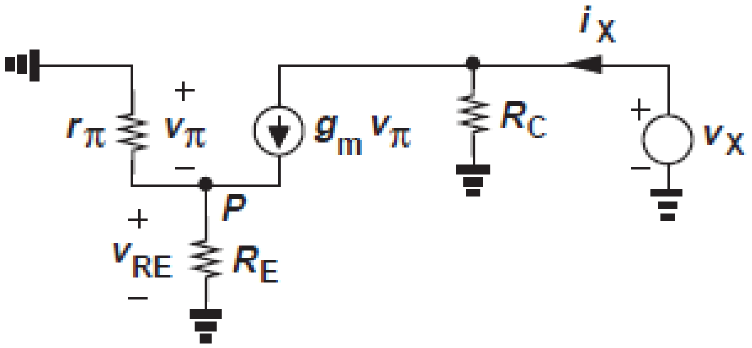
Bipolar Amplifiers

❑BJT Amplifier Topologies

❑Common Emitter Topology

❑With Emitter Degenerate Resistance R_E (without Early Effect)

❑ **Output Resistance Calculation**



$$v_{in} = 0 = v_\pi + \left(\frac{v_\pi}{r_\pi} + g_m v_\pi\right) R_E,$$

yielding $v_\pi = 0$ and hence $g_m v_\pi = 0$. Thus, all of i_X flows through R_C, and

$$R_{out} = \frac{v_X}{i_X}$$
$$= R_C,$$

Bipolar Amplifiers

❑BJT Amplifier Topologies

❑Common Emitter Topology

❑With Emitter Degenerate Resistance R_E (without Early Effect)

❑ Advantages of Emitter Degenerate Resistance (R_E)

✓ If $g_m R_E >> 1$, the voltage gain becomes independent of transconductance (g_m) and in effect, the biasing current I_C

$$A_v \to -R_C/R_E$$

Bipolar Amplifiers

❑BJT Amplifier Topologies

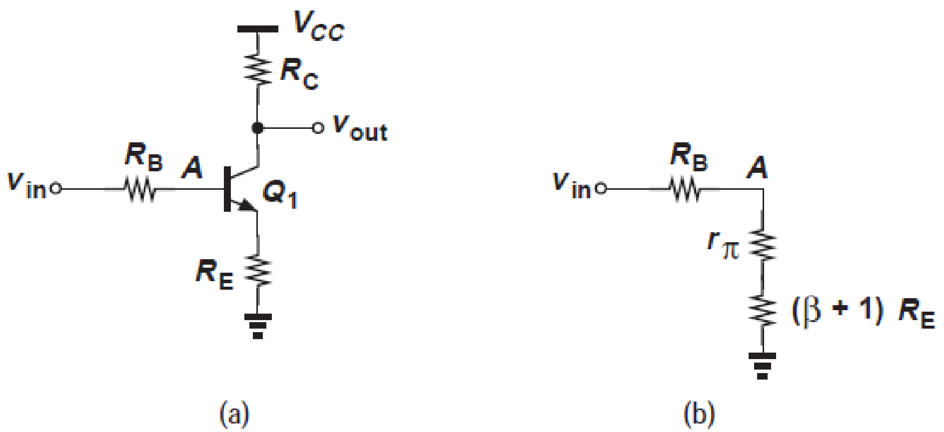
❑Common Emitter Topology

❑With Emitter Degenerate Resistance R_E (without Early Effect) and Base Resistance (R_B)

❑ **Analysis**

To analyze the small-signal behavior of this stage, we can adopt one of two approaches: (a) draw the small-signal model of the entire circuit and solve the resulting equations, or (b) recognize that the signal at node A is simply an attenuated version of v_{in} and write

$$\boxed{\frac{v_{out}}{v_{in}} = \frac{v_A}{v_{in}} \cdot \frac{v_{out}}{v_A}}.$$



(a) CE stage with base resistance, (b) equivalent circuit.

$$\frac{v_A}{v_{in}} = \frac{r_\pi + (\beta + 1)R_E}{r_\pi + (\beta + 1)R_E + R_B}.$$

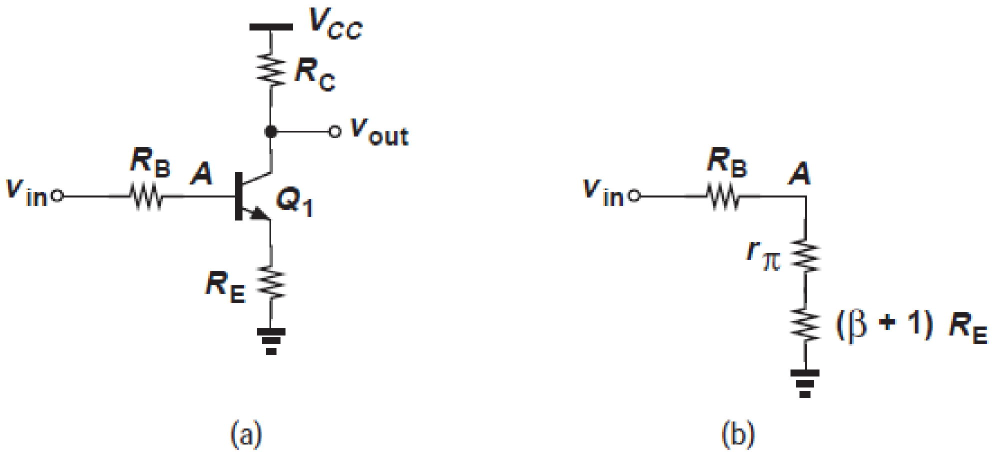
Bipolar Amplifiers

❑BJT Amplifier Topologies

❑Common Emitter Topology

❑With Emitter Degenerate Resistance R_E (without Early Effect) and Base Resistance (R_B)

❑ Analysis



(a) CE stage with base resistance, (b) equivalent circuit.

$$\boxed{\frac{v_{out}}{v_{in}} = \frac{v_A}{v_{in}} \cdot \frac{v_{out}}{v_A}.}$$

$$\frac{v_A}{v_{in}} = \frac{r_\pi + (\beta+1)R_E}{r_\pi + (\beta+1)R_E + R_B}.$$

$$\frac{v_{out}}{v_{in}} = \frac{r_\pi + (\beta+1)R_E}{r_\pi + (\beta+1)R_E + R_B} \cdot \frac{-g_m R_C}{1 + \left(\frac{1}{r_\pi} + g_m\right)R_E}$$

$$= \frac{r_\pi + (\beta+1)R_E}{r_\pi + (\beta+1)R_E + R_B} \cdot \frac{-g_m r_\pi R_C}{r_\pi + (1+\beta)R_E}$$

$$= \frac{-\beta R_C}{r_\pi + (\beta+1)R_E + R_B}.$$

$$\boxed{A_v \approx \frac{-R_C}{\frac{1}{g_m} + R_E + \frac{R_B}{\beta+1}}.}$$

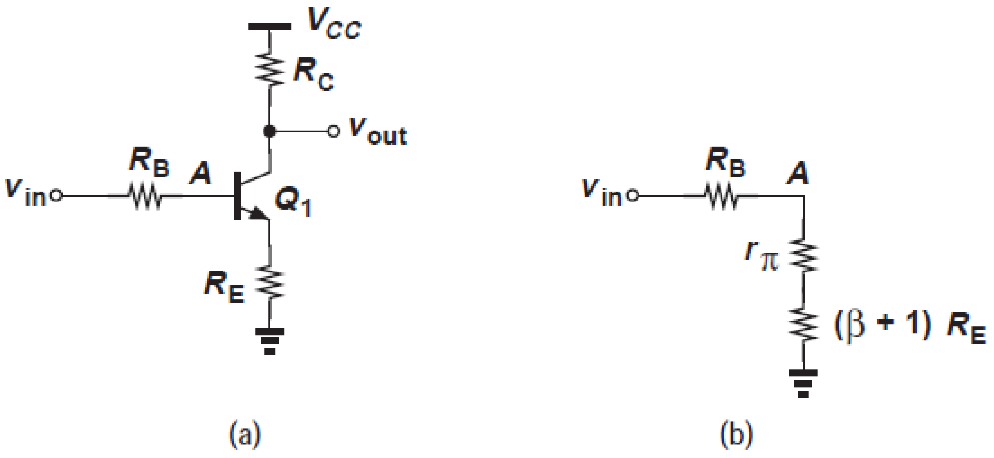
Bipolar Amplifiers

❑BJT Amplifier Topologies

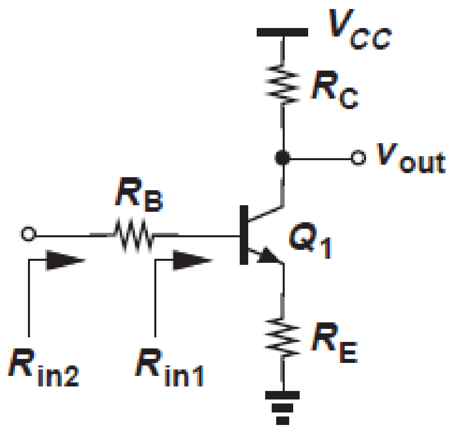
❑Common Emitter Topology

❑With Emitter Degenerate Resistance R_E (without Early Effect) and Base Resistance (R_B)

❑ **Analysis**



(a) CE stage with base resistance, (b) equivalent circuit.



$$R_{in1} = r_\pi + (\beta + 1)R_E$$

$$R_{in2} = R_B + r_\pi + (\beta + 1)R_E.$$

$$R_{out} = R_C$$

Bipolar Amplifiers

❑BJT Amplifier Topologies

❑Common Emitter Topology

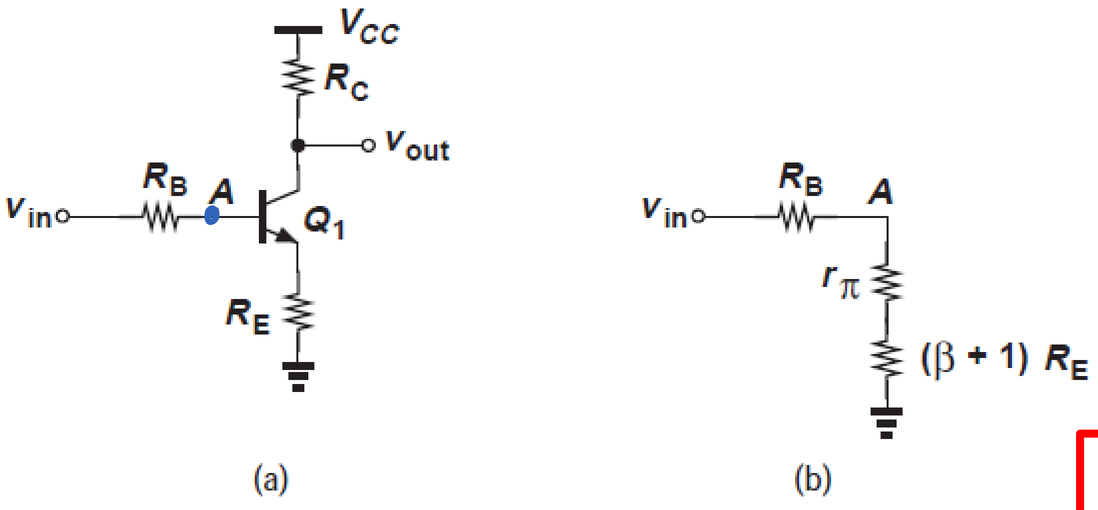
❑With Emitter Degenerate Resistance R_E (without Early Effect) and Base Resistance (R_B)

❑ **Challenges of Base Resistance (R_B)**

- ✓ Base resistance degrades the performance

Gain without R_B

$$\boxed{A_v = -\frac{g_m R_C}{1 + g_m R_E}.}$$



(a) CE stage with base resistance, (b) equivalent circuit.

Gain with R_B

$$\boxed{A_v \approx \frac{-R_C}{\frac{1}{g_m} + R_E + \frac{R_B}{\beta + 1}}.}$$

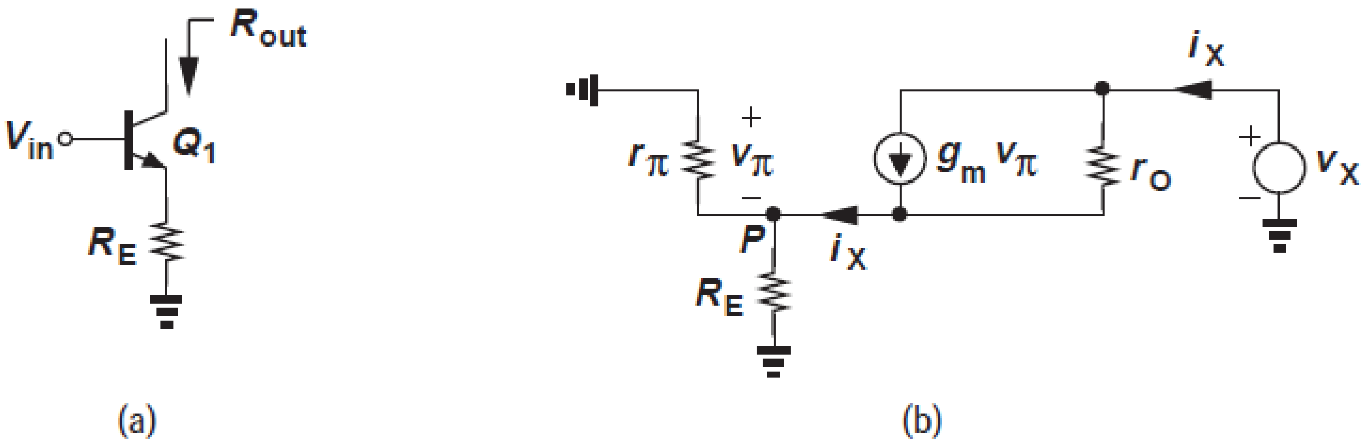
Bipolar Amplifiers

❑BJT Amplifier Topologies

❑Common Emitter Topology

❑With Emitter Degenerate Resistance R_E with Early Effect

- ❑ Early Effect primarily affects the **output impedance** of the circuit
- ❑ Let us calculate the output impedance with the early effect



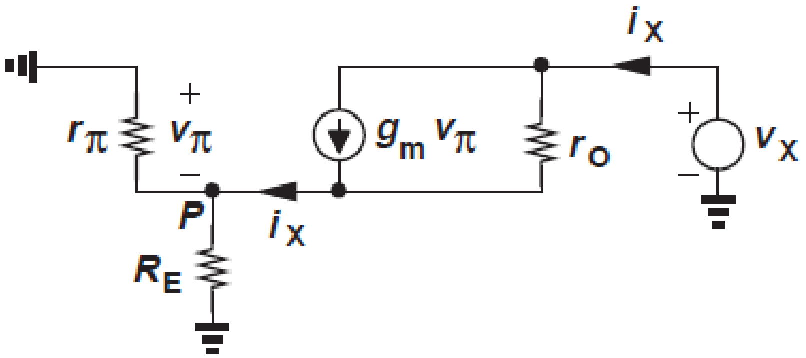
(a) Output impedance of degenerated stage, (b) equivalent circuit.

Bipolar Amplifiers

❑BJT Amplifier Topologies

❑Common Emitter Topology

❑With Emitter Degenerate Resistance R_E with Early Effect



$$v_\pi = -i_X(R_E||r_\pi),$$

$$v_X = (i_X - g_m v_\pi)r_O - v_\pi$$
$$= [i_X + g_m i_X(R_E||r_\pi)]r_O + i_X(R_E||r_\pi).$$

The output resistance is boosted by $(1 + g_m R_E)$ with the inclusion of Early Effect

$$R_{out} = [1 + g_m(R_E||r_\pi)]r_O + R_E||r_\pi$$
$$= r_O + (g_m r_O + 1)(R_E||r_\pi).$$

the intrinsic gain of the transistor, $g_m r_O \gg 1$

$$R_{out} \approx r_O + g_m r_O(R_E||r_\pi)$$
$$\approx r_O[1 + g_m(R_E||r_\pi)].$$

For $R_E \gg r_\pi$, we have $R_E||r_\pi \to r_\pi$ and

$$R_{out} \approx r_O(1 + g_m r_\pi)$$
$$\approx \beta r_O,$$

For $R_E \ll r_\pi$, we have $R_E||r_\pi \to R_E$ and

$$R_{out} \approx (1 + g_m R_E)r_O.$$

Bipolar Amplifiers

❑BJT Amplifier Topologies

❑Common Emitter Topology

❑Common Emitter with Biasing

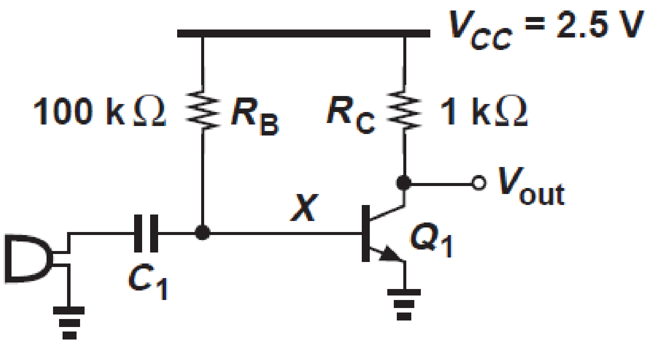
- ❑ Remember that we have seen three biasing schemes
  - ❑ Simple (Base Resistance) Biasing
  - ❑ Resistor-Divider Biasing
  - ❑ Self Biasing

Bipolar Amplifiers

❑BJT Amplifier Topologies

❑Common Emitter with Biasing

❑Case – 1 – Simple Biasing



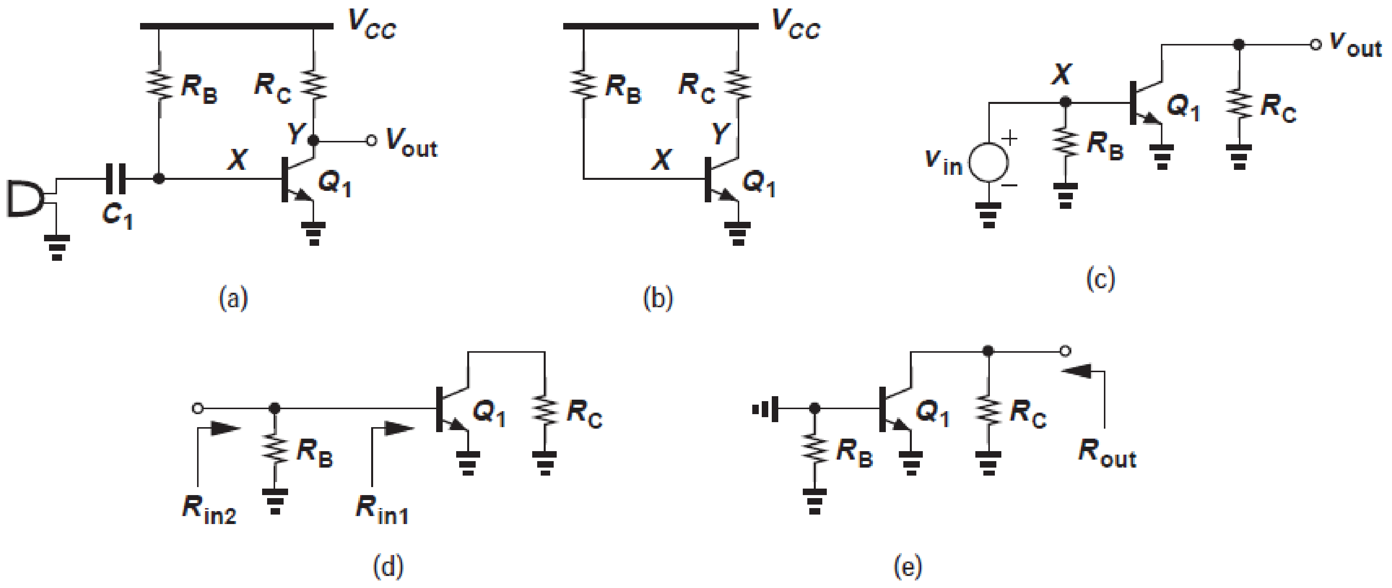


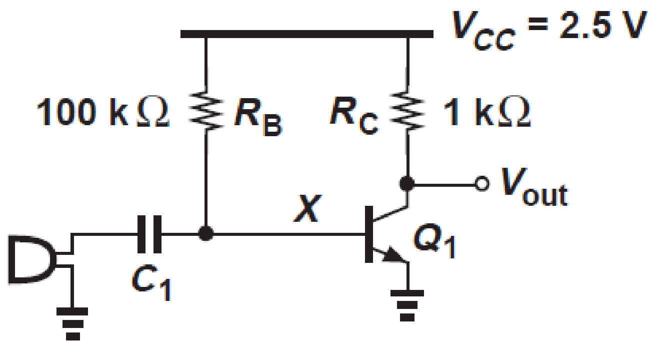
Figure 5.52 (a) Capacitive coupling at the input of a CE stage, (b) simplified stage for bias calculation, (c) simplified stage for small-signal calculation, (d) simplified circuit for input impedance calculation, (e) simplified circuit for output impedance calculation.

Bipolar Amplifiers

❑BJT Amplifier Topologies

❑Common Emitter with Biasing

❑Case – 1 – Simple Biasing



Voltage Gain

$$\frac{v_{out}}{v_{in}} = -g_m(R_C||r_O).$$

Input Impedance

$$R_{in2} = r_\pi||R_B.$$

Output Impedance

$$R_{out} = R_C||r_O.$$

DC Analysis

$$I_C = \beta\frac{V_{CC} - V_{BE}}{R_B},$$

$$V_Y = V_{CC} - \beta R_C\frac{V_{CC} - V_{BE}}{R_B}.$$

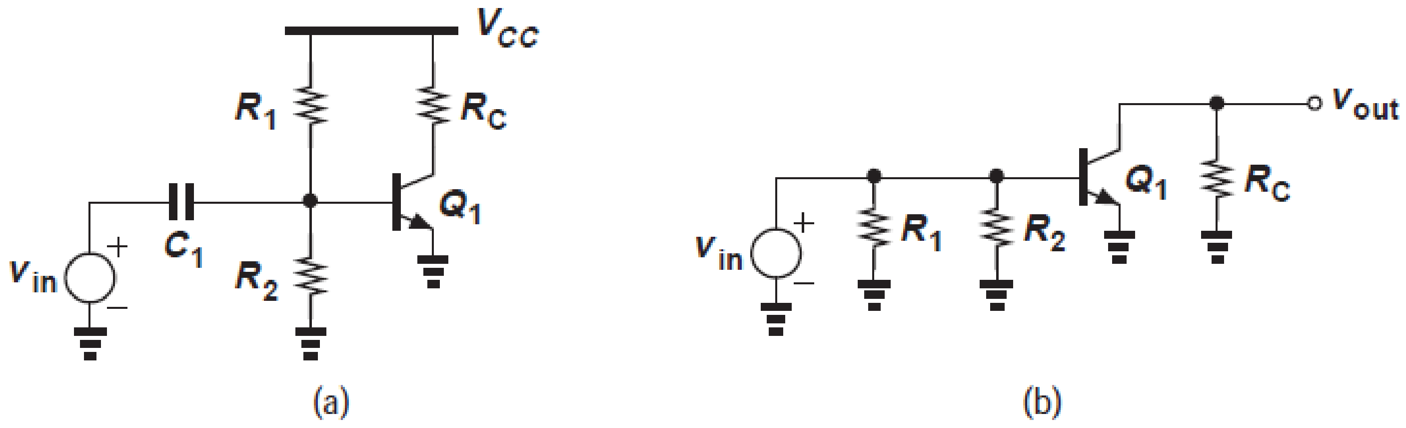
To avoid saturation, $V_Y \geq V_{BE}$.

Bipolar Amplifiers

❑BJT Amplifier Topologies

❑Common Emitter with Biasing

❑Case – 2a – Voltage Divider Biasing (with Early Effect)



(a) Biased stage with capacitive coupling, (b) simplified circuit.

Voltage Gain

$$-g_m(R_C||r_O)$$

Input Impedance

$$R_{in} = r_\pi||R_1||R_2.$$

Output Impedance

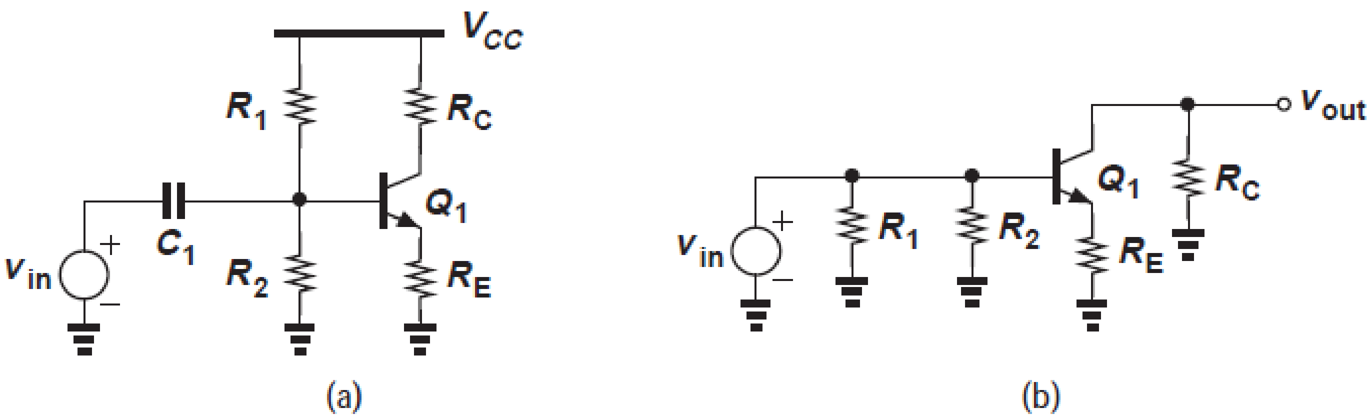
$$R_{out} = R_C$$

Bipolar Amplifiers

❑BJT Amplifier Topologies

❑Common Emitter with Biasing

❑Case – 2b – Voltage Divider Biasing with Emitter Degenerate Resistance



(a) Degenerated stage with capacitive coupling, (b) simplified circuit.

Voltage Gain

$$A_v = \frac{-R_C}{\frac{1}{g_m} + R_E},$$

Input Impedance

$$R_{in} = [r_\pi + (\beta + 1)R_E]||R_1||R_2,$$

Output Impedance

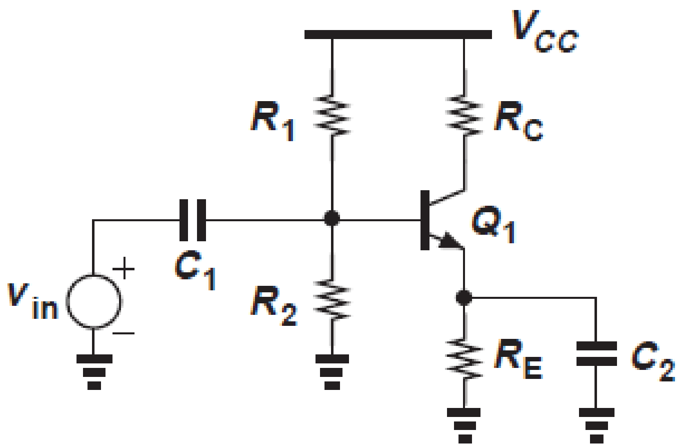
$$R_{out} = R_C$$

Bipolar Amplifiers

❑BJT Amplifier Topologies

❑Common Emitter with Biasing

❑Use of Capacitor to Eliminate Degenerate



Voltage Gain

$$A_v = -g_m R_C$$

Input Impedance

$$R_{in} = r_\pi || R_1 || R_2$$

Output Impedance

$$R_{out} = R_C .$$

Advantages

- The use of R_E provides biasing linearity and stability but decreases the gain
- Using capacitor eliminates R_E effect on the small-signal gain

Bipolar Amplifiers

❑BJT Amplifier Topologies

❑Common Emitter with Biasing

❑A general (practical) CE stage (without Early Effect)

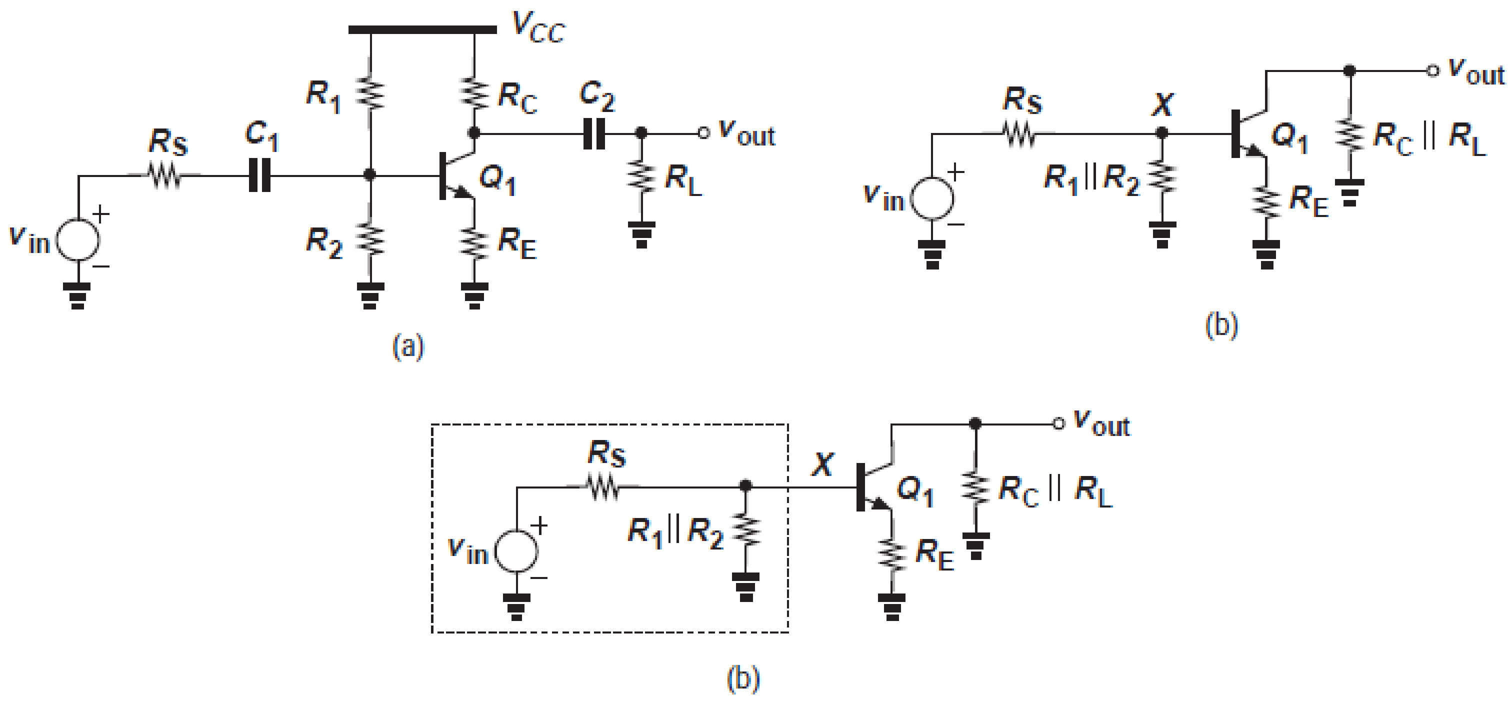


Figure 5.58 (a) General CE stage, (b) simplified circuit, (c) Thevenin model of input network.

Voltage Gain

$$A_v = -\frac{R_C||R_L}{\dfrac{1}{g_m} + R_E + \dfrac{R_{Thev}}{\beta + 1}} \cdot \frac{R_1||R_2}{R_1||R_2 + R_S},$$

Input Impedance (between R_S and node X)

$$R_1||R_2||[r_\pi + (\beta + 1)R_E]$$

Output Impedance

$$R_C \parallel R_L$$

Bipolar Amplifiers

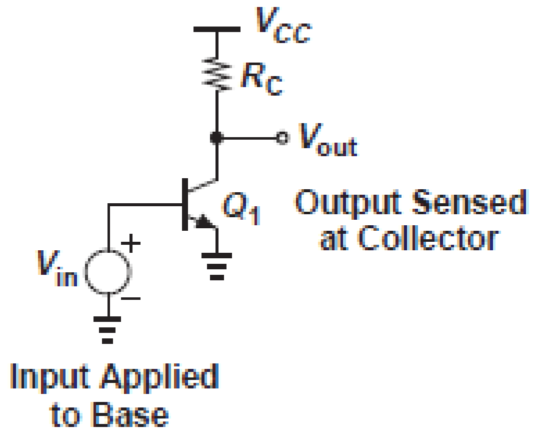
❑BJT Amplifier Topologies

Example 5.20 A CE stage must achieve an input impedance of R_{in} and an output impedance of R_{out}. What is the voltage gain of the circuit?

Bipolar Amplifiers

❑BJT Amplifier Topologies

Example 5.21 The circuit of Fig. 5.29 is biased with a collector current of 1 mA and $R_C = 1\,\text{k}\Omega$. If $\beta = 100$ and $V_A = 10$ V, determine the small-signal voltage gain and the I/O impedances.



Bipolar Amplifiers

❑BJT Amplifier Topologies

Example 5.22 Determine the voltage gain of the stage shown in Fig. 5.37(a).

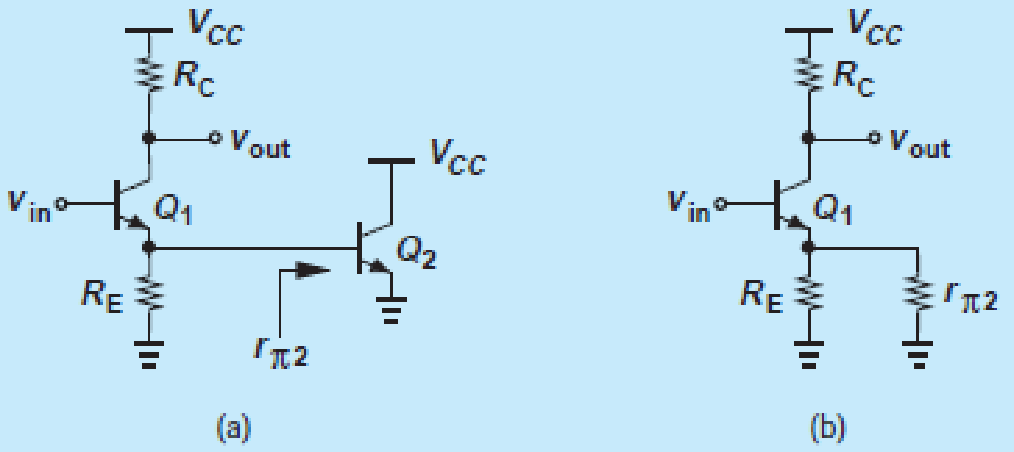


Figure 5.37 (a) CE stage example, (b) simplified circuit.

Bipolar Amplifiers

❑BJT Amplifier Topologies

Example 5.23 Calculate the voltage gain of the circuit in Fig. 5.38(a).

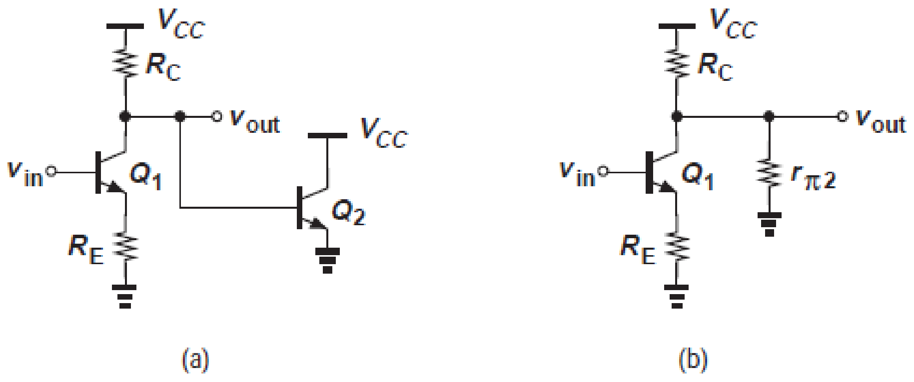


Figure 5.38 (a) CE stage example, (b) simplified circuit.

Bipolar Amplifiers

❑BJT Amplifier Topologies

Example 5.24

A CE stage is biased at a collector current of 1 mA. If the circuit provides a voltage gain of 20 with no emitter degeneration and 10 with degeneration, determine R_C, R_E, and the I/O impedances. Assume $\beta = 100$.

Bipolar Amplifiers

❑BJT Amplifier Topologies

Example 5.27

Determine the voltage gain and I/O impedances of the circuit shown in Fig. 5.45(a). Assume a very large value for C_1 and neglect the Early effect.

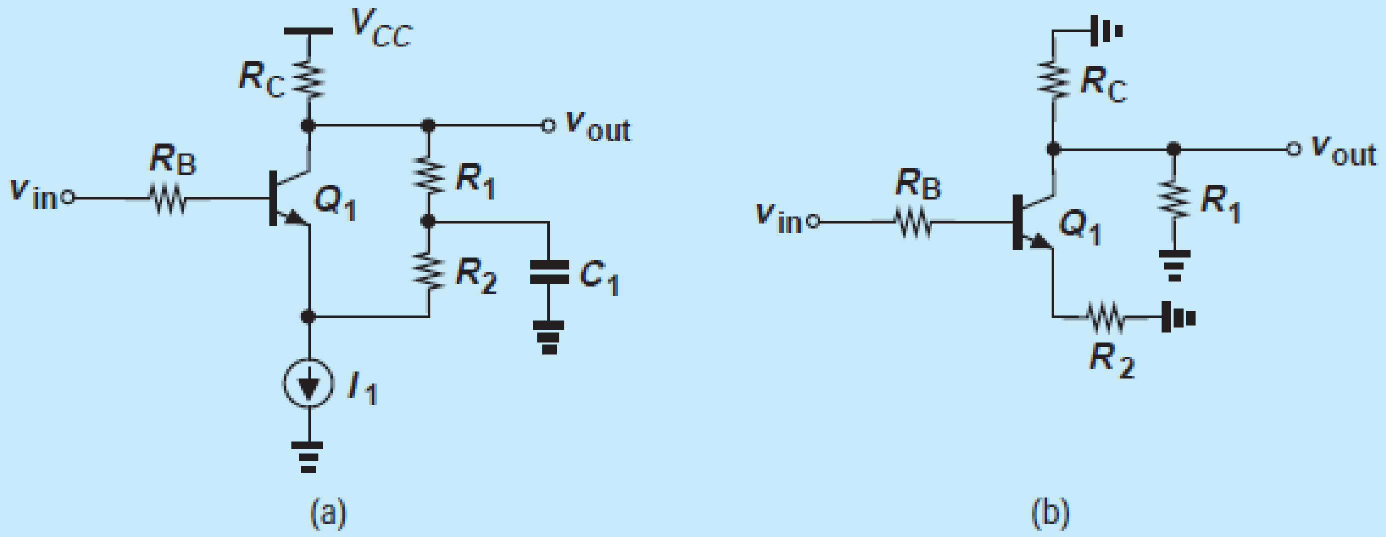


Figure 5.45 (a) CE stage example, (b) simplified circuit.

Bipolar Amplifiers

❑BJT Amplifier Topologies

Example 5.28

We wish to design a current source having a value of 1 mA and an output resistance of 20 kΩ. The available bipolar transistor exhibits $\beta = 100$ and $V_A = 10$ V. Determine the minimum required value of emitter degeneration resistance.

Bipolar Amplifiers

❑BJT Amplifier Topologies

Example 5.29

Calculate the output resistance of the circuit shown in Fig. 5.48(a) if C_1 is very large.

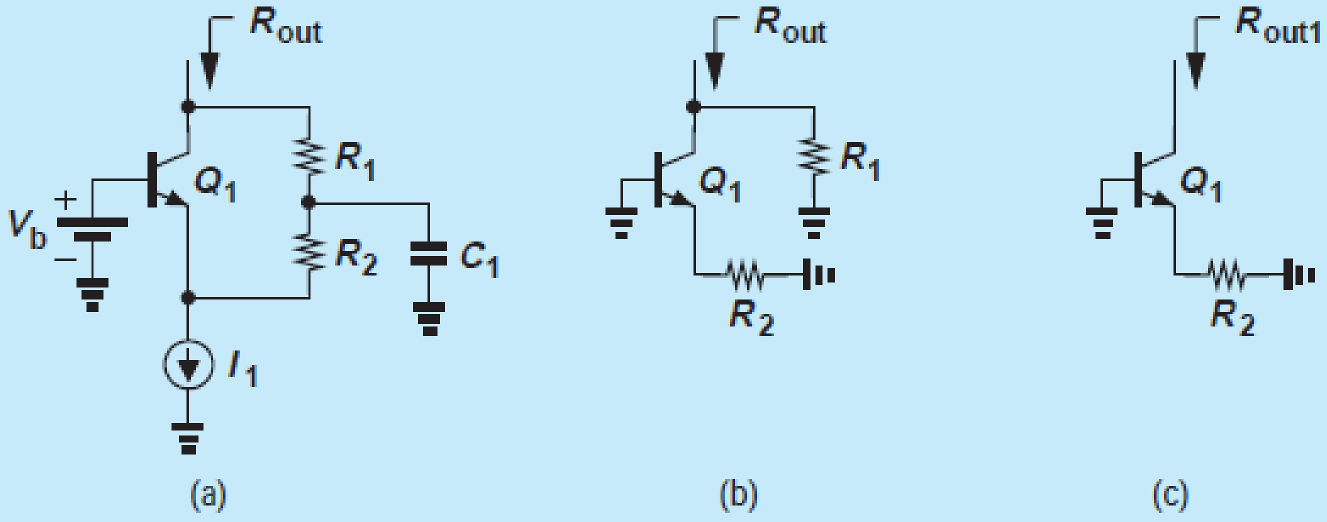


Figure 5.48 (a) CE stage example, (b) simplified circuit, (c) resistance seen at the collector.

Bipolar Amplifiers

❑BJT Amplifier Topologies

Example 5.30

Determine the output resistance of the stage shown in Fig. 5.49(a).

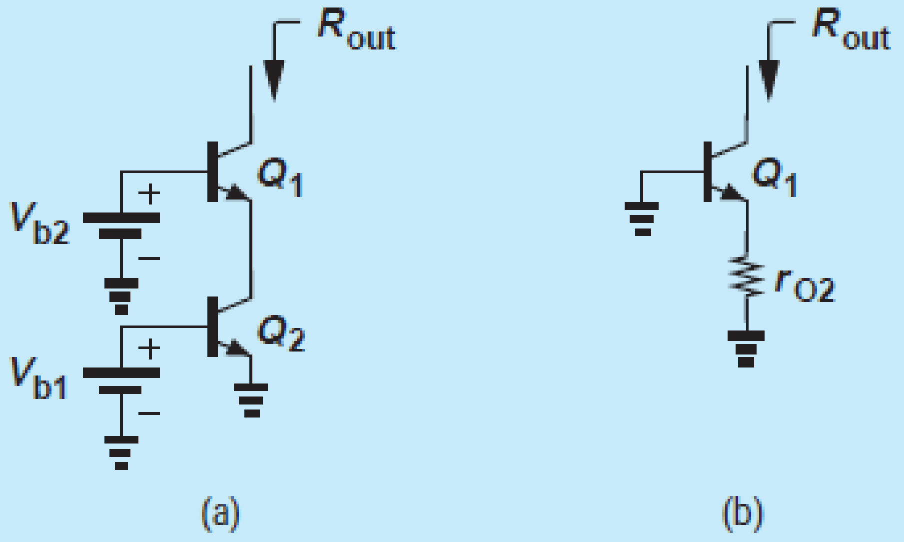


Figure 5.49 (a) CE stage example, (b) simplified circuit.

Bipolar Amplifiers

❑BJT Amplifier Topologies

Example 5.34

Design the stage of Fig. 5.57 to satisfy the following conditions: $I_C = 1$ mA, voltage drop across $R_E = 400$ mV, voltage gain $= 20$ in the audio frequency range (20 Hz to 20 kHz), input impedance > 2 kΩ. Assume $\beta = 100$, $I_S = 5 \times 10^{-16}$, and $V_{CC} = 2.5$ V.