Exercises 02

Memory Basics

Chapter 7

1) The following memories are specified by the number of words times the number of bits per word. How many address lines and input-output data lines are needed in each case?
a) 48K x 8; b) 512K x 32; c) 64M x 64; d) 2G x 1

2) a) The word number $(835)_{10}$ shown in the Figure 7-2 contains the binary equivalent of $(15103)_{10}$. List the 10-bit address and the 16-bit memory contents of the word.

Memory Address		
Binary	Decimal	Memory Contents
0000000000	0	10110101 01011100
0000000001	1	10101011 10001001
0000000010	2	00001101 01000110
	.	.
	.	.
	.	.
	.	.
	.	.
1111111101	1021	10011101 00010101
1111111110	1022	00001101 00011110
1111111111	1023	11011110 00100100

FIGURE 7-2
Contents of a 1024 × 16 Memory

b) Repeat part (a) for word number $(513)_{10}$ containing the binary equivalent of $(44252)_{10}$

3) How many address and data lines are needed for memory chips with the following organization?
a) 256 x 4
b) 512 x 8
c) 1K x 16
d) 32K x 8

4) A DRAM has a refresh interval of 64 ms (single refresh) and has 8192 rows. What is the interval between refreshes for distributed refresh? What is the total time required out of the 64ms for a refresh of the entire DRAM given the time of a single refresh equal to 60 ns? What is the minimum number of address pins on the DRAM?

5) How many 128K x 16 chips are needed to provide a memory capacity of 2MB? How many address lines are required to access 2MB? Each word is composed of 2 bytes.

6) A 1 Mbit DRAM memory has 1024 rows and 1024 columns. The refresh time is 5 ms, the access time is 60 ns. Compute the percentage of memory cycles for the refresh

7) Consider a 128 KB static memory with n banks, each consisting of 8 4Kx1 bit memory chips.
- What is the value of n?
- Which bits of the address select the bank to be activated?
- How many address lines must be decoded to select the bit of each chip?

8) Consider a 64 Kbit x 1 DRAM memory, organized as a square matrix, the reading of one memory cell require t_a=50 ns. Compute the minimum refresh time for each bit such that the percentage of the access for refresh over the total is less than 0.5 %.

9) Consider the memory below and solve the following points:

a) In which memory bank, the address byte A01B8 is stored?

b) How many bits does the architecture that uses this memory have?

c) How big is this memory, in Kilo Bytes?