Exercises 01

Computer Design Basics

Chapter 8

1) Given a 4-bits barrel shifter, find the output Y for each of the following inputs applied to (S_1, S_0, D_3, D_2, D_1, D_0):

(a) 110101 **(b) 101011**
(c) 011010 **(d) 001101**

2) Specify the 16-bits control word to be applied to the datapath to implement the following microoperations:

(a) R3 ←Data in **(b) R4 ← 0**
(c) R1 ← sr R4 **(d) R3 ← R3 + 1**
(e) R2 ←sl R2 **(f) R1 ← R2 ⊕ R4**
(g) R7 ← R1 + R3 **(h) R4 ← R5 – Constant in**

3) Given the following 16-bits control words for the datapath, determine a) the microoperation that is executed and b) the contents of the registers for each control word. Assume that the registers contain the value of their index (e.g., the register R5 contains 05 in hexadecimal). Assume that Constant in has value has 6 and Data In has value 1B.

(a) 101 100 101 0 1000 0 1 **(b) 110 010 100 0 0101 0 1**
(c) 101 110 000 0 1100 0 1 **(d) 101 000 000 0 0000 0 1**
(e) 100 100 000 1 1101 0 1 **(f) 011 000 000 0 0000 1 1**

4) A computer has a 32-bits instruction format consisting of the following: opcode (6 bits), 2 registers addresses (5 bits per each), and one immediate operand/registers addresses (16 bits).

a) What is the maximum number of operation possible?

b) How many registers can be addressed?

c) What is the maximum value of an immediate operand (unsigned) that can be provided?

d) What is the range of an immediate operand (unsigned) that can be provided if we assume that the operands are signed 2s complement binary numbers and the 15^{th} bit is the one associated with the sign?

5) A computer has a memory unit with 32 bits instruction and a register file with 64 registers. The instruction set consists of 130 different operations. The instruction format is the following: opcode, a register file address, and the immediate operand part. Each instruction is stored in one word of memory.

a) How many bits are necessary for the opcode part of the instruction?

b) How many bits are left for the immediate operand?

c) If the immediate operand is used as an unsigned address to memory, what is the maximum number of words that can be addressed in memory?

d) What are the largest and the smallest algebraic values of signed 2s complement binary numbers that can be accommodated as an immediate operand?

6) A single-cycle computer executes the five instructions in the following tables (a) and (b).

a) Complete the table

Instruction Register Tranfer	DA	AA	BA	MB	FS	MD	RW	MW	PL	JB
R[0] ← R[7] ⊕ R[3]										
R[1] ← M[R[4]]										
R[2] ← R[5] + 2										
R[3] ← sl R[6]										

if R[4] = 0 then
PC ← PC + se AD
else
PC ← PC + 1										

b) Complete the table

Instruction Register Transfer	Operation Code	DR	SA	SB or Operand
R[0] ←R[7] + R[6]				
R[1] ← R[5] - 1				
R[2] ← sl R[4]				
R[3] ← $\overline{R[3]}$				
R[4] ← R[2] ∨ R[1]				

7) Simulate the following sequence of instructions, assuming that each register initially contains contents equal to its index (e.g., R1 contains 1). Report the binary value of each instruction and the content of any register changed by the instruction.

Instruction	Code	Registers/Memory changed
ADD R0, R1, R2		
SUB R3, R4, R5		
SUB R6, R7, R0		
ADD R0, R0, R3		
SUB R0, R0, R6		
ST R7, R0		
LD R7, R6		
ADI R0, R6, 2		
ADI R3, R6, 3		

8) How many Mbyte is possible to address with 16 bit?, 20 bit?, 24 bit?, 32 bit?, 64 bit?