Esercizi 02

Memory Basics

Chapter 7 - Solutions

1) The following memories are specified by the number of words times the number of bits per word. How many address lines and input-output data lines are needed in each case?
a) 48K x 8; b) 512K x 32; c) 64M x 64; d) 2G x 1

Solution:
a) $N = \log_2(48x1024) = 15.58 = 16$; $D = 8$
b) $N = \log_2(512x1024) = 19$; $D = 32$
c) $N = \log_2(64x1024x1024) = 26$; $D = 64$
d) $N = \log_2(2x1024x1024x1024) = 31$; $D = 1$

2) a) The word number $(835)_{10}$ shown in the Figure 7-2 contains the binary equivalent of $(15103)_{10}$. List the 10-bit address and the 16-bit memory contents of the word.

Memory Address		
Binary	Decimal	Memory Contents
0000000000	0	10110101 01011100
0000000001	1	10101011 10001001
0000000010	2	00001101 01000110
	.	.
	.	.
	.	.
	.	.
	.	.
1111111101	1021	10011101 00010101
1111111110	1022	00001101 00011110
1111111111	1023	11011110 00100100

FIGURE 7-2
Contents of a 1024 × 16 Memory

b) Repeat part (a) for word number $(513)_{10}$ containing the binary equivalent of $(44252)_{10}$

Solution:
a) i = 11 0100 0011; d = 0011 1010 1111 1111
b) i = 10 0000 0001; d = 1010 1100 1101 1100

3) How many address and data lines are needed for memory chips with the following organization?
a) 256 x 4
b) 512 x 8
c) 1K x 16

d) 32K x 8

Solution:
a) 4 lines for data and 256 memory locations → 2^8 → I = 8
b) 2^9 → I = 9
c) 2^{10}→ I = 10
d) 2^{15}→ I = 15

4) A DRAM has a refresh interval of 64 ms (single refresh) and has 8192 rows. What is the interval between refreshes for distributed refresh? What is the total time required out of the 64ms for a refresh of the entire DRAM? What is the minimum number of address pins on the DRAM?

Solution:

- Number of rows to update 8192 → $I_{refresh}$ = 64 ms / 8192 = 7.1825 μs

- Total time for refresh: 60 ns * 8192 = 0.49 ms

- $\log_2 8192$ = 13 pins

5) How many 128K x 16 chips are needed to provide a memory capacity of 2MB? How many address lines are required to access 2MB? Each word is composed of 2 bytes.

Solution:
- 2MB / (128K * 16) = 2MB / 256 KB = 8
- Each word is composed of 2 bytes → to access to each word we need 2MB/2B = 2^{20} → 20 bits for the address

6) A 1 Mbit DRAM memory has 1024 rows and 1024 columns. The refresh time is 5 ms, the access time is 60 ns. Compute the percentage of memory cycles for the refresh

Solution:
In a DRAM, the refresh is performed through a reading operation related to a row. Given t_A the access time, T_R the refresh period and N_{rows} the number of rows of the matrix in the chip, the refresh time for each row is equal to:

$$t_R = \frac{T_R}{N_{rows}}$$

The ratio of the access time to the time required for a single refresh of just one row represent the number of cycles needed for the refresh. Therefore, the percentage of memory cycles for the refresh is:

$$Refresh\% = \frac{t_A}{t_R} \cdot 100 = \frac{60 \cdot 10^{-9}}{5 \cdot 10^{-3}} \cdot 1024 \cdot 100 = 1.2288\%$$

7) Consider a 128 KB static memory with n banks, each consisting of 8 4Kx1 bit memory chips.

- What is the value of n?
- Which bits of the address select the bank to be activated?
- How many address lines must be decoded to select the bit of each chip?

Solution:
Each bank provides a 4KB memory, so:
n = 128 KB / 4 KB = 2^{17} / 2^{12} = 2^5 = 32
To address 128Kbyte, 17 address line are needed**.** Among them, 5 are used to select the bank (via the activation of the corresponding input select in the chip) and 12 to address one of the 4Kbit in each chip.

8) Consider a 64 Kbit x 1 DRAM memory, organized as a square matrix, the reading of one memory cell require t_a=50 ns. Compute the minimum refresh time for each bit such that the percentage of the access for refresh over the total is less than 0.5 %.

Solution:
Given a square matrix, we have:

$$N_{rows} = N_{columns} = \sqrt{64K} = 256$$

$$Refresh\% = \frac{t_A}{t_R} = \frac{t_A}{\frac{T_R}{N_{rows}}} \leq 0.005$$

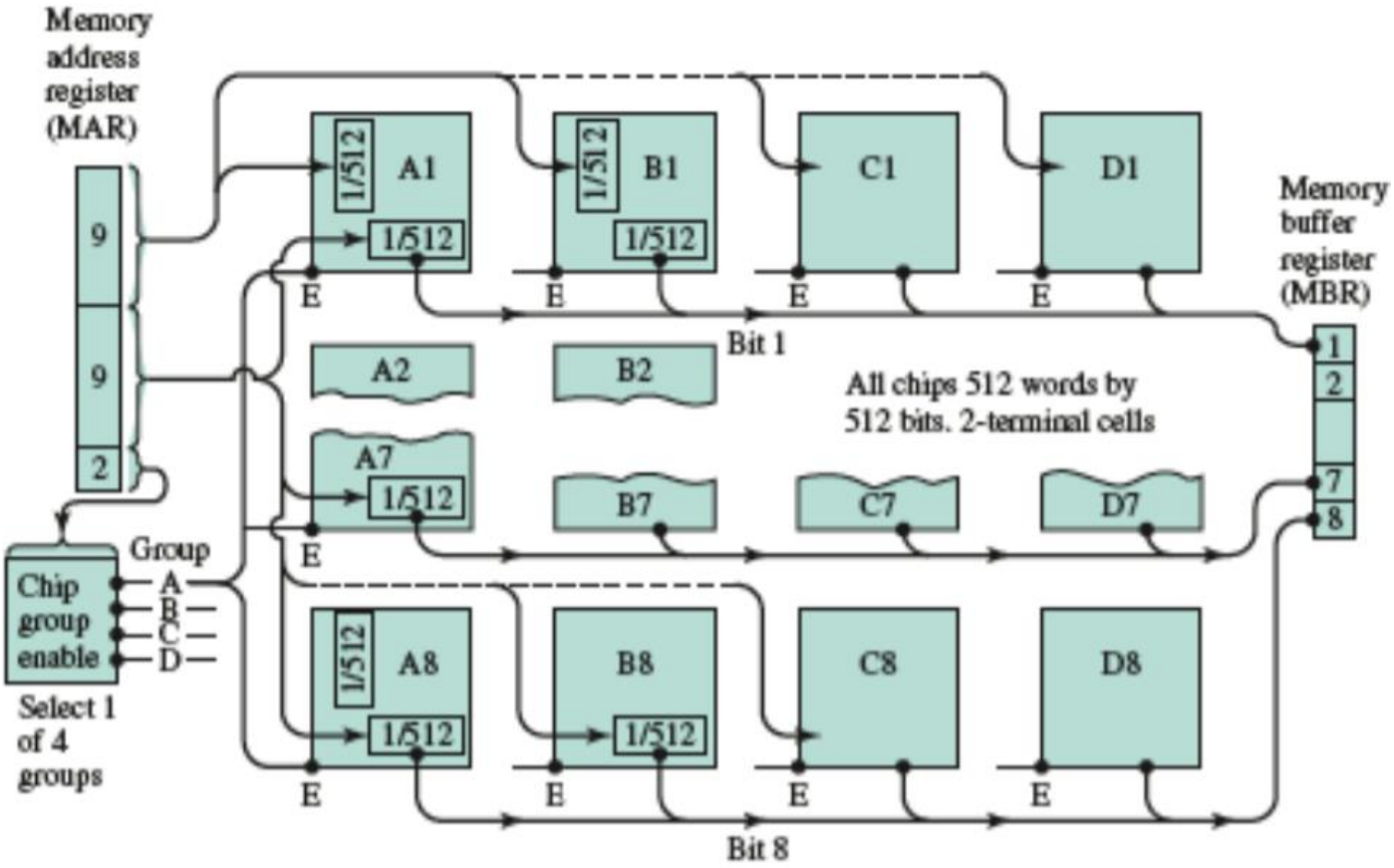
$$T_R \geq \frac{t_A \cdot N_{rows}}{0.005} = \frac{50 \cdot 10^{-9} \cdot 256}{0.005} = 2.56\, ms$$

9) Consider the memory below and solve the following points:

a) In which memory bank, the address byte A01B8 is stored?

b) How many bits does the architecture that uses this memory have?

c) How big is this memory, in Kilo Bytes?



Solution:

a)

By looking the figure, it is noted that the selection of the bank from which it is possible to access to the target location is entrusted to the 2 most significant bits of the address.

By converting the address in binary, we have:

1010 0000 0001 1011 1000

The target bank corresponds to 10, namely the bank with index$10_2 = 2_{10}$ → C

b)

The MBR register has 8 bits, i.e. 1 byte: this means that words are read from the memory 1 byte long and therefore we can say that the architecture is 8 bit.

The MAR register is 20 bits long, so we expect to be able to address 2^20 locations and since each word is 8 bits long, we expect the total memory to be 1 MB.

In fact we see from the diagram that there are 4 banks, each of 512 bit x 512 word. Each bank consists of 8 512x512 bit chips: each single chip contains 2^18 bits and during the operations of read/write 1 bit of each of the 8 chips is accessed in parallel, working on an entire byte.

Therefore, each bank contains 2^18 bytes.

c)

The memory consists of 4 banks and therefore we can store a total of 4 * 2^18 bytes = 2^2 * 2^18 bytes = 2^20 bytes, i.e. 1MB of data.