

## Lab#2: Basma Gamal Fawzy

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### Problem 1:

- a) Implement a Verilog code for 4-bit PISO.
  - b) Implement a Verilog code for 4-bit SIPO.
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### PISO

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```
module PISO #(parameter n = 4) (input clk , rst , sh_en, load , [n-1:0] pi ,
output reg so);
reg [n-1:0] q ;
assign so = q[0] ;
always @(posedge clk ) begin
    if (rst==1) q = 0 ;
    else if (load==1)    q = pi ;
    else if (sh_en==1)  q = {1'b0 , q[n-1:1] } ;
end
endmodule
```

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### PISO Testbench

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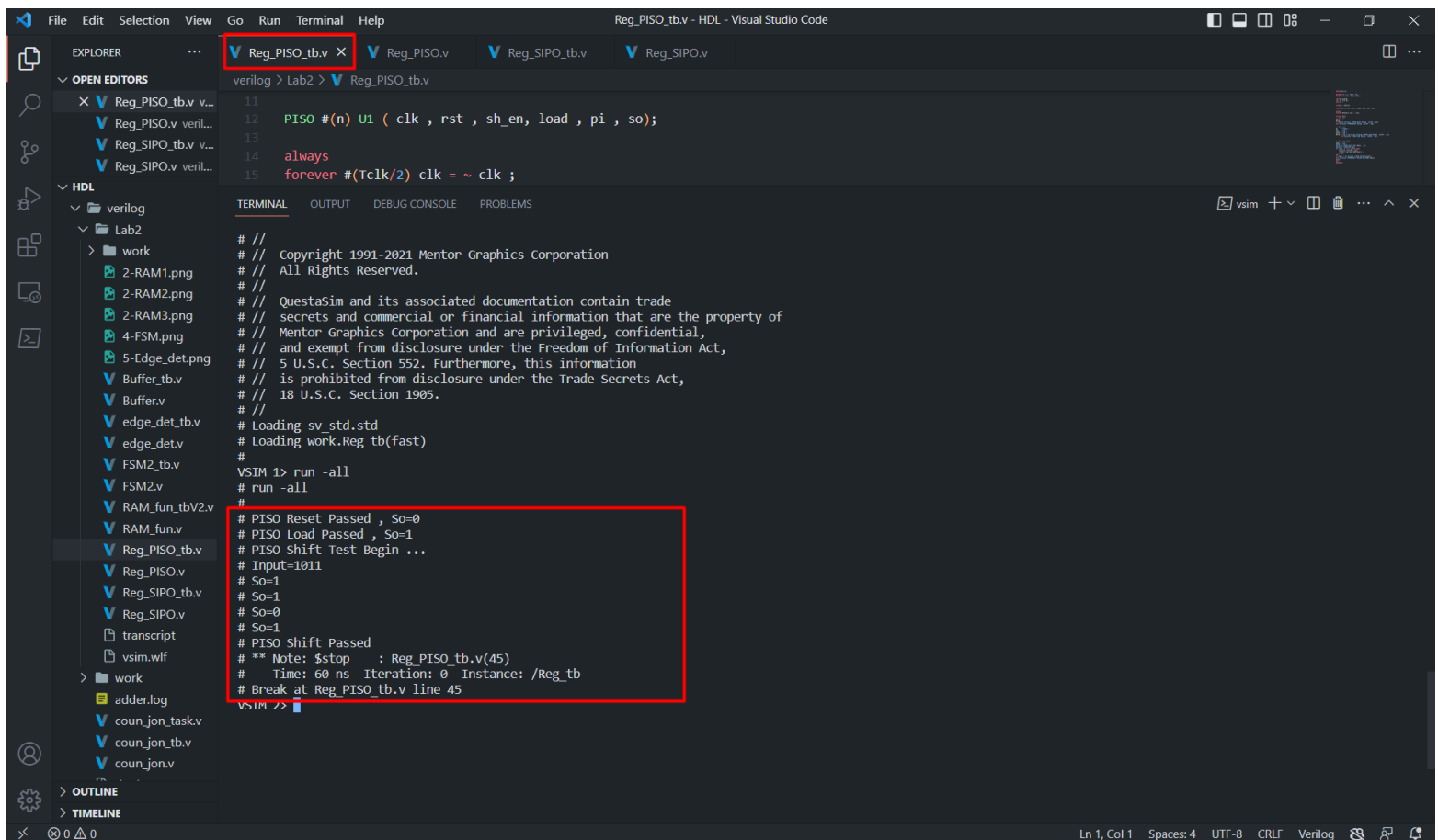
```
module Reg_tb;
parameter n = 4 , Tclk = 10;
reg clk = 0, rst , sh_en, load ;
reg si, so_old;
reg [n-1:0] pi; wire so ;
integer i ,fail=0;
PISO #(n) U1 ( clk , rst , sh_en, load , pi , so);

always
forever #(Tclk/2) clk = ~ clk ;
initial begin
// test rest
rst = 1 ;
#Tclk
if (so==0) $display ("PISO Reset Passed , So=%b" , so);
else $display ("PISO Reset Failed , So=%b" , so);

// test Load
pi = 4'b1011 ; rst= 1'b0 ; load= 1'b1 ; sh_en = 1'b0 ;
#Tclk if (so == pi [n-1]) $display ("PISO Load Passed , So=%b" , so);
else $display ("PISO Load Failed , So=%b" , so);
```

```
// test shift PISO
load = 1'b0 ;
sh_en = 1'b1 ;
$display ("PISO Shift Test Begin ...");
$display ("Input=%b",pi);
for (i=0 ; i < n ; i=i+1) begin
    $display ("So=%b ", so);
    if (so != pi [i]) fail=fail+1 ;
    #Tclk ;
end
if (fail == 0) $display ("PISO Shift Passed");
else $display ("PISO Shift Failed Fail=%0d",fail);
$stop ;
end
endmodule
```

## PISO Output



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## SIPO

---

```
module SIPO #(parameter n = 4) (input clk , rst , sh_en, load , si , output reg
[n-1:0] po);
always @(posedge clk ) begin
    if (rst==1) po = 0 ;
    else if (load==1)    po = { si , po[n-1:1] };
    else if (sh_en==1)   po = { 1'b0, po[n-1:1]};
end
endmodule
```

---

## SIPO Testbench

---

```
module Reg_tb;
parameter n = 4 , Tclk = 10;
reg clk = 0, rst , sh_en, load, si;
reg [n-1:0] inputs , po_sh;
wire [n-1:0] po ;
integer i ,fail=0;
SIPO #(n) U2 ( clk , rst , sh_en, load , si , po);
always
forever #(Tclk/2) clk = ~ clk ;

initial begin
// test rest
rst = 1 ;
#Tclk
if (po==0) $display ("SIPO Reset Passed , Po=%b",po);
else $display ("SIPO Reset Failed , Po=%b",po);

// test load
inputs = 4'b1011 ; rst = 1'b0 ; load = 1'b1 ; sh_en = 1'b0 ;
for (i=0 ; i < n ;i=i+1) begin
si= inputs[i] ; #Tclk ;
end
if (po == inputs) $display ("SIPO Load Passed , Po=%b",po);
else $display ("SIPO Load Failed , Po=%b",po);

// test shift SIPO
load = 1'b0 ;
sh_en = 1'b1 ;
po_sh = po;
$display ("Shift Test begins ...");
```

```

for (i=0 ; i < n ;i=i+1) begin
$display ("Output=%b Shifted output=%b",po, po_sh);
po_sh = {1'b0 , po_sh[n-1:1]} ;
#Tclk if (po != po_sh) fail=fail+1 ;
end

if (fail == 0) $display ("SIPO Shift Passed");
else $display ("SIPO Shift Failed");
$stop ;
end
endmodule

```

## SIPO Output

The screenshot shows the Visual Studio Code interface with the Verilog file `Reg_SIPO.v` open in the editor. The file explorer on the left shows a project structure with various Verilog files and a `work` directory. The terminal window at the bottom displays the simulation output, which includes the compilation process and the results of the SIPO shift test.

```

# vlog Reg_SIPO.v Reg_SIPO_tb.v
#
# ** Note: (vlog-1901) OptionFile "E:/5-Software/HDL/verilog/vlog.opt" not found. Ignored.
# QuestaSim-64 vlog 2021.1 Compiler 2021.01 Jan 19 2021
# Start time: 17:08:49 on Aug 25,2023
# vlog Reg_SIPO.v Reg_SIPO_tb.v
# -- Compiling module SIPO
# -- Compiling module Reg_tb
#
# Top level modules:
#   Reg_tb
# End time: 17:08:49 on Aug 25,2023, Elapsed time: 0:00:00
# Errors: 0, Warnings: 0
VSIM 3> vsim Reg_tb -batch
# vsim Reg_tb -batch
#
# End time: 17:09:15 on Aug 25,2023, Elapsed time: 0:02:14
# Errors: 0, Warnings: 0
# vsim Reg_tb -batch
# Start time: 17:09:15 on Aug 25,2023
# ** Note: (vsim-3813) Design is being optimized due to module recompilation...
# Loading sv_std.std
# Loading work.Reg_tb(fast)
VSIM 4> run -all
# run -all
#
# SIPO Reset Passed , Po=0000
# SIPO Load Passed , Po=1011
# Shift Test begins ...
# Output=1011 Shifted output=1011
# Output=0101 Shifted output=0101
# Output=0010 Shifted output=0010
# Output=0001 Shifted output=0001
# SIPO Shift Passed
# ** Note: $stop : Reg_SIPO_tb.v(51)
# Time: 90 ns Iteration: 0 Instance: /Reg_tb
# Break at Reg_SIPO_tb.v line 51
VSIM 5>

```

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2- Write Verilog to model ram block and write a function in ram module to translate the input address ranges from 16'h8000- 16'h800f to 8'h00-8'h0f as the address of the ram is 8bits. The address port of the block is 16-bit. The data\_in and data\_out is 8-bit.

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```
module RAM_fun #(parameter n = 16 , d = 8)
    (input rst , clk , en , wr , [d-1:0] data_in , [n-1:0] adr,
     output reg [d-1:0] data_out);

    reg [d-1:0] mem [0: (2**n)-1];
    reg [7:0] new_adr ;
    integer i ;

    function [7:0] adr_conv;
    input [n-1:0] adr ;
    adr_conv= adr[7:0] ;
    endfunction

    always @(posedge(clk)) begin

        // // Initialize
        if (rst==1)
            for (i=0 ; i< 2**n ; i=i+1)
                mem[i]=0 ;

        // Synchronous Read
        else if (en==1)
            if (wr==1) mem[new_adr] = data_in ;
        end

        // asynchronous Read
        assign data_out = (en & ~ wr) ? mem[new_adr] : 0 ;

        // adres convert
        assign new_adr= adr_conv(adr);
    endmodule
```

---

## Simple Testbench

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```
module RAM_fun_tb ;

parameter n=16 , d=8 , Tclk=4;

reg rst , clk = 0 , en = 1 , wr ;
reg [d-1:0] data_in , v1 , v2;
reg [n-1:0] adr;
wire [d-1:0] data_out;

integer i , test=0;

// Map DUT
RAM_fun #(n,d) U (rst , clk , en , wr , data_in ,adr , data_out);

// clock generation
always
forever #(Tclk/2)   clk = ~ clk ;

initial begin
//test rest
rst = 1 ;
#Tclk $display ("Testing Loading ...");
rst = 0 ; en  = 1 ; wr  = 0 ;

for (i=0 ; i < 2**n ; i=i+1) begin
    adr = i ;
    if (data_out != 0 ) begin
        test = test + 1 ;
    end
end

if (test == 0) $display ("Inilization Test Passed") ;
else $display ("Inilization Test Failed ");

adr=16'h00_00 ;
#(Tclk/8) v1 = data_out ;

adr=16'h80_00 ;
#(Tclk/8) v2 = data_out ;

$display("check RAM with function initization....");
```



File Edit View Compile Simulate Add Memory Data Tools Layout Bookmarks Window Help

[illegible]

The screenshot shows the Visual Studio Code IDE with a Verilog project. The Explorer panel on the left displays a file tree with 'RAM\_fun\_tbV2.v' selected. The main editor shows the Verilog code for 'RAM\_fun\_tbV2.v', which includes module declarations, parameters, registers, and a testbench. The TERMINAL panel at the bottom shows the execution of 'vsim' and 'run' commands, with a red box highlighting the test results and a red arrow pointing to the text 'Keep writing insame place'.

```

verilog > Lab2 > RAM_fun_tbV2.v
1  module RAM_fun_tb ;
2
3  parameter n=16 , d=8 , Tclk=4;
4
5  reg rst, clk = 0 , en = 1 , wr ;
6  reg [d-1:0] data_in , v1 , v2;
7  reg [n-1:0] adr;
8  wire [d-1:0] data_out;
9
10 integer i , test=0;
11
12 // Map DUT
13
14 RAM_fun #(n,d) U (rst , clk , en , wr , data_in , adr , data_out);
15

```

```

TERMINAL OUTPUT DEBUG CONSOLE PROBLEMS
VSIM 4> vsim RAM_fun_tb -batch
# vsim RAM_fun_tb -batch
#
# End time: 16:47:32 on Aug 25,2023, Elapsed time: 0:04:03
# Errors: 0, Warnings: 0
# vsim RAM_fun_tb -batch
# Start time: 16:47:32 on Aug 25,2023
# ** Note: (vsim-3812) Design is being optimized...
# Loading sv_std.std
# Loading work.RAM_fun_tb(fast)
VSIM 5> run -all
# run -all
#
# Testing Loading ...
# Inilization Test Passed
# check RAM with function initialization...
# address in range data=00000000 & corresponding address out of range data=00000000
# Writing starts ...
# check RAM with function writing....
# address in range data=11111111 & corresponding address out of range data=11110000
# ** Note: $stop : RAM_fun_tbV2.v(69)
# Time: 12 ns Iteration: 1 Instance: /RAM_fun_tb
# Break at RAM_fun_tbV2.v line 69
VSIM 6>

```

Keep writing insame place



---

### 3- Write a Verilog code to model simple memory buffer:

- The input signals: clk, rst, w, r, 16-bit data\_in.
  - The output signals: 16-bit data\_out.
  - The internal writer pointer and read pointer of the memory buffer should wrap.
- 

#### Code

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```
module FIFO #(parameter depth = 4 , width = 16) (input clk , rst , w , r ,
[width-1:0] data_in , output reg [width-1:0] data_out);

parameter MSB = $clog2(depth)-1;
reg [width-1:0] stack [depth -1 : 0 ] ;
reg [MSB: 0] r_p = 0 , w_p = 0 ;
wire full, empty ;
reg overflow =0;
integer ocup = 0;

assign empty = (ocup == 0) ? 1'b1 : 1'b0 ;
assign full = (ocup == depth)? 1'b1 : 1'b0 ;

task push ( ) ;
begin
stack[w_p] = data_in ;
ocup = ocup + 1 ;
if (w_p==(depth-1)) begin
overflow = 1'b1;
w_p = 0 ;
end
else w_p = w_p + 1 ;
end
endtask

task pop ();
begin
data_out = stack[r_p] ;
ocup = ocup-1 ;
if (r_p==(depth-1)) begin
r_p = 0 ; overflow =1'b0;
end
else r_p = r_p + 1 ;
end
endtask
```

```

always @(posedge clk ) begin
if (rst == 1) begin
r_p  = 0 ;
w_p  = 0 ;
ocup = 0 ;
end
else if (w==1 & r==0) begin
// Not Full & NO Overflow or less than read at the Overflow
if ((!full && !overflow) || (overflow && (w_p < r_p)) )
push ; end

else if (w==0 & r==1) begin
if ((!overflow && (r_p < w_p)) || (!empty && overflow) )
pop ; end

else if (w==1 & r==1) begin
if (empty)
data_out = data_in ;
else
begin
pop; push;
end
end
end
endmodule

```

---

## Testbench

---

```

// FIFO
module FIFO_tb ;

parameter depth = 3 , width = 16, Tclk= 10;
reg clk = 0, rst , w , r ;
reg [width-1:0] data_in ;
wire [width-1:0] data_out;

FIFO #(depth,width) U (clk , rst , w , r , data_in , data_out) ;

always
forever #(Tclk/2) clk= ~clk ;

initial begin

rst = 1 ;

```

```

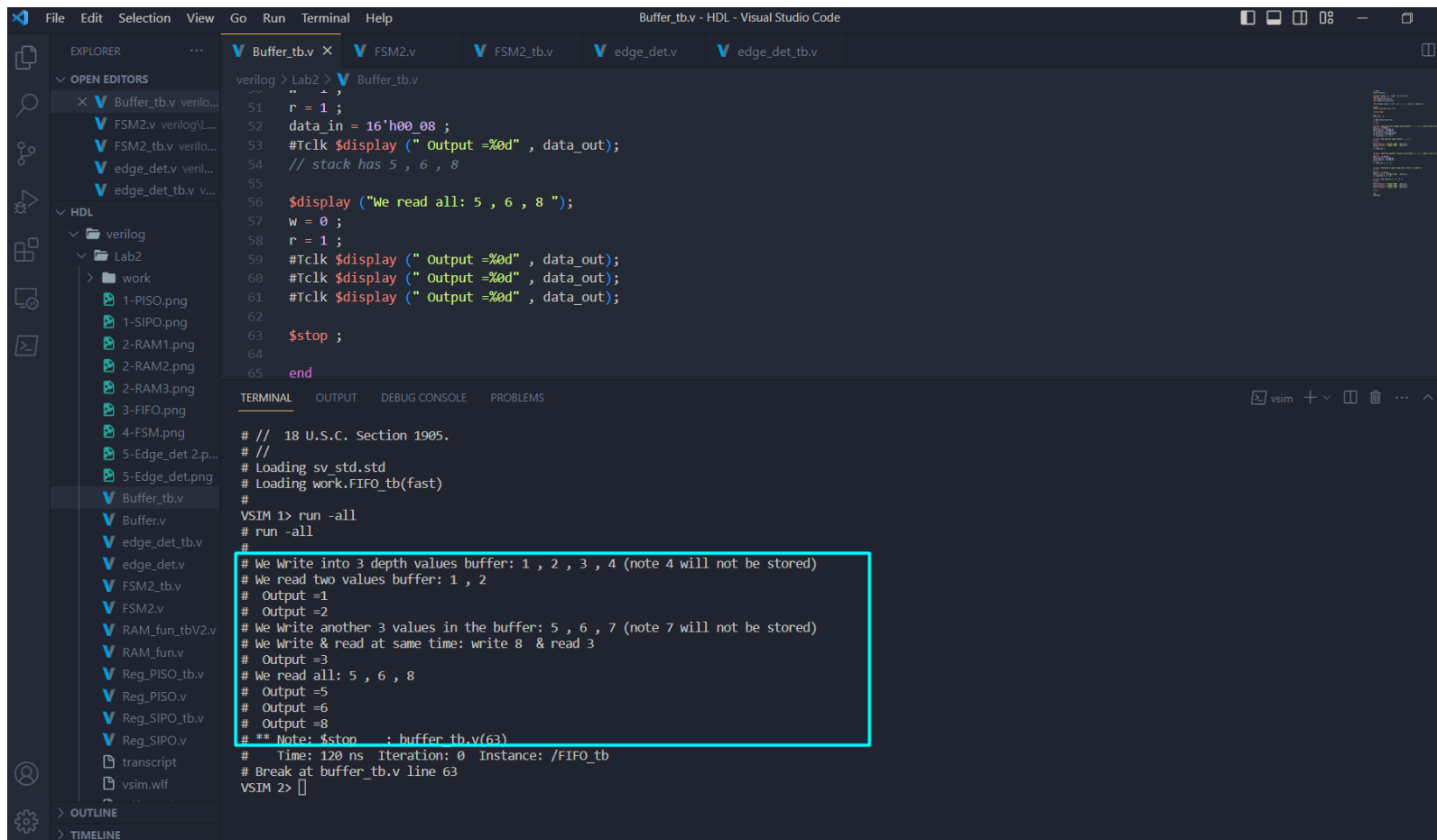
#Tclk rst = 0 ;

// Make stack above full
w = 1 ; r = 0 ;
$display ("We Write into 3 depth values buffer: 1 , 2 , 3 , 4 (note 4 will not be
stored)");
data_in = 16'h00_01 ;
#Tclk data_in = 16'h00_02 ;
#Tclk data_in = 16'h00_03 ;
// add extra value than depth
#Tclk data_in = 16'h00_04 ;
// stack has 1 , 2 , 3

$display ("We read two values buffer: 1 , 2 ");
w = 0 ;
r = 1 ;
#Tclk $display (" Output =%0d" , data_out);
#Tclk $display (" Output =%0d" , data_out);
r = 0 ;
// stack has 3
$display ("We Write another 3 values in the buffer: 5 , 6 , 7 (note 7 will not be
stored)");
w = 1 ;
data_in = 16'h00_05 ;
#Tclk data_in = 16'h00_06 ;
#Tclk data_in = 16'h00_07 ;
w = 0 ;
// stack has 3 , 5 , 6
$display ("We Write & read at same time: write 8 & read 3");
w = 1 ;
r = 1 ;
data_in = 16'h00_08 ;
#Tclk $display (" Output =%0d" , data_out);
// stack has 5 , 6 , 8
$display ("We read all: 5 , 6 , 8 ");
w = 0 ;
r = 1 ;
#Tclk $display (" Output =%0d" , data_out);
#Tclk $display (" Output =%0d" , data_out);
#Tclk $display (" Output =%0d" , data_out);
$stop ;
end
endmodule

```

## Output



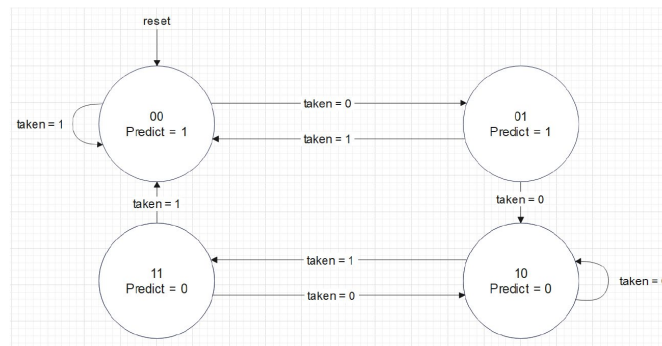
The screenshot shows the Visual Studio Code interface with the Verilog file `Buffer_tb.v` open. The code defines a testbench for a buffer. The terminal window displays the output of the simulation, which includes the values written to and read from the buffer. A red box highlights the output of the `$stop` command, showing the final state of the buffer.

```
verilog > Lab2 > Buffer_tb.v
51  r = 1 ;
52  data_in = 16'h00_08 ;
53  #Tclk $display (" Output =%0d" , data_out);
54  // stack has 5 , 6 , 8
55
56  $display ("We read all: 5 , 6 , 8 ");
57  w = 0 ;
58  r = 1 ;
59  #Tclk $display (" Output =%0d" , data_out);
60  #Tclk $display (" Output =%0d" , data_out);
61  #Tclk $display (" Output =%0d" , data_out);
62
63  $stop ;
64
65  end

TERMINAL OUTPUT DEBUG CONSOLE PROBLEMS
# // 18 U.S.C. Section 1905.
# //
# Loading sv_std.std
# Loading work.FIFO_tb(fast)
#
VSIM 1> run -all
# run -all
#
# We Write into 3 depth values buffer: 1 , 2 , 3 , 4 (note 4 will not be stored)
# We read two values buffer: 1 , 2
# Output =1
# Output =2
# We Write another 3 values in the buffer: 5 , 6 , 7 (note 7 will not be stored)
# We Write & read at same time: write 8 & read 3
# Output =3
# We read all: 5 , 6 , 8
# Output =5
# Output =6
# Output =8
# ** Note: $stop : buffer_tb.v(63)
# Time: 120 ns Iteration: 0 Instance: /FIFO_tb
# Break at buffer_tb.v line 63
VSIM 2>
```

---

4-Write a Verilog code that implement this state machine. Using Moore.



---

```
module FSM (input clk , rst , taken , output reg predict);
integer count ;
localparam s0 = 2'b00 , s1 = 2'b01 , s2 = 2'b10 , s3 = 2'b11 ;
reg [1:0] pr , nxt ;
always @(posedge clk ) begin
    if (rst == 1) pr = s0 ;
    else pr = nxt ; end
always @(pr,taken) begin
    case (pr)
    s0 : begin
        predict = 1'b1 ;
        if (taken==0) nxt = s1 ;
        else nxt = s0 ; end
    s1 : begin
        predict = 1'b1 ;
        if (taken==0) nxt = s2 ;
        else nxt = s0 ; end
    s2 : begin
        predict = 1'b0 ;
        if (taken==0) nxt = s2 ;
        else nxt = s3 ; end
    s3 : begin
        predict = 1'b0 ;
        if (taken==0) nxt = s2 ;
        else nxt = s0 ; end
    default : begin
        nxt = s0 ; predict = 1'b1 ; end
    endcase
end
endmodule
```

---

## Test bench

---

```
module FSM_tb;
reg clk = 0 , rst , taken ; wire predict ; parameter Tclk = 4 ;
FSM U (clk , rst , taken , predict) ;

always
forever #(Tclk/2) clk = ~ clk ;

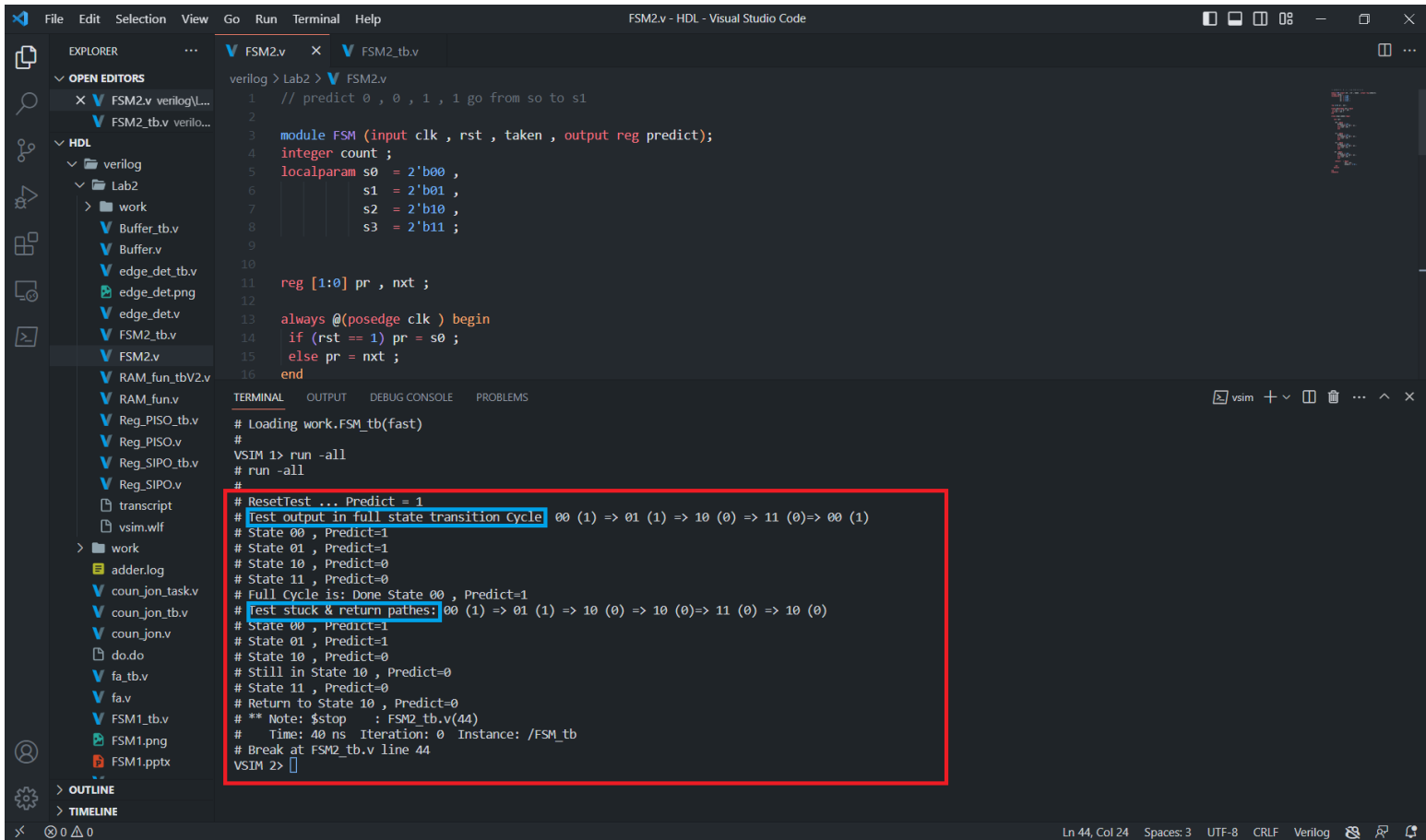
initial begin

rst = 1 ; #Tclk $display ("ResetTest ... Predict = %b", predict) ;
rst = 0 ;

$display ("Test output in full state transition Cycle: 00 (1) => 01 (1) => 10 (0)
=> 11 (0)=> 00 (1) ") ;
$display ("State 00 , Predict=%b" , predict) ;
taken = 1'b0;
#Tclk $display ("State 01 , Predict=%b" , predict) ;
taken = 1'b0;
#Tclk $display ("State 10 , Predict=%b" , predict) ;
taken = 1'b1;
#Tclk $display ("State 11 , Predict=%b" , predict) ;
taken = 1'b1;
#Tclk $display ("Full Cycle is: Done State 00 , Predict=%b" , predict) ;

$display ("Test stuck & return pathes: 00 (1) => 01 (1) => 10 (0) => 10 (0)=> 11
(0) => 10 (0)") ;
$display ("State 00 , Predict=%b" , predict) ;
taken = 1'b0;
#Tclk $display ("State 01 , Predict=%b" , predict) ;
taken = 1'b0;
#Tclk $display ("State 10 , Predict=%b" , predict) ;
taken = 1'b0;
#Tclk $display ("Still in State 10 , Predict=%b" , predict) ;
taken = 1'b1;
#Tclk $display ("State 11 , Predict=%b" , predict) ;
taken = 1'b0;
#Tclk $display ("Return to State 10 , Predict=%b" , predict) ;
$stop ;
end
endmodule
```

## Result



The screenshot displays the Visual Studio Code interface with a Verilog file named `FSM2.v` open. The code defines an FSM module with inputs `clk`, `rst`, and `taken`, and an output `reg predict`. It includes a counter and several state variables. The simulation results in the terminal show the FSM's behavior, including state transitions and predictions.

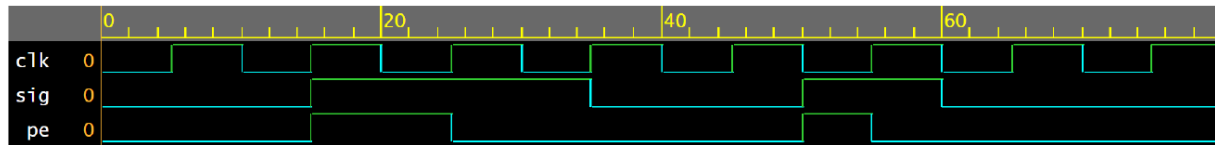
```
verilog > Lab2 > FSM2.v
1 // predict 0, 0, 1, 1 go from s0 to s1
2
3 module FSM (input clk , rst , taken , output reg predict);
4 integer count ;
5 localparam s0 = 2'b00 ,
6             s1 = 2'b01 ,
7             s2 = 2'b10 ,
8             s3 = 2'b11 ;
9
10
11 reg [1:0] pr , nxt ;
12
13 always @(posedge clk ) begin
14     if (rst == 1) pr = s0 ;
15     else pr = nxt ;
16 end
```

Terminal Output:

```
# Loading work.FSM_tb(fast)
#
VSIM 1> run -all
# run -all
#
# ResetTest ... Predict = 1
# Test output in full state transition cycle 00 (1) => 01 (1) => 10 (0) => 11 (0) => 00 (1)
# State 00 , Predict=1
# State 01 , Predict=1
# State 10 , Predict=0
# State 11 , Predict=0
# Full cycle is: Done State 00 , Predict=1
# Test stuck & return pathes: 00 (1) => 01 (1) => 10 (0) => 10 (0) => 11 (0) => 10 (0)
# State 00 , Predict=1
# State 01 , Predict=1
# State 10 , Predict=0
# Still in State 10 , Predict=0
# State 11 , Predict=0
# Return to State 10 , Predict=0
# ** Note: $stop : FSM2_tb.v(44)
# Time: 40 ns Iteration: 0 Instance: /FSM_tb
# Break at FSM2_tb.v line 44
VSIM 2>
```

---

5-Write a Verilog code that implements a positive edge detector.



---

```
module det (input clk , sig , output reg pe) ;
reg in_edge ;
always @(posedge sig)
in_edge = 1'b1 ;
always @(posedge clk , posedge in_edge) begin
if (in_edge==1) pe=1'b1;
else pe=1'b0 ;
in_edge=1'b0;
end
endmodule
```

---

Test bench

---

```
module det_tb ;
reg clk = 0 , sig =0;
wire pe ;
parameter T = 10 ;

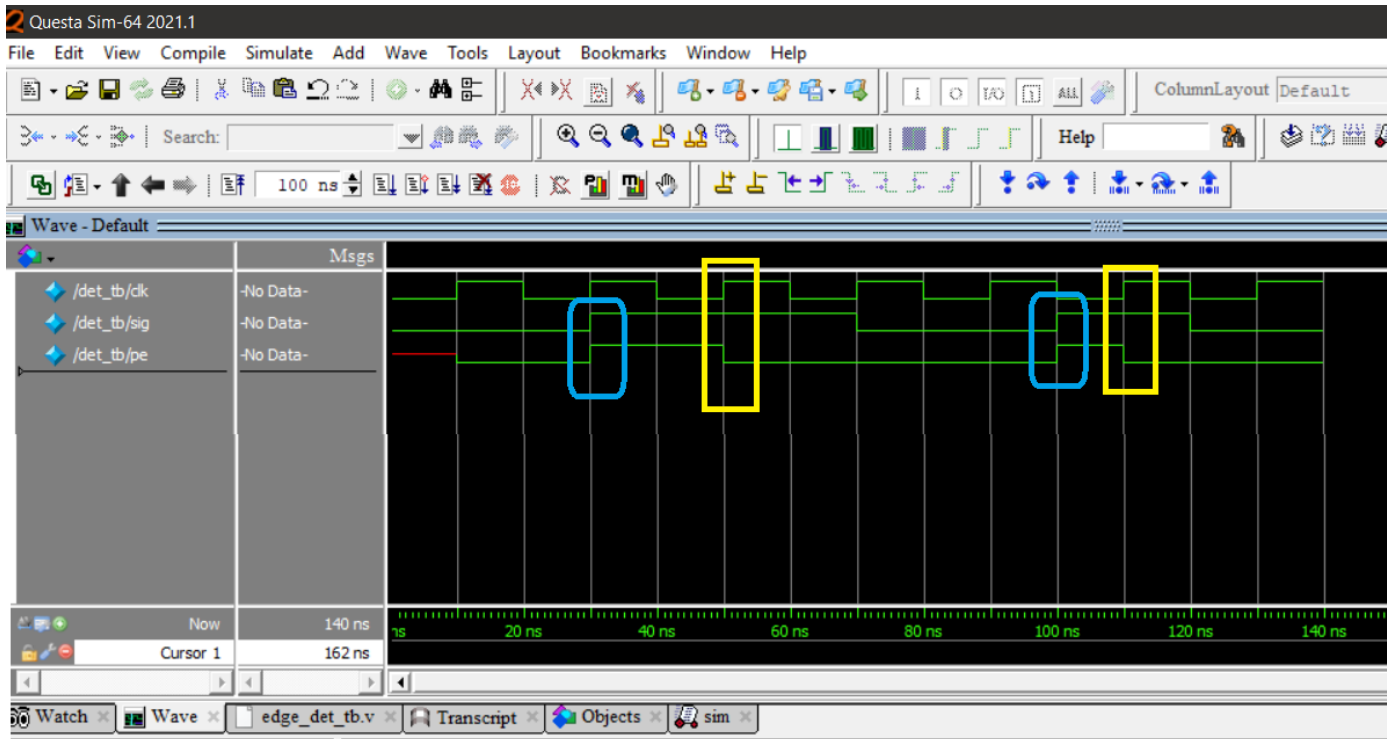
det U (clk , sig , pe) ;

always
forever #(T) clk = ~clk ;

initial begin
$monitor ("Clk=%b Sig=%b Pe=%b", clk , sig , pe);
#(3*T) sig = 1'b1 ;
#(4*T) sig = 1'b0 ;
#(3*T) sig = 1'b1 ;
#(2*T) sig = 1'b0 ;
#(2*T) $stop ;
end
endmodule
```



## --Result



edge\_det.v - HDL - Visual Studio Code

```
verilog > Lab2 > V edge_det.v
1 module det (input clk , sig , output reg pe) ;
2
3 reg in_edge ;
4
5 always @(posedge sig)
6   in_edge = 1'b1 ;
7
8
9 always @(posedge clk , posedge in_edge) begin
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