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Submit:

PCI Target Report

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Table of Contents

Table of Figures

Block Diagram:

Here, we can see the block diagram of PCI Target [Figure 1]. The diagram consists of the PCI bus which carry the signals and the target.
The target consists of:

- Address decoder that checks if the address is valid or not.
- Main memory
- Buffer
- I/O Registers
- Target controller

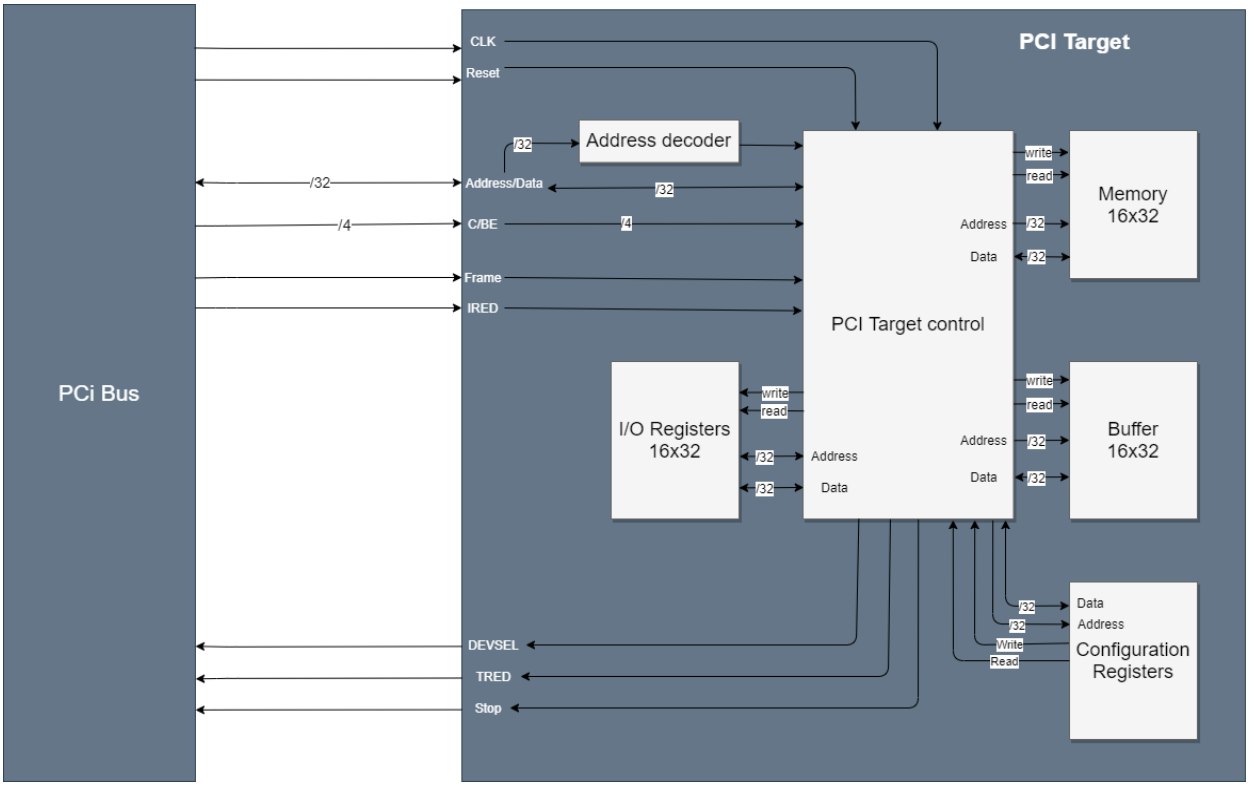


Figure 1: Block diagram

Signal Descriptions:

External signals:

Signal	Type	Description
CLK	In	The PCI system clock provides timing for all transactions. The clock frequency operates up to 33MHz. This clock is also used to provide timing to the Target and master.
NRST	In	The asynchronous PCI system reset is used to set the PCI device to a starting known and stable state. It forces all PCI signals, sequencers, and registers to an initialized state.
AD [31:0]	In/out	Multiplexed lines used for address and data.
C/BE [3:0]	In	Bus command and byte enable signals. During the data phase, the lines indicate which of the four-byte lanes carry meaningful data.
NFRAME	In	The NFRAME signal is driven by the current master and used to indicate the start of cycle and the duration of the cycle
NIRED	In	The initiator ready signal indicates that the current master is ready for the data phase (to write or read data).
NTRDY#	Out	The target ready signal indicates that the current target is ready for the data phase (to write or read data).
NDEVSEL#	Out	Initialization Device Select. Used as a chip select during configuration read and write transactions.
NSTOP	Out	Indicates that current target wishes the initiator to stop the current transaction.

Internal Registers:

Signal	Description
[31:0] IN_Memory [0:15]	The main memory of the target.
[31:0] buffer [0:15]	Extra memory to handle the overflow and not lose data.
[31:0] mask	mask the data with byte enable to get the valid date before writing it in the memory.
[31:0] recieved_address	Save the address in the address phase and act as memory index in read and write commands.
[3:0] buffer_ptr	Flag for the buffer to trace the process of transfer data from memory to buffer and to check if the buffer is full or empty.
[31:0] Data	register to get the data from the memory and place it on the address_data in the data phase.
[3:0] control	Register to save the C/BE in the address phase.
Write_NRead	Flag to control the address_data bus (1 for write, 0 for read or idle state).
[3:0] Dev_flag	Flag for dev select to assert DEVSEL & TRDY after IRDY asserted by one cycle.
[4:0] stop_flag	Stop flag to trace the process of stop the current transaction.
[31:0] message	Save the message in the special cycle.
m_done	Flag to check if the message saved only one time.
mast_rdy	Check if the master is ready or not in the positive edge of the CLK
confg_data	Save the configuration data in configuration write
confg_flag_write	flag to check if the configuration data saved only one time
confg_flag_read	flag to check if the configuration data send only one time
dual_flag	Check if it's dual cycle to read the address in two phases

Internal signals:

Signal	Description
dev_trdy	Assert the DEVSEL and TRDY after the IRED asserted by one cycle in medium mood.
end_trans	Indicates the end of the transaction so all signals would deasserted.
read_op	Indicates that the command is read operation in the address phase
index	Index of the memory
add_valid	Indicates that the address on the bus in the address phase is belong to the current target.
Add_IO_valid	set 1 if the address is in the target input output addresses range
special_cycle_start	Asserted when the C/BE is special cycle in the address bus.
master_target_ready	Asserted when both master and target are ready.
mem_full_buffer_empty	Asserted in case the memory is full, and the buffer is empty
mem_full_buffer_full	Asserted when both the memory and the buffer are full
read_trigger	Trigger the read block.

PCI Commands:

C/BE	Command
0000	Interrupt Acknowledge
0001	Special Cycle
0010	I/O Read
0011	I/O Write
0100	Reserved
0101	Reserved
0110	Memory Read
0111	Memory Write
1000	Reserved
1001	Reserved
1010	Configuration Read
1011	Configuration Write
1100	Memory Read Multiple
1101	Dual address Cycle
1110	Memory Read Line
1111	Memory Write and Invalidate

Different scenarios:

Memory Write:

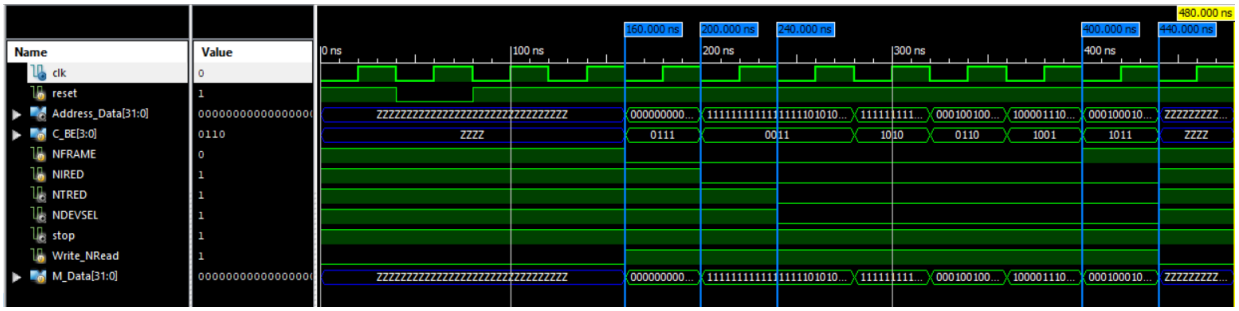


Figure 2: Memory Write

CLK	Phase	Description
1	Idle	The bus is in the idle state and all signals are deasserted.
2	Reset	The reset signal is asserted to make sure all signals are initialized.
3	Idle	The bus is in the idle state and all signals are deasserted.
4	Idle	The bus is in the idle state and all signals are deasserted.
5	Address	The initiator places a valid address and places a write command on the C/BE signals.
6	Data 1	The initiator places a valid data on AD and byte enable on C/BE signals. The initiator asserts NIRED low indicating valid data is available.
7	Wait	The initiator waits for the target to receive the data from the last clk. The target asserts NDEVSEL low as an acknowledgment it has decoded the address. The target asserts TRDY# low indicating it is ready to capture the data. The target captures the valid data.
8	Data 2	The initiator provides new data and byte enable. The target captures the valid data.
9	Data 3	The initiator provides new data and byte enable. The target captures the valid data.
10	Data 4	The initiator provides new data and byte enable. The target captures the valid data.
11	Data 5	The initiator deasserts NFRAME indicating this is the final data phase. The initiator provides new data and byte enable. The target captures the valid data.
12	Turn around	The initiator puts the NFRAME#, address_data and C_BE signals in turn around cycle and deasserts NIRED and keep it high for one cycle to end the transaction. The target deasserts NTRDY and NDEVSEL for one cycle.

Memory Read:

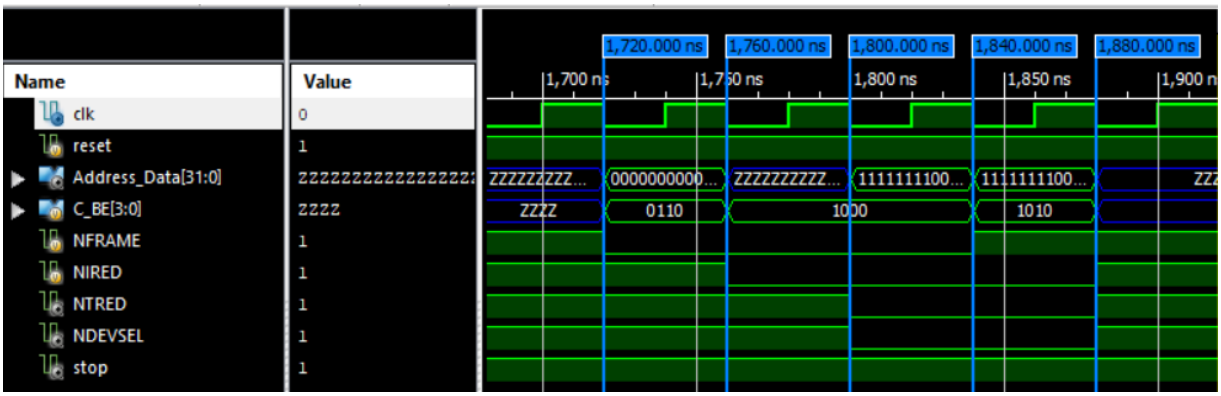


Figure 3: Memory Read

CLK	Phase	Description
1	Idle	The bus is in the idle state and all signals are deasserted.
2	Address	The initiator places a valid address and places a memory read command on the C_BE signals. The target saves the address in received_address and save the C_BE in control registers.
3	Turn around	The initiator leaves the address bus and drive it by high impedance (z). The initiator asserts NIRED indicating it is ready to receive data. The initiator provides the byte enable.
4	Data 1	The target asserts NDEVSEL as an acknowledgment it has decoded the address. The target asserts NTRED indicating it is ready to send the data. The target provides valid data. The initiator captures the valid data.
5	Data 2	The initiator deasserts NFRAME indicating this is the final data phase. The initiator provides the byte enable. The target provides valid data. The initiator captures the valid data.
6	Turn around	The initiator puts the NFRAME#, address_data and C_BE signals in turn around cycle and deasserts NIRED and keep it high for one cycle to end the transaction. The target deasserts NTRDY and NDEVSEL for one cycle.

Additional Features:

Memory Read Line:

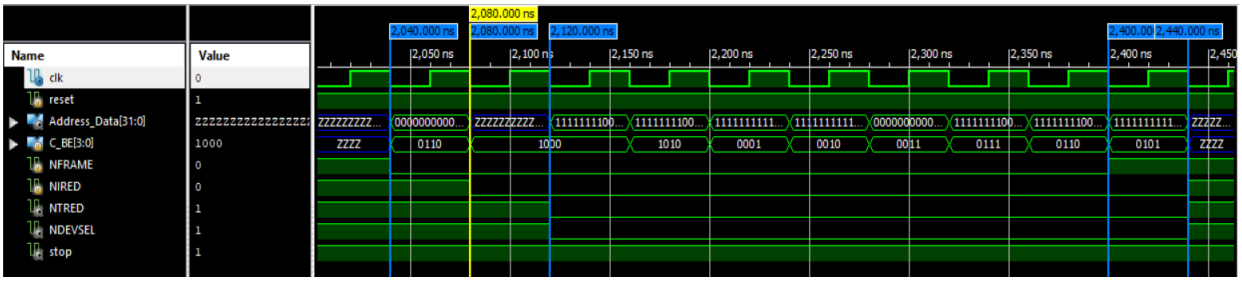


Figure 4: Memory Read Line

CLK	Phase	Description
1	Idle	The bus is in the idle state and all signals are deasserted.
2	Address	The initiator places a valid address and places a memory read command on the C_BE signals. The target saves the address in received_address and save the C_BE in control registers.
3	Turn around	The initiator leaves the address bus and drive it by high impedance (z). The initiator asserts NIRED indicating it is ready to receive data. The initiator provides the byte enable.
4	Data 1	The target asserts NDEVSEL as an acknowledgment it has decoded the address. The target asserts NTRED indicating it is ready to send the data. The target provides valid data. The initiator captures the valid data.
5-10	Data 2 – 7	The initiator provides the byte enable. The target provides valid data. The initiator captures the valid data.
11	Data 8	The initiator deasserts NFRAME indicating this is the final data phase. The initiator provides the byte enable. The target provides valid data. The initiator captures the valid data.
12	Turn around	The initiator puts the NFRAME#, address_data and C_BE signals in turn around cycle and deasserts NIRED and keep it high for one cycle to end the transaction. The target deasserts NTRDY and NDEVSEL for one cycle.

Memory Read multiple:

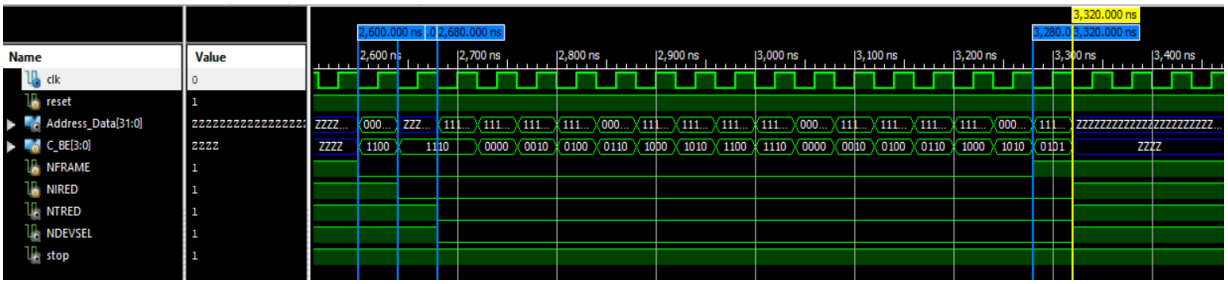


Figure 5: Memory Read Multiple

CLK	Phase	Description
1	Idle	The bus is in the idle state and all signals are deasserted.
2	Address	The initiator places a valid address and places a memory read command on the C_BE signals. The target saves the address in received_address and save the C_BE in control registers.
3	Turn around	The initiator leaves the address bus and drive it by high impedance (z). The initiator asserts NIRED indicating it is ready to receive data. The initiator provides the byte enable.
4	Data 1	The target asserts NDEVSEL as an acknowledgment it has decoded the address. The target asserts NTRED indicating it is ready to send the data. The target provides valid data. The initiator captures the valid data.
5-18	Data 2 – 15	The initiator provides the byte enable. The target provides valid data. The initiator captures the valid data.
19	Data 16	The initiator deasserts NFRAME indicating this is the final data phase. The initiator provides the byte enable. The target provides valid data. The initiator captures the valid data.
20	Turn around	The initiator puts the NFRAME#, address_data and C_BE signals in turn around cycle and deasserts NIRED and keep it high for one cycle to end the transaction. The target deasserts NTRDY and NDEVSEL for one cycle.

Special Cycle:

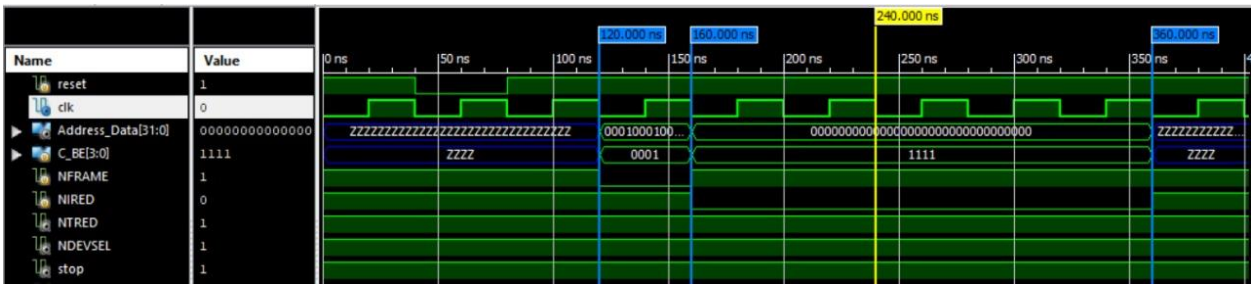


Figure 6: Special Cycle

CLK	Phase	Description
1	Idle	The bus is in the idle state and all signals are de-asserted.
2	Address	The initiator places a non-valid address and places a special cycle command on the C_BE signals. The initiator asserts the NFRAME.
3	Message	The initiator asserts NIRED. The initiator de-asserts the NFRAME. The initiator provides the byte enable. The initiator places the message on the bus. The target receives the message and saves it in a register.
4, 5, 6	Wait	The initiator leaves the message for three cycles.
6	Turn around	The initiator puts address_data and C_BE signals in turn around cycle and de-asserts NIRED and keep it high for one cycle to end the transaction.

Configuration Write:

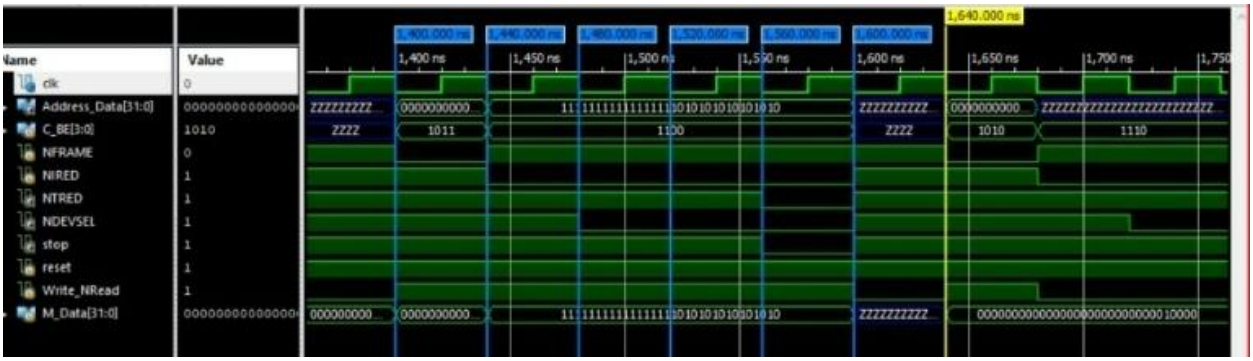


Figure 7: Configuration Write

CLK	Phase	Description
1	Idle	The bus is in the idle state and all signals are de-asserted.
2	Address	The initiator places a valid BAR(Base Address Register) address and places a configuration write command on the C/BE signals. NFRAME is asserted low by the initiator.
3	Data 1	The initiator places a valid data on AD and byte enable on C/BE signals. The initiator asserts NIRED low indicating valid data is available. NFRAME is de-asserted by the initiator.
4	Wait	The initiator waits for the target to receive the data from the last clk. The target asserts NDEVSEL low as an acknowledgment it has decoded the address. Target saves the data.
5	Data1	The target puts the data on the address bus.
6	Wait	The target asserts TRDY# indicating that the transfer is complete. The target asserts stop to disconnect any possible burst-mode transfer attempt.
7	Turn around	address data and C_BE signals in turn around cycle and de-asserts NIRED and keep it high for one cycle to end the transaction. The target de-asserts NTRDY, stop and NDEVSEL at least for one cycle.

Configuration Read:

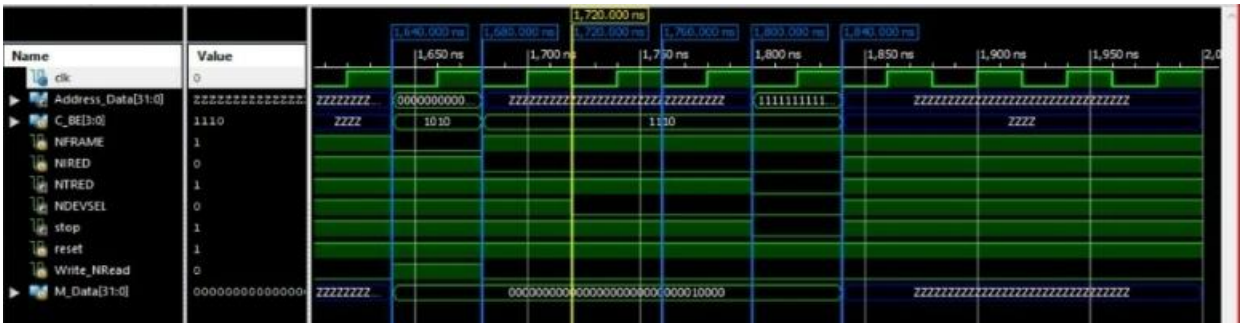


Figure 8: Configuration Read

CLK	Phase	Description
1	Idle	The bus is in the idle state and all signals are de-asserted.
2	Address	The initiator places a valid BAR(Base Address Register) address and places a configuration read command on the C/BE signals. NFRAME is asserted low by the initiator.
3	Wait	The initiator places byte-enable on C/BE signals. The initiator asserts NIRED low indicating that the byte-enable and address are valid. NFRAME is de-asserted by the initiator. Address bus enters turn around cycles to give the bus to the target for sending the data.
4	Wait	The target asserts NDEVSEL low as an acknowledgment it has decoded the address. Target gets the data from the BAR(BASE Address Register).
5	Mask	The target masks the data and saves it in BAR memory.
6	Wait	The target asserts TRDY#, and the stop low indicating that it has written.
7	Turn around	address data and C_BE signals in turn around cycle and de-asserts NIRED and keep it high for one cycle to end the transaction. The target de-asserts NTRDY, stop and NDEVSEL at least for one cycle.

I/O Memory Write & Read:

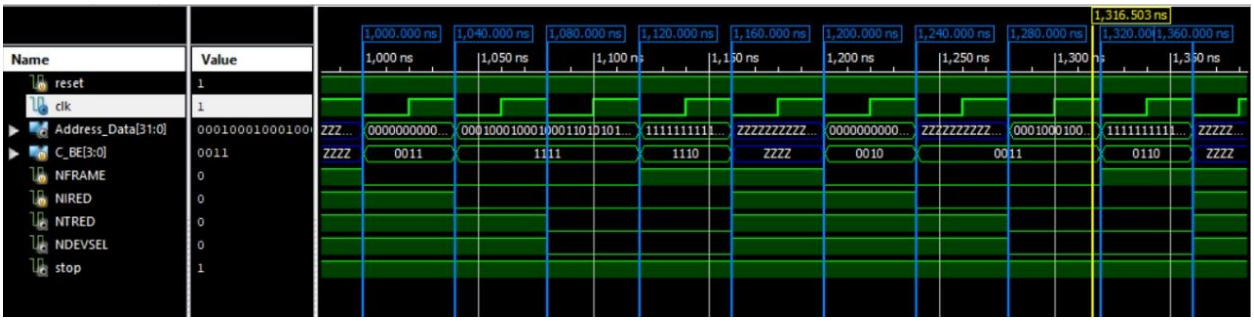


Figure 9: I/O Write & Read

CLK	Phase	Description
1	Idle	The bus is in the idle state and all signals are de-asserted.
2	Address	The initiator places a valid i/o address and places a i/o write command on the C/BE signals.
3	Data 1	The initiator places a valid data on AD and byte enable on C/BE signals. The initiator asserts NIRED low indicating valid data is available.
4	Wait	The initiator waits for the target to receive the data from the last clk. The target asserts NDEVSEL low as an acknowledgment it has decoded the address. The target asserts TRDY# low indicating it is ready to capture the data. The target captures the valid data.
5	Data 2	The initiator provides new data and byte enable. The target captures the valid data. The initiator de-asserts the NFRAME#.
6	Turn around	The initiator puts the NFRAME#, address_data and C_BE signals in turn around cycle and deasserts NIRED and keep it high for one cycle to end the transaction. The target deasserts NTRDY and NDEVSEL for one cycle.
7	Idle	The bus is in the idle state and all signals are de-asserted.
8	Address	The initiator places a valid i/o address and places a i/o memory read command on the C_BE signals. The target saves the address in received_address and save the C_BE in control registers.
9	Turn around	The initiator leaves the address bus and drive it by high impedance (z). The initiator asserts NIRED indicating it is ready to receive data. The initiator provides the byte enable.
10	Data 1	The target asserts NDEVSEL as an acknowledgment it has decoded the address. The target asserts NTRED indicating it is ready to send the data. The target provides valid data. The initiator captures the valid data.
11	Data 2	The initiator de-asserts NFRAME indicating this is the final data phase. The initiator provides the byte enable. The target provides valid data. The initiator captures the valid data.
12	Turn around	The initiator puts the NFRAME#, address_data and C_BE signals in turn around cycle and de-asserts NIRED and keep it high for one cycle to end the transaction. The target de-asserts NTRDY and NDEVSEL for one cycle.

Dual Address Cycle Write:

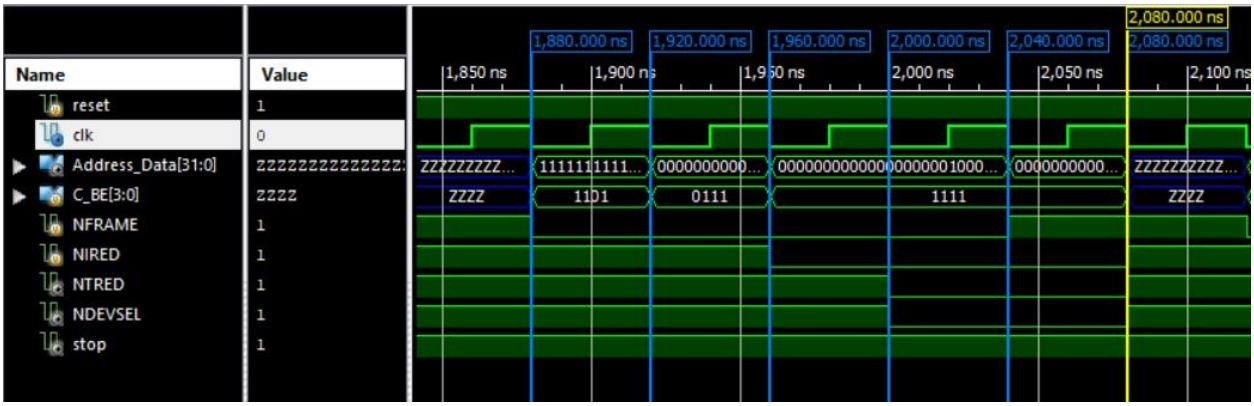


Figure 10: Dual Address Cycle Write

CLK	Phase	Description
1	Idle	The bus is in the idle state and all signals are de-asserted.
2	Address1	The initiator places the low half of the valid address and places a DAC command on the C/BE signals.
3	Address2	The initiator places the high half of the valid address and places a write command on the C/BE signals.
4	Data 1	The initiator places a valid data on AD and byte enable on C/BE signals. The initiator asserts NIRED low indicating valid data is available.
5	Wait	The initiator waits for the target to receive the data from the last clk. The target asserts NDEVSEL low as an acknowledgment it has decoded and concatenated the two halves of the address. The target asserts TRDY# low indicating it is ready to capture the data. The target captures the valid data.
6	Data 2	The initiator provides new data and byte enable. The target captures the valid data. The initiator de-asserts the NFRAME#.
7	Turn around	The initiator puts the NFRAME#, address_data and C_BE signals in turn around cycle and de-asserts NIRED and keep it high for one cycle to end the transaction. The target de-asserts NTRDY and NDEVSEL for one cycle.

Dual Address Cycle Read:

Figure 11: Dual Address Cycle Read

CLK	Phase	Description
1	Idle	The bus is in the idle state and all signals are de-asserted.
2	Address1	The initiator places the low half of the valid address and places a DAC command on the C/BE signals.
3	Address2	The initiator places the high half of the valid address and places a read command on the C/BE signals.
3	Turn around	The initiator leaves the address bus and drive it by high impedance (z). The initiator asserts NIRED indicating it is ready to receive data. The initiator provides the byte enable.
4	Data 1	The target asserts NDEVSEL as an acknowledgment it has decoded and concatenated the two halves of the address. The target asserts NTRED indicating it is ready to send the data. The target provides valid data. The initiator captures the valid data.
5	Data 2	The initiator de-asserts NFRAME indicating this is the final data phase. The initiator provides the byte enable. The target provides valid data. The initiator captures the valid data.
12	Turn around	The initiator puts the NFRAME#, address_data and C_BE signals in turn around cycle and de-asserts NIRED and keep it high for one cycle to end the transaction. The target de-asserts NTRDY and NDEVSEL for one cycle.

Fatal Cases:

Memory read master not ready:

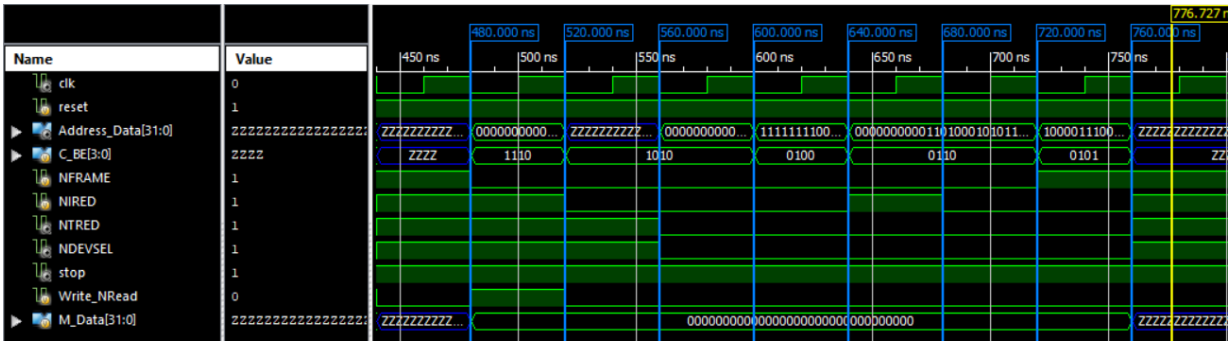


Figure 12: Memory read master not ready

CLK	Phase	Description
1	Idle	The bus is in the idle state and all signals are deasserted.
2	Address	The initiator places a valid address and places a memory read command on the C_BE signals. The target saves the address in received_address and save the C_BE in control registers.
3	Turn around	The initiator leaves the address bus and drive it by high impedance (z). The initiator asserts NIRED indicating it is ready to receive data. The initiator provides the byte enable.
4	Data 1	The target asserts NDEVSEL as an acknowledgment it has decoded the address. The target asserts NTRED indicating it is ready to send the data. The target provides valid data. The initiator captures the valid data.
5	Data 2	The initiator provides the byte enable. The target provides valid data. The initiator captures the valid data.
6	Data 3	The initiator provides the byte enable. The target provides valid data. The initiator captures the valid data. The initiator deasserts NIRED indicating it is busy and can't capture any data.
7	Wait	The target is wait for the initiator to be ready and capture the data. The initiator asserts NIRED and capture the valid data.
8	Data 4	The initiator deasserts NFRAME indicating this is the final data phase. The initiator provides the byte enable. The target provides valid data. The initiator captures the valid data.
9	Turn around	The initiator puts the NFRAME#, address_data and C_BE signals in turn around cycle and deasserts NIRED and keep it high for one cycle to end the transaction. The target deasserts NTRDY and NDEVSEL for one cycle.

Write overflow:

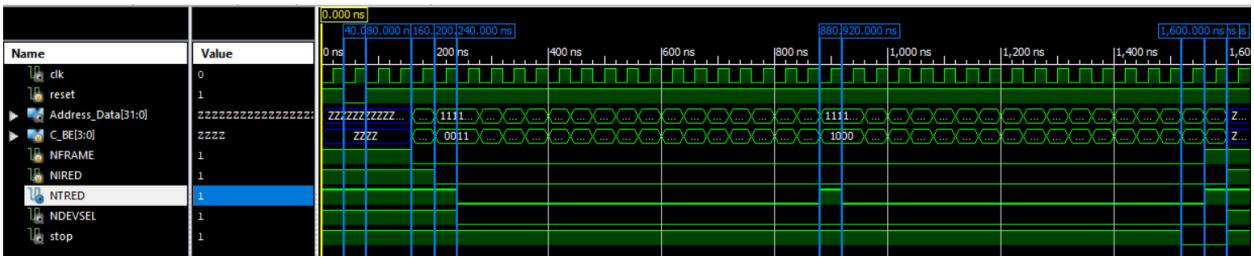


Figure 13: Write overflow

CLK	Phase	Description
1	Idle	The bus is in the idle state and all signals are deasserted.
2	Reset	The reset signal is asserted to make sure all signals are initialized.
3	Idle	The bus is in the idle state and all signals are deasserted.
4	Idle	The bus is in the idle state and all signals are deasserted.
5	Address	The initiator places a valid address and places a write command on the C/BE signals.
6	Data 1	The initiator places a valid data on AD and byte enable on C/BE signals. The initiator asserts NIRED low indicating valid data is available.
7	Wait	The initiator waits for the target to receive the data from the last clk. The target asserts NDEVSEL low as an acknowledgment it has decoded the address. The target asserts TRDY# low indicating it is ready to capture the data. The target captures the valid data.
8 - 22	Data 2 - 16	The initiator provides new data and byte enable. The target captures the valid data.
9	Data 17	The initiator provides new data and byte enable. The target captures the valid data.
10	Data 4	The initiator provides new data and byte enable. The target captures the valid data.
11	Data 5	The initiator deasserts NFRAME indicating this is the final data phase. The initiator provides new data and byte enable. The target captures the valid data.
12	Turn around	The initiator puts the NFRAME#, address_data and C_BE signals in turn around cycle and deasserts NIRED and keep it high for one cycle to end the transaction. The target deasserts NTRDY and NDEVSEL for one cycle.

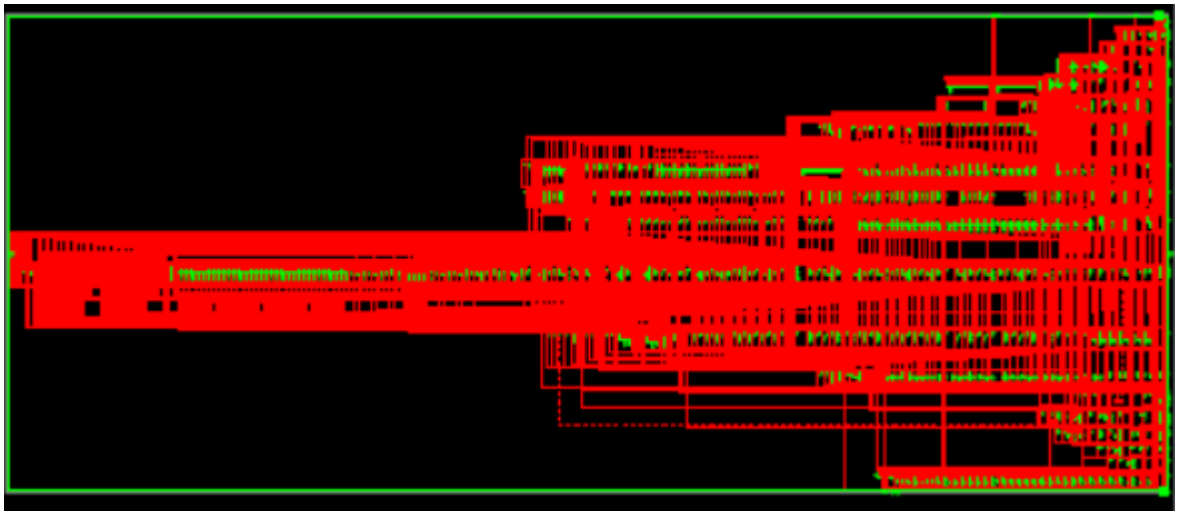
Memory Read overflow:

The system handles the read overflow when the initiator wants to read more than the capacity of the memory. Each time the index exceeds the memory range it will reset to the first index of the memory.

The overflow handling exists in all read operations.

Its figure is same as any read operation figures.

RTL



Contributions:

Ahmed Mohamed Ahmed Abd El-Hamed	Memory read, Memory read line, Report
Aya Sameh Mazhar Mohamed	Memory write, special cycle, Report
Bassant Yasser Soltan	I/O Memory read, Dual cycle read and write, Report
Basmala Magdy Ali Abo El-Nasr	I/O Memory write, configuration read, power point
Sarah Mohamed Ahmed Ahmed	Memory read multiple, configuration write, power point