Microinstructions

DESIGN OF CONTROL WORD

- 4 BITS FOR OUT ALL REGISTERS (Rsrc_out,Rdst_out,PC_out,IR_out,X_out,Y_out,Z-OUT,MDR-OUT,MAR-OUT) F1
- 3 BITS FOR IN ALL REGISTERS (Rdst_IN,Rsrc_IN,PC_IN,IR_in,Z_in) F2
- 3 BIT IN FOR (X_in,Y_in,MDR_in,MAR_in) F3
- 5 BITS FOR ALU OPERATIONS F4
- 2 BITS FOR 0 OPERAND F5 (RST / STOP CLK)
- 2 BIT FOR READ/WRITE F6
- 1 BIT FOR WFMC F7
- 2 BITS FOR SET CARRY,CLEAR CARRY,CLEAR Y F8
- 3 BITS FOR uPC STATUS F9
- 1 BIT FOR PLA F10

F1 OUT REG	F2 IN REG	F3 TMP IN	F4 ALU	F5 0 OP	F6 READ/WRITE	F7 WFMC	F8 SET/CLEAR	F9 Upc Status	F10 PLA
4 BITS	3 BITS	3 BITS	5 BITS	2 BITS	2 BITS	1 BIT	2 BITS	3 BITS	1 BIT

DESIGN OF CONTROL STORE

Memory Access	CLK CYCLES	CONTROL WORD	Comment	F9/F10	Address
1	3	PC_out,MAR_in,Read,Clr_y,Set_Cry,ADC,Zin		000/0	000 000 000
		Zout,PC_in,WFMC		000/0	000 000 001
		MDR_out,IR_in (PLA=1)		000/1	000 000 010
0	1	Rsrc_out,Xin	Register Direct	001/1	001 000 000
1	3	Rsrc_out,MAR_in,Read,CLR_y,setCry,ADC,Zin	AutoIncrement	001/0	001 001 000
		Zout,Rsrc_in,WFMC		001/0	
		MDR_out,Xin (PLA=1)		001/1	
1	3	Rsrc_out,Clr_y,setCry,SBC,Zin	Autodecrement	001/0	001 010 000
		Zout,Rsrc_in,MAR_in,Read,WFMC		001/0	
		MDR_out,Xin (PLA=1)		001/1	
2	6	PC_out,MAR_in,Read,Clr_y,Set_Cry,ADC,Zin	Indexed	001/0	001 011 000
		Zout,PC_in		001/0	
		Rsrc_out,Y_in,WFMC		001/0	
		MDR_out,ADD,Zin		001/0	
		Zout,MAR_in,Read,WFMC		001/0	
		MDR_out,Xin (PLA=1)		001/1	
1	2	Rsrc_out,MAR_in,Read,WFMC	Register Indirect	001/0	001 100 000
		MDR_out,Xin (PLA=1)		001/1	
2	4	Rsrc_out,MAR_in,Read,CLR_y,setCry,ADC,Zin	AutoIncrement IND	001/0	001 101 000
		Zout,Rsrc_in,WFMC		001/0	
		MDR_out,MAR_in,Read,WFMC		001/0	
		MDR_out,Xin (PLA=1)		001/1	
2	4	Rsrc_out,Clr_y,setCry,SBC,Zin	Autodecrement IND	001/0	001 110 000
		Zout,Rsrc_in,MAR_in,Read,WFMC		001/0	
		MDR_out,MAR_IN,READ,WFMC		001/0	
		MDR_out,Xin (PLA=1)		001/1	

3	7	PC_out,MAR_in,Read,Clr_y,Set_Cry,ADC,Zin	Indexed IND	001/0	001 111 000
		Zout,PC_in		001/0	
		Rsrc_out,Y_in,WFMC		001/0	
		MDR_out,ADD,Zin		001/0	
		Zout,MAR_in,Read,WFMC		001/0	
		MDR_out,MAR_in,READ,WFMC		001/0	
		MDR_out,Xin (PLA=1)		001/1	
		-----Destination routines----------			
0	1	Rdst_out,Yin (PLA=1)	Register Direct	010/1	010 000 000
1	3	Rdst_out,MAR_in,Read, CLR_y, setCry,ADC,Zin	AutoIncrement	010/0	010 001 000
		Zout,Rdst_in,WFMC		010/0	
		MDR_out,Yin (PLA=1)		010/1	
1	3	Rdst_out,Clr_y,setCry,SBC,Zin	Autodecrement	010/0	010 010 000
		Zout,Rdst_in,MAR_in,Read,WFMC		010/0	
		MDR_out,Yin (PLA=1)		010/1	
2	6	PC_out,MAR_in,Read,Clr_y,Set_Cry,ADC,Zin	Indexed	010/0	010 011 000
		Zout,PC_in		010/0	
		Rdst_out,Y_in,WFMC		010/0	
		MDR_out,ADD,Zin		010/0	
		Zout,MAR_in,Read,WFMC		010/0	
		MDR_out,Yin (PLA=1)		010/1	
1	2	Rdst_out,MAR_in,Read,WFMC	Register IND	010/0	010 100 000
		MDR_out,Yin (PLA=1)		010/1	
2	4	Rdst_out,MAR_in,Read,CLR_y,setCry,ADC,Zin	AutiIncrement IND	010/0	010 101 000
		Zout,Rdst_in,WFMC		010/0	
		MDR_out,MAR_in,Read,WFMC		010/0	
		MDR_out,Yin(PLA=1)		010/1	

2	4	Rdst_out,Clr_y,setCry,SBC,Zin	Autodecrement IND	010/0	010 110 000
		Zout,Rdst_in,MAR_in,Read,WFMC		010/0	
		MDR_out,MAR_IN,READ,WFMC		010/0	
		MDR_out,Yin (PLA=1)		010/1	
3	7	PC_out,MAR_in,Read,Clr_y,Set_Cry,ADC,Zin	Indexed IND	010/0	010 111 000
		Zout,PC_in		010/0	
		Rdst_out,Y_in,WFMC		010/0	
		MDR_out,ADD,Zin		010/0	
		Zout,MAR_in,Read,WFMC		010/0	
		MDR_out,MAR_in,READ,WFMC		010/0	
		MDR_out,Yin (PLA=1)		010/1	
		---------ALU----------			
0	1	F=X,Zin	MOV	011/1	011 000 000
0	1	F=X+Y,Zin	ADD	011/1	011 000 001
0	1	F=X+Y+Cry_in,Zin	ADC	011/1	011 000 010
0	1	F=Y-X,Zin	SUB	011/1	011 000 011
0	1	F=Y-X-Cry_in,Zin	SBC	011/1	011 000 100
0	1	F=X&Y,Zin	AND	011/1	011 000 101
0	1	F=X|Y,Zin	OR	011/1	011 000 110
0	1	F=X^Y,Zin	XOR	011/1	011 000 111
0	1	F=Y-X	CMP	011/1	011 001 000
				011/1	
0	1	F=Y+1	INC	011/1	100 000 000
0	1	F=Y-1	DEC	011/1	100 000 001
0	1	F=0	CLR	011/1	100 000 010
0	1	F=!Y	INV	011/1	100 000 011
0	1	F=Y>>1	LSR	011/1	100 000 100
0	1	F=ror(Y)	ROR	011/1	100 000 101
0	1	F=Y>>1 | insert msb from right	ASR	011/1	100 000 110
0	1	F=Y<<1	LSL	011/1	100 000 111
0	1	F=rol(Y)	ROL	011/1	100 001 000

0	3	------Branch Routine-------			
		IRout, Yin		100/0	101 000 000
		PC_out,ADD,Zin		100/0	101 000 001
		Zout,PC_in (PLA=1)		100/1	101 000 010
		----------Write result----------			
0	1	Zout,Rdst_out	(Write In Register If Register Direct Mode)	101/1	110 000 000
1	1	Zout,MDR_in,Write,WFMC	(Write In Memory)	110/1	110 000 001
		---------- 0 Operand ----------			
0	1	Set Reset bit	RST	111/1	111 000 000
0	1	CLR RAM uPC=0 PC=0	HLT	111/1	111 000 001

System Analysis

- **2 OPERANDS**
- **Fetch + Src + Dst + ALU +Write**
- **Instruction CMP doesn't write (no mem access & clk for write)**

SRC	DST	Memory Access	Clk cycles
Register	Register	1	7
	Register Indirect	3	8
	Autoincrement	3	9
	Autoincrement Indirect	4	10
	Autodecrement	3	9
	Autodecrement indirect	4	10
	Indexed	4	12
	Indexed Indirect	5	13
Register Indirect	Register	2	8
	Register Indirect	4	9
	Autoincrement	4	10
	Autoincrement Indirect	5	11
	Autodecrement	4	10
	Autodecrement indirect	5	11
	Indexed	5	13
	Indexed Indirect	6	14
Autoincrement	Register	2	9
	Register Indirect	4	10
	Autoincrement	4	11

	Autoincrement Indirect	5	12
	Autodecrement	4	11
	Autodecrement indirect	5	12
	Indexed	5	14
	Indexed Indirect	6	15
Autoincrement Indirect	Register	3	10
	Register Indirect	5	11
	Autoincrement	5	12
	Autoincrement Indirect	6	13
	Autodecrement	5	12
	Autodecrement indirect	6	13
	Indexed	6	14
	Indexed Indirect	7	16
Autodecrement	Register	2	9
	Register Indirect	4	10
	Autoincrement	4	11
	Autoincrement Indirect	5	12
	Autodecrement	4	11
	Autodecrement indirect	5	12
	Indexed	5	14
	Indexed Indirect	6	15
Autodecrement indirect	Register	3	10
	Register Indirect	5	11
	Autoincrement	5	12

	Autoincrement Indirect	6	13
	Autodecrement	5	12
	Autodecrement indirect	6	13
	Indexed	6	15
	Indexed Indirect	7	16
Indexed	Register	3	12
	Register Indirect	5	13
	Autoincrement	5	14
	Autoincrement Indirect	6	15
	Autodecrement	5	14
	Autodecrement indirect	6	15
	Indexed	6	17
	Indexed Indirect	7	18
Indexed Indirect	Register	4	13
	Register Indirect	6	14
	Autoincrement	6	15
	Autoincrement Indirect	7	16
	Autodecrement	6	15
	Autodecrement indirect	7	16
	Indexed	7	18
	Indexed Indirect	8	19

- **1 operand**
- **Fetch + Dst +ALU +Write**

Dst	Memory Access	Clk cycles
Register	1	6
Register Indirect	3	7
Autoincrement	3	8
Autoincrement Indirect	4	9
Autodecrement	3	8
Autodecrement indirect	4	9
Indexed	4	11
Indexed Indirect	5	12

- **Branch**

Condition	Memory Access	Clk cycles
True	1	6
False	1	3

- **0 operand**

Memory Access	Clk cycles
1	4

- **AVG CLK Cycles per instruction**

2 operands	**12**
1 operand	**8**
0 operand	**4**
Branch	**5**

- **AVG CLK Cycles in system = 9**