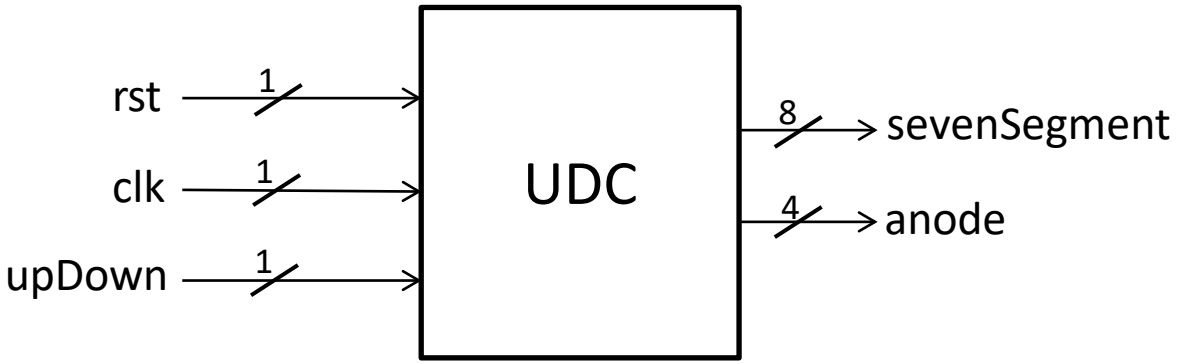
One Digit Up-Down Counter (UDC)

Design Description:

- In this lab exercise you will design, test and implement one digit up down counter application. On FPGA board we have 4 seven segments displays and for this design we want to implement up – down counter only using one of the seven segments display.
- Note that we don’t provide initial code for your design, so please generate new verilog file.
- It should count from 0 to 9 and 9 to 0 according to one of the input (upDown)

Design I/O:

rst:	1 bit input for reset
clk:	1 bit input for clock
upDown:	1 bit input coming from a push-button
sevenSegment:	8 bit output
anode:	4 bit output



Design Behavior:

- Output anode should be assigned 4'b0111 to make active only one seven-segment display out of 4.
- On the seven-segment display, we should see 0 if the rst signal is high, otherwise it should increment or decrement one by one depending on upDown input signal. If upDown is 1, it should increment (from 0 to 9 and jumps back to 0 and continue increasing) and if upDown is 0, it should decrement (from 9 to 0 and jumps back to 9 and continue decreasing).
- Do not forget to implement the delay logic from your previous labs to slow down incrementing or decrementing. Otherwise, numbers on display can not be seen.