State Machine
with Debounce

Design Description:

- For this lab exercise, you will design a state machine and use a debounce module to obtain a clear input signal.
- Note that we don’t provide initial code for the state machine, so you should generate a new Verilog file and instantiate debounce module in your design.
- When the push button is pressed to generate a single transition from 0 to 1 or from 1 to 0, it generates multiple transitions because of the tendency of any two metal contacts to bounce.
- Debounce circuit aims to eliminate the multiple transitions.
- When the push button is pressed, it should trigger a counter, and your circuit should ignore input for a short while. That is, for as long as the timer counts.

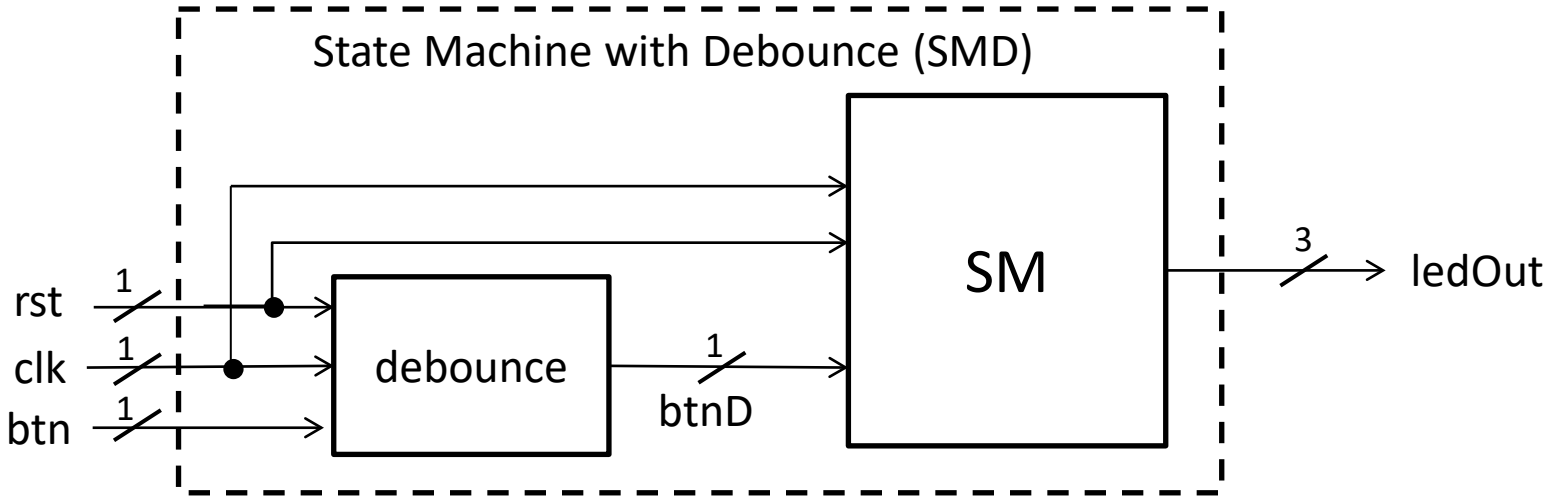
Design I/O:

rst: 1 bit input for reset

clk: 1 bit input for clock

btn: 1 bit input coming from a push-button

ledOut: 3 bit output



Design Behavior:

- State machine part of your design is depict on the right hand side. You have 4 states and an input btn to direct the transition between states and output ledOut at each state.
- For debounce circuit, your design should ignore input for a short while after push button is pressed. To do that, you should trigger a counter and while counting you should ignore input.