EE462 HDL Based Digital Systems Design
Lab 6

1. Design a combinational hardware that performs the following vector matrix multiplication (for example, O1 = I1x10 + I2x8 + I3x4), adds the values in the resulting vector (O = O1+O2+O3) and outputs the result (O). I1, I2, I3 values are 8-bit integers in the range [0-255].

$$[I1\ I2\ I3] \times \begin{bmatrix} 10 & 9 & 4 \\ 8 & 4 & 6 \\ 4 & 2 & 7 \end{bmatrix} = [O1\ O2\ O3]$$

In your hardware, you are not allowed to use multiplier hardware for implementing multiplication with a constant. This operation should be implemented using shifter and adder hardware.

Write a Verilog RTL module implementing your hardware. Your Verilog RTL module should have the following inputs: I1 (8 bit), I2 (8 bit), I3 (8 bit). It should have the following output: O (16 bit).

Synthesize your code; it shouldn't give any errors or "latch inferred" warnings. When you're done, go to your ISE project folder and copy the file with the .syr extension somewhere convenient. It contains your synthesis report.

2. Design a sequential hardware that performs the following vector matrix multiplication (for example, O1 = I1x10 + I2x8 + I3x4), adds the values in the resulting vector (O = O1+O2+O3) and outputs the result (O). I1, I2, I3 values are 8-bit integers in the range [0-255].

$$[I1\ I2\ I3] \times \begin{bmatrix} 10 & 9 & 4 \\ 8 & 4 & 6 \\ 4 & 2 & 7 \end{bmatrix} = [O1\ O2\ O3]$$

In your hardware, you are not allowed to use multiplier hardware for implementing multiplication with a constant. This operation should be implemented using shifter and adder hardware. In your hardware, you should use 6 adders.

Write a Verilog RTL module implementing your hardware. Your Verilog RTL module should have the following inputs: clk (1 bit), reset (1 bit), I1 (8 bit), I2 (8 bit), I3 (8 bit). It should have the following output: O (16 bit). Write a Verilog testbench module which verifies your Verilog RTL module.

Synthesize your code; it shouldn't give any errors or "latch inferred" warnings. When you're done, go to your ISE project folder and copy the file with the .syr extension somewhere convenient.

Upload your .v files (including the testbench) and the synthesis reports to LMS.