7 Segment Display Driver

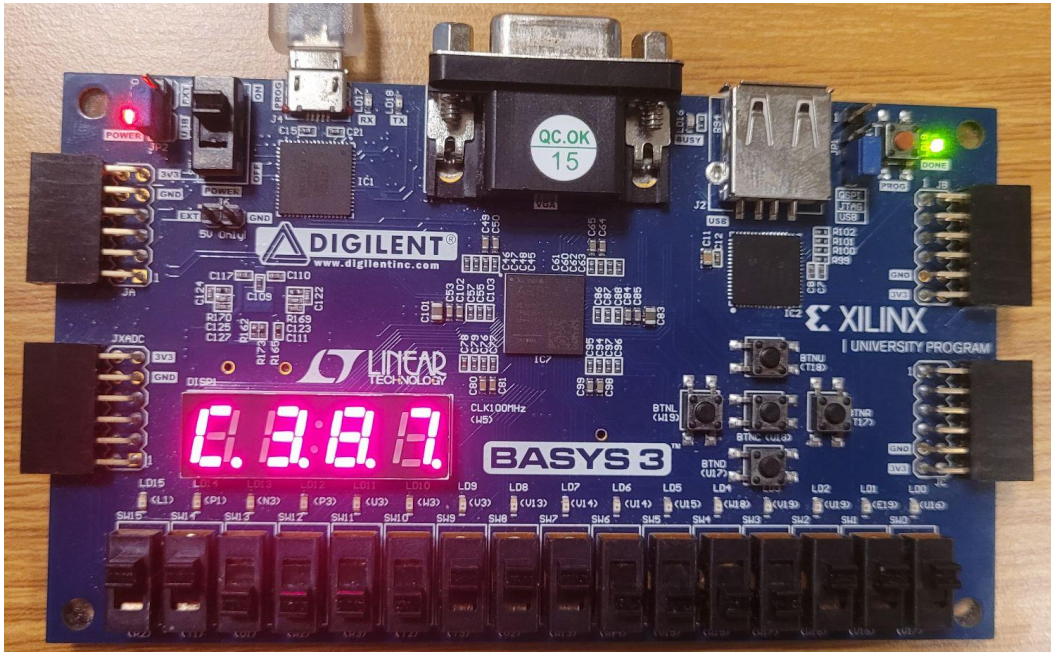
Design Top Level:

- Inputs
  - dataIn[15:0] will be mapped to the switches on the board.
  - clk will be connected to the clock pin.
  - rst will be connected to a button on the board.
- Outputs
  - anode[3:0] will be connected to 7 segment anode pins.
  - sevenSeg[7:0] will be connected to each of the seven segment displays.

Design Behavior:

- There are 4 displays. Each 4 bits input out of 16 is assigned for one of the display.
- You need to update the active display within an order. To do that you need 16 bits counter at least. Such that;
- When counter[15:14] == 00, you should drive first display and deactivate the rest. To do that you should assign anode = 4'b0111;
- When counter[15:14] == 01, you should assign anode = 4'b1011; to drive second display and deactive the rest.
- When counter[15:14] == 10, you should assign anode = 4'b1101; for third one.
- When counter[15:14] == 11, you should assign anode = 4'b1110; for last one.

Design Behavior:



As it can be seen from the picture above, 4 different 4-bit data (max value = F (15)) will be entered from switches and the output should be observed on 7-segment display instantaneously.